LOGIC ANALYZER

INTRODUCTION:

This analyzer is designed to work in conjunction with the developmental sysytem. All the operation is controlled by the developmental system software. The operation is similar to the Motorola Microprocessor Analyzer (Model MPA-1). However, it has a more sophisticated triggering capability. The capacity of data sampling is much greater - (256 maximum). The clock speed can go up to about 2 MHz. With a faster capture RAM replacement (bipolar RAM) the clock rate could be about 4 MHz.

OPERATIONAL DESCRIPTION:

The analyzer has mainly two modes of operation, Nth Trigger Mode and Continuous Mode. In both modes, the game data (16 bit address lines, 8 bit data bus lines and 8 bit external data) are latched in by $\Phi 2$ and stored in the Capture RAM. At the end of capturing the data, the valid data could be properly formatted and displayed on a T.V. monitor by the software. The triggering point can be specified by the triggering data (Trigger Pattern Data and Mask Bit Data).

Nth Trigger Mode:- The number of trigger counts can be specified prior to the start. Then after the count is satisfied, 127 words of data are sampled into the Capture RAM. The number of valid data words since the start until the last trigger is stored in a latch. The address for the Capture RAM where the last trigger occured is also stored in a latch. From these two information items, only the valid data words could be displayed and the trigger point could be indicated. The maximum number of the valid data before the last trigger is 128.

Continuous Mode:- In this mode, the data words are continuously sampled until the stop signal is sent. The triggering address for the Capture RAM holds the last trigger address before the stop signal. The valid data counts before the trigger is stored in a latch. After the trigger, 63 data words are sampled and the trigger is ignored during that time. The maximum number of the data previous to the trigger is 64.

DETAIL OF FUNCTIONAL DESCRIPTION:

Trigger Circuit:- 32 bits of data from the game board (16 bit address, 8 bit data bus and 8 bit external data) are latched into 74S374 (8 bit edge-triggered latch) on every falling edge of the $\Phi 2$ clock. The latched data is fed into the compare logic to produce a trigger

signal. The latched game data are first EXCLUSIVE ORed to the Pattern Data then, NANDed with the Mask Bit Data. Finally, all the individual bits are ANDed together. The logical operation is as follows.

$$\text{TRIGGER} = \overline{(\text{GAME DATA } \emptyset \oplus \text{PATTERN } \emptyset) \cdot \text{MASK } \emptyset} \cdot \overline{(\text{GAME DATA 1} \oplus \text{PATTERN 1}) \cdots\cdots \overline{(\text{Game Data 31} \oplus \text{Pattern 31}) \cdot \text{MASK 31}}}$$

TRIGGER ENABLE:

The trigger generated from the Trigger Circuit is passed to several sections, Trigger Counter, Data Counter, Valid Data Counter and Trigger Address Latch, according to the mode and the state of the analyzer.
Nth Trigger Mode:- The trigger is enabled after the start signal from Start Control. The trigger is sent to the clock input of the Trigger Counter until the Nth count is reached, then the trigger is disabled.
Continuous Mode:- The trigger is enabled after the start signal and kept enabled except while the Data Counter is counting 63 data words from the last trigger. At the end of the count the trigger is enabled again. This allows the analyzer to sample 63 valid data words after a trigger.

END SIGNAL GATE:

The two ripple signals from the trigger Counter and the Data Counter are ANDed together.
Nth Trigger Mode:- The end signal is generated when both the Trigger and Data Counters, reach the end of the count. Then the end signal is sent to the Stop Control logic to stop writing to the Capture RAM and turn on the Data Valid Flag. 127 words of data after the last trigger are sampled in this way.
Continuous Mode:- The end signal is generated on every 63 counts from the last trigger. Then it switches the page of the Capture RAM since the RAM is divided into two portions, 128 data words each.

DATA VALID FLAG LATCH:

The rising edge of the End Signal sets the flag. The flag is cleared when the analyzer is started. In Nth trigger mode, the flag indicates the completion of the data sampling. In continuous mode, it indicates that at least once, the trigger has occured and 63 data words have been sampled.

CAPTURE RAM:

The data from the Data Latch is written into the RAM with $R/\overline{W}$ low going pulses and the address input from the Address Counter when the analyzer is sampling the data. The sampled data are read out to the devlopmental system data bus with the output enable signal (CAPTURE RAM READ) and the address input from the devlopmental system address bus when the analyzer is stopped.

PAGE SELECT:

In the Nth trigger mode, the input E7 (the most significant bit of the Data Counter is sent to the input of the Address MPX (E7*). In the continuous mode, a J-K flip-flop, set to toggle, is triggered by the End Signal and the output is sent to the input of the Address MPX as the most significant bit of the Capture RAM address (E7*). The 256 locations are divided into two portions, 128 locations each, and switched at every end signal.

CAPTURE RAM WRITE ENABLE GATE:

The output from the Stop Control, CAPRAMEN, and $\overline{\text{WRITE}}$ signal (Game Φ2) are NANDed together to produce WRITE (CAPRAMCK). Therefore, when CAPRAMEN is low, the CAPRAMCK is high to disable writing into the CAPTURE RAM.

TRIGGER ADDRESS LATCH:

The addresses from the Address Counter and the Page Select, EØ - E7*, are latched on every Q TRIG. The address of the Capture RAM where the trigger has occured is saved and used in displaying the data.

VALID DATA COUNTER:

The counter is preset to 0 at the rising edge of the TRIGEN signal and counted up until 128 (in Nth trigger mode) or 64 (in Continuous mode) count is reached then stopped. The qualified trigger signal (QTRIG) latches the counter output number. This latched number represents the number of valid data words from the time of start until the time of the last trigger.

START CONTROL:

Nth Trigger Mode:- The start signal from the developmental system is synchronized to the Game Ø 2 and the trigger is enabled. At the same time, a preset signal is sent to the Stop Control logic to enable the write signal for the Capture RAM. Also the Data Valid Flag is cleared. At the end of 127 data word count after the Nth trigger, the start control is cleared to disable the trigger. The start control is cleared any time by the stop signal.

Continuous Mode:- The start control enables the trigger and clears the Data Valid Flag. After every trigger, the trigger is disabled until the 63 data count ends. The controls could be cleared any time by the stop signal.

STOP CONTROL:

Nth Trigger Mode:- The Stop Control enables the write signal for the Capture RAM by the start signal. The write signal could be disabled either by the end signal after 127 words of data are sampled or the Stop Control could be activated from the developmental system at any time.

Continuous Mode:- The start signal enable the write signal. Activating the Stop Control from the developmental system disables the write signal. If the Data Counter is in the process of counting 63 data words at the time, the write signal would be disabled at the end of the count to ensure the 63 data word sampling after the last trigger.

ADDRESS COUNTER:

This counter is counting upwards from 0 through 255 and back to 0, synchronized to Game Ø 2. The counter outputs EØ through E6 are directly fed to the Address MPX. The most significant output E7 goes into the Page Select to divide 256 locations into two portions, 128 each, in the Continuous mode. In the Nth trigger mode, E7 is directly passed to the Address MPX.

ADDRESS MPX:

When the sampled data is read out by the developmental system, the address bus AØ through A7 of the devlopmental system is sent to the Capture RAM. At all other times, the address is supplied from the Address Counter (EØ - E6) and the Page Select (E7).

MODE CONTROL LATCH:

The 4 bits of data from the developmental system data bus are latched to chose the modes. Logic one on the DØ selects the continuous mode and logic one on the D1 selects the Nth trigger mode. D2 and D3 are reserved for future expansion.

STATUS REGISTER:

Two status signals could be read out to the developmenta system data bus through this port. D7 is the Data Valid Flag Latch and D6 is the CAPRAMEN. D6 should be looked at after the stop signal is sent to the analyzer since the capture RAM might be in the process of sampling 63 data words after the last trigger. At the end of the sample, D6 would be low.

PROGRAMMING REFERENCE:

Input signals to the logic analyzer. (Memory address in [ ]).

START [B4ØA]: Starts the logic analyzer.

STOP [B4ØB]: Stops the analyzer.
In Nth trigger mode, it is honored any time. In continuous mode, it is honored after 63 data words are sampled since the last trigger.

TRIGGER COUNT: [B4Ø8]

Loads in the trigger count number in the Nth trigger mode. If one is loaded, the analyzer acts as a one-shot mode. Zero represents a count of 256. In continuous mode, the trigger count number is ignored.

MODE CONTROL: [B4Ø9]

Selects the mode, Nth trigger mode or continuous mode. Logic "one" on DØ corresponds to the continuous mode and logic "one" on D1 for the Nth trigger mode. DØ and D1 can not have logic "one" simultaneously.

TRIGGER CIRCUIT:

The analyzer has two basic data patterns used to produce a trigger; Bit Pattern and Bit Mask. The trigger would occur on any desired address, data and external data by setting Bit Pattern, however, any bit is ignored by storing zero in Bit Mask latch.

$$\text{TRIGGER} = \overline{(\text{ADDPTN} \oplus \text{ADDRESS} + \overline{\text{ADDMSK}})} \cdot \overline{(\text{DATA PTN} \oplus \text{DATA} + \overline{\text{DATAMSK}})} \cdot \overline{(\text{EXTPTN} \oplus \text{EXTDATA} + \overline{\text{EXTMSK}})}$$

All individual bits are ANDed.

LAADHPTN [B4ØØ] High byte of address pattern latch.

LAADLPTN [B4Ø1] Low byte of address pattern latch

LADPTN [B4Ø2] Data bus pattern latch.

LAXPTN [B4Ø3] External data pattern latch.

LAADHMSK [B4Ø4] High byte of address mask bit latch.

LAADLMSK [B4Ø5] Low byte of address mask bit latch.

LADMSK [B4Ø6] Data bus mask bit latch.

LAXMSK [B4Ø7] External data mask bit latch.

Output signals from the logic analyzer.

LARAMSELØ [BØØØ - BØFF] High byte address captured data.

LARAMSEL1 [B1ØØ - B1FF] Low byte address captured data.

LARAMSEL2 [B2ØØ - B2FF] Data bus captured data.

LARAMSEL3 [B3ØØ - B3FF] External Data captured data

Status Register [B5ØØ]

D7 Data Valid Flag

D6 Capture RAM write enable.

Trigger Address Latch [B51Ø]

The address of the Capture RAM where the last trigger occured.

Pretrigger Valid Data Counter[B4ØC]

The number of valid data words before the last trigger.

PROGRAMMING PROCEDURE:

Nth Trigger Mode:-

- Load all the pattern and mask bit latches
- Set the mode to Nth trigger mode by storing Ø2 in the mode control [B4Ø9]
- Load the trigger count number in the Trigger Counter[B4Ø8] If one is stored, the analyzer acts as a one-shot mode. Ø is equivalent to 256 count.

. Write into START [B4ØA].

. Wait for the Data Valid Flag to go high, D7 of the Status Register..

. The operation could be terminated by referencing STOP B4ØB with R/$\overline{W}$ low..

. If the Data Valid Flag becomes high, proceed to display.

. In display routine, the trigger address from the Trigger Address Latch [B51Ø] and the number of valid data words before the last trigger from the Pretrigger Valid Data Counter [B4ØC] should be read out. The 256 locations are wrapped around. The valid data would be, Trigger Address - Pretrigger Valid Data up to Trigger Address +127.

Continuous Mode:-

. Load all the pattern and mask bit latches.

. Store Ø1 in the mode control [B4Ø9] to select the continuous mode.

. Reference the START with R/$\overline{W}$ low..

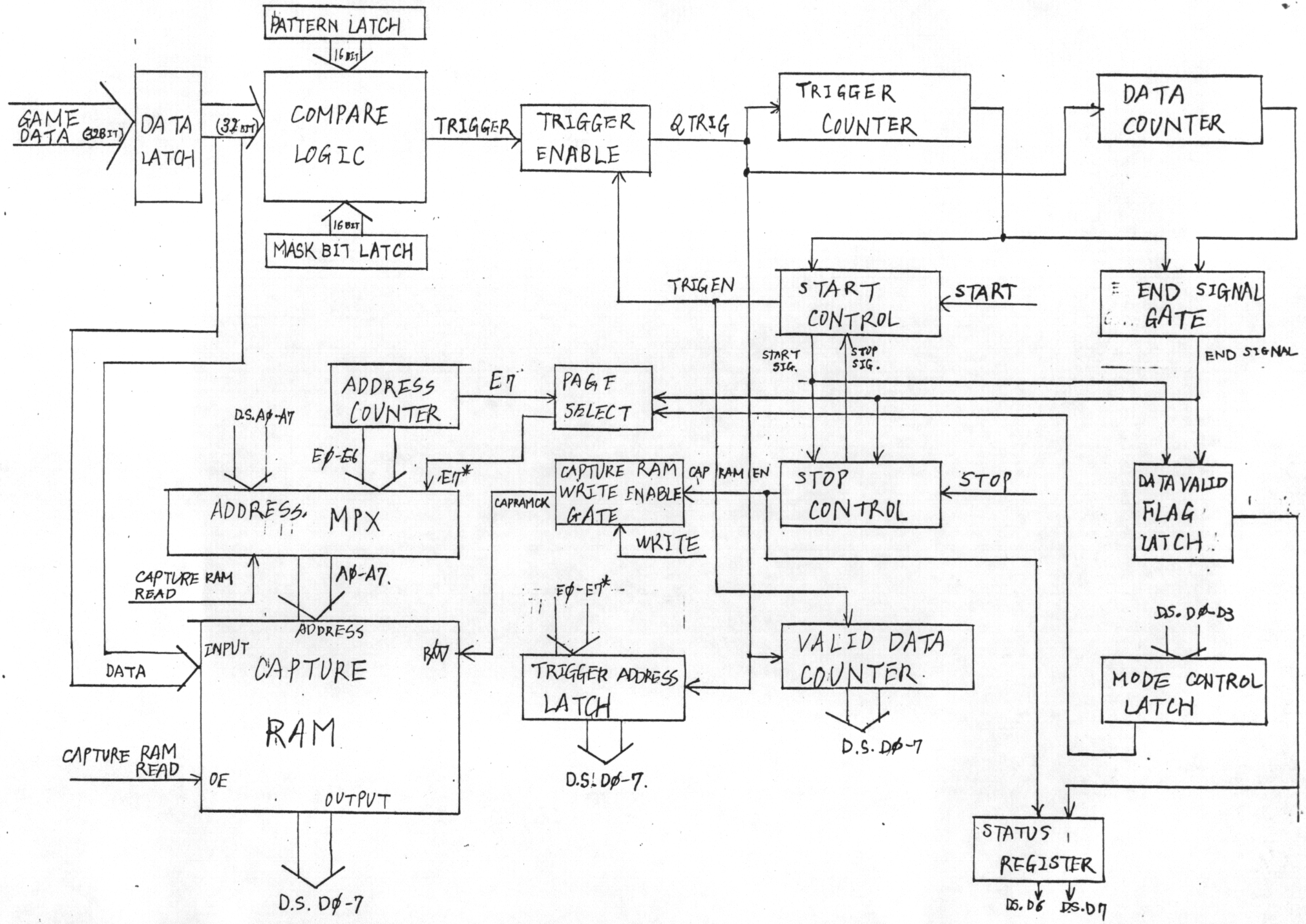
. The Data Valid Flag high indicates that a trigger has occured at least once.

. The analyzer could be stopped at any time.

. Wait for the Capture RAM write enable on D6 of Status Register to be low. This guarantees the 63 data sample after the last trigger.

. In the display routine, the trigger address and the number

. of valid data words before the last trigger should be read out. However, since the 256 locations of the Capture RAM are divided into two portions, 128 locations each, the most significant bit of the trigger address is interpretted as a page number. For page Ø, D7=Ø For page 1, D7=1. Only 63 data words after the last trigger should be displayed. The number of valid data words before the last trigger is saved in the Valid Data Counter. Make sure to keep the page number the same when the valid data are read out from the Capture RAM.



D.S. (Developmental System)

SOFTWARE DEVELOPMENT SYSTEM
LOGIC ANALYZER PCB CIRCUIT DESCRIPTION

1. SYNC CHAIN

THE LATCHES J9 AND K9, AND COUNTERS H9 AND F9 PROVIDE THE SYNCRONIOUS SIGNALS FOR THE 6502A AND THE DYNAMIC RAM REFRESH. THE 6502A PHASE ϕ INPUT GETS $\overline{4H}$, A 1.25MHz CLOCK, AND THE DYNAMIC RAM USES 1F THRU 64F. THE DYNAMIC RAM ALSO USES THE SIGNALS $\overline{RAS}$, $\overline{CAS}$, AND RADSEL, WHICH ARE DERIVED FROM THE SYNC SIGNALS 1H, 2H, AND 10MHz USING LATCHES K9 AND K11. K11 SHOULD BE A 74S74 PART AND K9 SHOULD BE A 74109 IN ORDER TO DRIVE THE RAM INPUTS PROPERLY. (SOME NATIONAL 74LS109 PARTS HAVE BEEN USED SUCCESSFULLY AT POSITION K9). LATCH L8 SUPPLIES THE SIGNAL $\overline{LATCH}$, A SPECIALY DECODED PULSE FOR THE PRE-TRIGGER VALID DATA COUNTER LATCH IN THE ANALYZER SECTION. ALL SYNC SIGNALS START WITH THE 10MHz OSCILLATOR. THIS TYPE OF OSCILLATOR CIRCUIT IS NOT USED IN DESIGN ANY MORE BECAUSE OF ITS INFREQUENT START-UP PROBLEMS. THE INVERTERS AT L10 MUST BE 74H04 OR 74S04.

2. MICROPROCESSOR

SINCE THE PHASE ø INPUT CLOCK FREQUENCY IS 1.25 MHz THE PROCESSOR USED SHOULD BE A 6502A ALTHOUGH I HAVE YET TO SEE A 6502 FAIL AT SPEEDS LESS THAN 1.5 MHz. ¶ K13 IS A DISABLED WATCHDOG RESET CIRCUIT. THE SPLIT PAD BETWEEN 3 SHOULD BE OPEN ONLY FOR SOME TROUBLE SHOOTING OPERATIONS, AS THE SOFTWARE DOESN'T STROBE THE WATCHDOG COUNTER; $\overline{\text{WDGRST}}$ IS INACTIVE. ¶ NMI INTERUPTS THE PROCESSOR EVERY 16.7 ms. THE NMI SIGNAL IS A LOW-GOING PULSE FROM LATCH L11, WHICH IS CLOCKED BY A 60 Hz CLOCK. 60 Hz IS DERIVED FROM AN AC SIGNAL AND THE CIRCUITRY TO DO THIS HAS BEEN THROUGH MANY CHANGES. THE LATEST REVISION USES A 311 COMPARATOR AT L4 TO GENERATE A TTL COMPATIBLE 60 Hz CLOCK.

TASKS OR FUNCTIONS TO BE DONE BY THE PROCESSOR ARE INITIATED BY A LOW IRQ INPUT. THE ACIA, GAME INTERFACE, AND THE PROGRAM RAM PARITY CHECK ARE THE CIRCUITS THAT CAN SIGNAL IRQ.

THE DECODE CIRCUITRY GENERATES READ SIGNALS OUT OF GATES J10, AND K6, AND DECODERS H10, J5, AND J6. THE READ SIGNALS ARE SIMPLE DECODES FROM THE PROCESSOR ADDRESS LINES, THEREFORE NOISY DURING PHASE 1, WHICH IS OK EXCEPT FOR THE SIGNAL $\overline{\text{DSIORD}}$, SO A CAP FIX HAS BEEN APPLIED TO J5-7. THE WRITE SIGNALS OUT OF DECODERS H10, J5, A13, AND A14 ARE DECODED WITH THE SIGNAL $\overline{\text{WTTL}}$ FOR THE PROPER TIMING. $\overline{\text{WTTL}}$ COMES FROM LATCH J7 AND GATE K7.

THE LOWER QUARTER OF THE ADDRESS SPACE, 0000-3FFF, HAS THE PROGRAM RAM, WHICH IS USED FOR THE ANALYZER SECTION PROGRAM. THE SECOND QUARTER, 4000-7FFF, IS UNUSED. DECODER J11 DIVIDES THE UPPER HALF OF THE ADDRESS SPACE AMONG THE REST OF THE CIRCUITS ALLOWING THE UPPER 8K, E000-FFFF, FOR PROGRAM ROM. AT THIS TIME LESS THAN 4K OF THE PROGRAM ROM SPACE IS USED.

POWER-ON OR MANUAL RESET SETS LATCH L8, WHICH CAN BE CLEARED ONLY BY SOFTWARE CONTROL IN ORDER TO SEND A LOW RESET PULSE TO THE GAME INTERFACE RESET LINE.

3. ASYNCRONOUS COMMUNICATIONS INTERFACE ADAPTOR (ACIA)

THIS IS THE COMMUNICATIONS LINK TO THE SOFTWARE DEVELOPMENT SYSTEM TERMINAL. THE CIRCUIT IS BUILT AROUND A MC 68 B50, J15. THE SLOWER MC6850 IS NOT USED BECAUSE OF TIMING PROBLEMS. A BYTE OF DATA FROM THE TERMINAL CAN BE LATCHED SERIALLY THROUGH OPTO-COUPLER L15. THE TWO INPUT LINES, ON L15-2 & L15-3, ARE NOT REFERENCED TO THIS PCB'S GROUND SO TO SEE THE INPUT L15-3 SHOULD BE TIED TO GROUND. THE SIGNAL ON L15-2 SHOULD THEN BE A SERIES OF SQUARE WAVES EVERY FEW SECONDS WITH AN AMPLITUDE OF OVER ½ VOLT RIDING ON ABOUT A 1½ TO 2 VOLT LEVEL. L15-6 PROVIDES A TTL COMPATIBLE SIGNAL, WHICH IS LOADED SERIALLY INTO THE 68B50. WHEN THE INPUT BUFFER IS FULL THE IRQ OUTPUT OF THE 68B50 GOES LOW TO SIGNAL THE PROCESSOR'S IRQ INPUT. BYTES OF DATA CAN BE READ FROM THE 68B50'S INPUT BUFFER OR WRITTEN TO ITS OUTPUT BUFFER VIA THE PROCESSOR'S UNBUFFERED DATA BUSS. BYTES OF DATA FROM THE 68B50'S OUTPUT BUFFER ARE TRANSMITTED SERIALLY THROUGH Q1.

4. PROGRAM RAM

THIS RAM SECTION (E7 THRU E15) IS 16K x 9 BITS OF INFORMATION. 16K x 8 IS USABLE RAM SPACE AND 16K x 1 IS FOR THE PARITY CHECK CIRCUIT. THE RAM IS ARRANGED IN ROWS AND COLUMNS. DURING PHASE 2 THE LOWER 14 BITS OF THE PROCESSOR'S BUFFERED ADDRESS LINES ARE MULTIPLEXED 7 BITS INTO THE ROW SELECT, DURING $\overline{RAS}$, AND 7 BITS INTO THE COLUMN SELECT, DURING $\overline{CAS}$. THE ADDRESS MULTIPLEXERS (F10, F11, F12, AND F13, SHOULD BE 74S153 PARTS AS A 74LS153 CANNOT PROPERLY DRIVE THE RAM INPUTS, SINCE THESE ARE DYNAMIC RAMS THEY MUST BE REFRESHED EVERY 2 MS SO DURING PHASE 1 $\overline{RAS}$ AND $\overline{CAS}$ ALSO OCCUR IN ORDER TO (LOAD INTO) THE RAM ADDRESSING THE SYNC SIGNALS 1F THRU 64F VIA THE MULTIPLEXERS. THIS ACCESSES EVERY ROW AND EVERY COLUMN IN THE RAM ARRAY EACH 100 μS. SO TWICE DURING EACH PROCESSOR CYCLE THE PROGRAM RAM IS ADDRESSED, ONCE DURING PHASE 1 FOR REFRESH, AND ONCE DURING PHASE 2 FOR PROGRAM ACCESS. IF THE PROCESSOR IS READING THE RAM THE SIGNAL $\overline{RAMRD}$ IS ACTIVE LOW

DURING PHASE 2 SO THAT THE PROCESSOR-ADDRESSED DATA FROM THE RAM IS DRIVEN ON THE BUFFERED DATA BUSS BY F15. IF THE PROCESSOR IS WRITING TO THE RAM THE SIGNAL $\overline{\text{RAMWR}}$ IS ACTIVE LOW DURING PHASE 2 SO THAT DATA DRIVEN ON THE DATA BUSS BY H15 FROM THE PROCESSOR CAN BE WRITTEN INTO THE PROCESSOR-ADDRESSED RAM LOCATION. $\overline{\text{RAMWR}}$ HAS A GLITCH ON IT ABOUT 100 ns BEFORE THE REAL WRITE PULSE, BUT IT SHOULD NOT CAUSE A WRITE TO ONE OF THE REFRESH ADDRESSES BECAUSE IT OCCURS AFTER THE RISING EDGE OF $\overline{\text{RAS}}$, WHICH SIGNALS THE START OF THE PHASE 2 CYCLE.

FOR THE PARITY ERROR CIRCUIT TO FUNCTION PROPERLY THE PROGRAM MUST NEVER READ A RAM LOCATION BEFORE IT WRITES TO THAT LOCATION. WHEN A RAM LOCATION IS WRITTEN TO, BR/$\overline{\text{W}}$ APPLIES A LOW INPUT TO THE I INPUT OF THE PARITY GENERATOR F14 SO THAT THE NUMBER OF HIGHS IN THE DATA BYTE TO BE WRITTEN CAN DETERMINED AS ODD OR EVEN. IF ODD A LOW WILL BE PRESENTED TO THE DATA INPUT OF RAM E15, AND IF EVEN A HIGH WILL BE ON E15's DATA INPUT. THEREFORE A 9 BIT DATA PATTERN WITH AN ODD NUMBER

OF HIGHS WILL ALWAYS BE WRITTEN INTO THE RAM LOCATION. WHEN THE PROGRAM READS THAT RAM LOCATION, BR/$\bar{W}$ WILL ALLOW THE DATA BIT IN RAM EIS TO BE THE INPUT AT F14-4 SO THAT THE FULL 9 BIT DATA PATTERN CAN BE SEEN BY THE PARITY GENERATOR. THE NUMBER OF HIGHS AMONG THE 9 BITS SHOULD ALWAYS BE ODD SO THE Σ ODD OUTPUT OF F14 IS HIGH WHEN THE SIGNAL $\overline{\text{RAMRD}}$ CLOCKS IT INTO LATCH J7. IF THERE IS A FAILURE IN THE RAM, IT IS MOST LIKELY THAT ONLY ONE BIT WILL BE WRONG (ONE RAM DEVICE PER DATA BIT) SO THE NUMBER OF HIGHS IN THE 9 BIT DATA PATTERN PRESENTED TO THE PARITY GENERATOR WILL BE EVEN WHEN THE BAD RAM LOCATION IS READ AND THUS J7 WILL LATCH A LOW TO ITS Q OUTPUT, $\overline{\text{PERR}}$. $\overline{\text{PERR}}$ GOES TO THE PROCESSOR'S IRQ INTERUPT, AND THE CURRENT PROGRAM DOESN'T RESET LATCH J7 OR INDICATE TO THE DEVELOPMENT SYSTEM USER THAT A RAM FAILURE OCCURED. CURRENTLY A LED IS BEING ADDED TO THE SIGNAL $\overline{\text{PERR}}$ SO THAT SOMEONE CAN TELL BY THE LED BEING ON THAT A RAM FAILURE HAS OCCURED.

5. GAME COMMUNICATIONS

THE DATA BUSS OF THE GAME INTERFACE PCB (GBBD0 - GBBD7) IS BROUGHT ONTO THE ANALYZER PCB ON CONNECTOR J1 AND IS INTERFACED TO THE ANALYZER'S BUFFERED DATA BUSS VIA THE 8 BIT LATCHES D7 AND D8. DATA TO BE SENT TO THE GAME INTERFACE IS LATCHED INTO D7 USING SIGNAL $\overline{\text{DS1OWRT}}$. THE GAME INTERFACE CAN THEN READ THE DATA BY ENABLING THE OUTPUTS OF D7 USING SIGNAL $\overline{\text{GB1ORD}}$. SIMILARLY THE GAME INTERFACE SENDS DATA TO THE ANALYZER BY LATCHING THE DATA INTO D8 WITH $\overline{\text{GB1OWRT}}$, AND THEN THE ANALYZER READS THE DATA WITH $\overline{\text{DS1ORD}}$. THIS DATA TRANSFER OPERATION IS MONITORED BY LATCH A6 WITH THE OUTPUTS DSGBEMP AND GBDSEMP, AND THE STATUS OF THESE TWO SIGNALS CAN BE READ BY THE ANALYZER PROCESSOR THRU BUFFER A2, OR BY THE GAME INTERFACE THRU BUFFER B7. HOWEVER, WHILE THE GAME INTERFACE MUST PERIODICALLY POLL B7 TO DETERMINE WHETHER TO SEND OR RECIEVE DATA, THE SIGNALS DSGBEMP OR GBDSEMP WHEN LOW CAUSES AN IRQ INTERUPT IN THE ANALYZER PROCESSOR. THE A6-7 OUTPUT $\overline{\text{DSGBMASK}}$

IS USED TO AVOID CAUSING AN IRQ INTERUPT WHEN DSGBEMP IS LOW, AS THE PROGRAM MAY NOT NEED TO BE REMINDED THAT IT WROTE TO THE OUTPUT LATCH D7. ALL OF THE INPUTS TO A6 ARE NORMALLY HIGH SIGNALS. WHEN $\overline{\text{MASK}}$ PULSES LOW $\overline{\text{DSGBMASK}}$ GOES LOW, AND WHEN $\overline{\text{UNMASK}}$ PULSES LOW $\overline{\text{DSGBMASK}}$ GOES HIGH. ON POWER UP OR MANUAL RESET $\overline{\text{SYSRST}}$ PULSES LOW WHICH CAUSES BOTH DSGBEMP AND GBDSEMP TO BE SET HIGH. THEN IF $\overline{\text{DSIOWRT}}$ PULSES LOW DSGBEMP GOES LOW, AND IF $\overline{\text{GBIOWRT}}$ PULSES LOW GBDSEMP GOES LOW. DSGBEMP IS RESET HIGH BY A LOW PULSE ON $\overline{\text{GBIORD}}$, AND GBDSEMP IS RESET HIGH BY A LOW PULSE ON $\overline{\text{DSIORD}}$. THEREFORE THE SIGNAL DSGBEMP WHEN LOW INDICATES NEW DATA IN LATCH D7 IS READY TO BE READ BY THE GAME INTERFACE AND WHEN HIGH MEANS THAT THE GAME INTERFACE HAS RECIEVED THE DATA. SIMILARLY THE SIGNAL GBDSEMP WHEN LOW MEANS THAT THE GAME INTERFACE HAS SENT DATA TO LATCH D8 AND WHEN HIGH SHOWS THAT THE DATA HAS BEEN READ BY THE ANALYZER PROCESSOR. IT SHOULD BE CLEAR THAT ANY NOISE ON THE INPUTS TO A6 MAY CAUSE THE OUTPUTS TO CHANGE AND COMMUNICATIONS

6. LOGIC ANALYZER SECTION

THE LOGIC ANALYZER HAS THE CAPACITY TO READ AND HOLD 256 GAME PROCESSOR INSTRUCTIONS OF 36 BITS EACH. THE 36 BITS INCLUDE 16 ADDRESS BITS (GBBAØ - GBBA 15), 8 LOW ORDER DATA BITS (GBBDØ - GBBD 7), 8 HIGH ORDER DATA BITS OR EXTERNALS (GBBD 8 - GBBD 15), THE GAME PROCESSOR SYNC LINE AND READ/WRITE LINE (GBSYNC, GBR/$\bar{W}$), AND TWO EXTERNALS (GBEXT1, GBEXT2). THE RAM USED TO STORE THESE SIGNALS ARE 9 2101's (E5, F5-F8, H5-H8), WHICH ARE 256 LOCATIONS BY 4 DATA BITS, GIVING THE SPACE OF 256 x 4 x 9 OR 256 x 36.

THE GAME PROCESSOR'S PHASE 2 CLOCK, GBΦ2, COMES TO THE LOGIC ANALYZER AT J1-20. IT GOES THRU TWO IN914 DIODES TO REDUCE NOISE AND THEN TO A 74LS14 GATE TO MAKE $\overline{\text{GBΦ2}}$. THE SIGNAL $\overline{\text{GBΦ2}}$ IS USED TO LATCH THE GAME'S LOWER 8 ADDRESS LINES INTO B8, WHICH HOLDS THIS INFORMATION FOR ONE GAME CLOCK CYCLE SO THAT IT CAN BE STORED IN THE ANALYZER "CAPTURE" RAM, F7 AND H7, AND COMPARED TO THE DESIRED TRIGGER ADDRESS. THE LOWER 8 BITS OF THE TRIGGER ADDRESS ARE LATCHED IN D11 AND ARE COMPARED TO THE GAME

ADDRESS BITS AT EXCLUSIVE OR'S B11 AND C11. ANY BITS THAT ARE THE SAME WILL MAKE THE OUTPUT OF THE CORRESPONDING 74LS86 GATE LOW. BITS THAT DON'T MATCH GIVE A HIGH OUTPUT. EACH OF THESE 8 COMPARE RESULTS ARE INDIVIDUALLY SELECTABLE AS TO WHETHER OR NOT THEY ARE IMPORTANT IN THE DESIRED TRIGGER ADDRESS. THE LOWER ADDRESS "MASK" IS LATCHED IN D12. (NOTE: THE CURRENT ANALYZER ONLY ALLOWS THE LATCHING INTO D12 AND/OR D11 WHILE THE LOGIC ANALYZER IS STOPPED ie NOT WAITING FOR A TRIGGER TO HAPPEN). THE OUTPUTS OF D12 EACH GO TO ONE INPUT ON THE BANK OF NAND GATES AT B12 AND C12 WHILE THE ADDRESS BIT COMPARE RESULTS EACH GO TO THE OTHER INPUT. IF THE COMPARE INPUT IS LOW, MEANING THE ADDRESS BIT MATCHES THE TRIGGER ADDRESS BIT, OR IF THE MASK BIT IS LOW, MEANING THAT THIS COMPARE ISN'T IMPORTANT TO THE TRIGGER, THEN THE NAND GATE'S OUTPUT WILL BE HIGH. IF BOTH INPUTS ARE HIGH, MEANING THE BITS DON'T MATCH AND ARE IMPORTANT, THEN THE NAND GATE'S OUTPUT WILL BE LOW. IF ALL OF THE 8 NAND GATE'S OUTPUTS

ARE HIGH THEN THEIR NANDING AT GATE B15 WILL CAUSE THE SIGNAL $\overline{\text{UQADLTR}}$ TO GO LOW. THIS OUTPUT, B15-8, DRIVES A LONG TRACE ON THE PCB AND IS SUSEPTIBLE TO NOISE. A 75 pF FROM B15-8 TO GND WILL QUIET THIS SIGNAL DOWN SO THAT IT WON'T CAUSE PROBLEMS. THIS APPLIES ALSO TO OUTPUTS C15-8, A3-8, AND A5-8. ALL THESE OUTPUTS, (PLUS $\overline{\text{UQEXTTR}}$), WHEN LOW WILL CAUSE THE SIGNAL "MATCH" TO GO HIGH WHICH MEANS THAT THE DESIRED TRIGGER ADDRESS AND DATA WAS JUST ENCOUNTERED. THE OUTPUTS $\overline{\text{UQADHTR}}$, $\overline{\text{DLOWEQ}}$, $\overline{\text{UQDTR}}$, AND $\overline{\text{UQEXTTR}}$ EACH COME FROM CIRCUITS EXACTLY THE SAME AS THE JUST DESCRIBED CIRCUITRY FOR $\overline{\text{UQADLTR}}$. THE SIGNAL $\overline{\text{UQDTR}}$ IS SPECIAL THOUGH, BECAUSE LATCH J4 CAN CHANGE THE MEANING OF $\overline{\text{UQDTR}}$. IF J4-9 IS HIGH THEN IF $\overline{\text{UQDTR}}$ IS LOW IT MEANS ALL 16 DATA BITS MATCH THE DESIRED TRIGGER DATA. IF J4-9 IS LOW THEN IF $\overline{\text{UQDTR}}$ IS LOW IT MEANS THE GAME DATA BITS DON'T MATCH THE TRIGGER DATA. THIS IS USEFUL FOR THE "DATA NOT EQUAL" TRIGGER MODE.

THE SIGNAL $\overline{\text{CAPQUAL}}$ COMES FROM THE EXTERNAL TRIGGER CIRCUITRY OUT OF

GATE A12 IN A SIMILAR MANNER TO ALL THE OTHER TRIGGER SIGNALS, BUT IT IS USED TO TURN OFF OR INHIBIT THE SPECIAL CLOCKING THAT STORES DATA INTO THE CAPTURE RAMS AND ADVANCES THE LOGIC ANALYZER'S CONTROL REGISTERS. THIS IS USEFUL FOR STORING AND READING ONLY TRIGGERED GAME PROCESSOR INSTRUCTIONS, OR ONLY READS, ONLY WRITES, OR ONLY OPCODES, OR ANY COMBINATION, AND GBEXT1 INPUT CAN BE USED TOO.

THE INVERTED GAME PHASE 2 CLOCK, $\overline{GB\Phi 2}$ IS PUT THRU ANOTHER INVERTER TO MAKE GBΦ2, AND THEN THRU A SERIES OF 3 INVERTERS AND 2 RC DELAYS FOR A TOTAL DELAY OF ABOUT 150 ns TO MAKE $\overline{GB\Phi 2DLY}$. BOTH GBΦ2 AND $\overline{GB\Phi 2DLY}$ ARE USED IN THE ANALYZER CONTROL CIRCUITRY.

ANALYZER SINGLE-SHOT MODE:

THE ANALYZER PROCESSOR STARTS THE ANALYZER LOOKING FOR A TRIGGER BY PULSING THE SIGNAL $\overline{LASTART}$. THIS SETS LATCH J1 AND SO, ON $\overline{GB\Phi 2}$, SETS THE OTHER LATCH J1, WHICH CAUSES THE FIRST LATCH TO BE CLEARED. THE SECOND LATCH AND $\overline{GB\Phi 2}$ MAKES $\overline{LARESET}$ GO LOW. $\overline{LARESET}$ CAUSES TRIGEN TO GO HIGH.

TRIGEN AND MATCH (FROM THE TRIGGER SIGNALS) AND THE CLOCK MADE FROM AN OR OF GB$2DLY AND GB$2SQUASH ALL BEING HIGH MAKES QTRIG GO HIGH, WHICH SIGNALS THE CONTROL CIRCUITRY THAT A TRIGGER IS HAPPENING. LARESET ALSO SETS LATCH J4 MAKING CAPRAMEN LOW, WHICH ALONG WITH CAPQUAL ENABLES THE CLOCK, CAPRAMCK, THAT LOADS DATA INTO THE CAPTURE RAMS. CAPRAMEN ALSO ENABLES THE CAPTURE RAM ADDRESS COUNTERS, F3 AND H3, TO CYCLE THROUGH THE 256 ADDRESSES, WHILE LARESET CLEARS THE PRE-TRIGGER DATA COUNTERS, B2 AND C2, THE DATAVALID LATCH, F1, AND THE TRCONT LATCH, L11.

NOW THE LOGIC ANALYZER IS RUNNING. THE CAPTURE RAM ADDRESS COUNTERS COUNT UP TO 256, FF, THEN GO TO Ø AND COUNT TO 256, ETC. THE OUTPUTS OF F3 AND H3 GO THRU MULTIPLEXERS F4 AND H4 TO THE CAPTURE RAM ADDRESS BUSS, AND THE SIGNAL CAPRAMCK WRITES THE GAME INSTRUCTIONS DATA INTO THE ADDRESS COUNTER SPECIFIED LOCATION OF THE CAPTURE RAMS. THIS PROCESS CONTINUES WITHOUT INTERUPTION CYCLE BY CYCLE, EXCEPT IF THE SELECTIVE TRIGGER SIGNAL CAPQUAL GOES HIGH. WHILE CAPQUAL IS HIGH, QUALCLK IS DISABLED HALTING THE ADDRESS COUNTERS,

AND $\overline{\text{CAPRAMCK}}$ IS DISABLED SO NO DATA IS LOADED INTO THE CAPTURE RAMS. WHEN $\overline{\text{CAPQUAL}}$ IS LOW THE PROCESS CONTINUES. AT THE SAME TIME $\overline{\text{QUALCLK}}$ IS ADVANCING THE PRE-TRIGGER DATA COUNTERS, B2 AND C2. WHEN B2-7 GOES HIGH THE CAPTURE RAMS HAVE STORED 128 GAME INSTRUCTIONS SO THRU MULTIPLEXER E3 THE PRE-TRIGGER DATA COUNTERS ARE DISABLED SINCE 128 IS THE MOST INSTRUCTIONS THAT WILL BE SAVED BEFORE THE TRIGGER. THE REAL USEFULNESS OF THIS PRE-TRIGGER CIRCUIT IS FOR THE CASES WHEN A TRIGGER IS ENCOUNTERED BEFORE THE COUNT OF 128 HAS BEEN REACHED. WHEN A TRIGGER HAPPENS QTRIG GOES HIGH AND WITH $\overline{\text{GBL2DLY}}$ THRU E1 MAKES $\overline{\text{DATACNTLD}}$ GO LOW. $\overline{\text{DATACNTLD}}$ GOES THRU MULTIPLEXER E3 AND GATE K10 TO LATCH INTO D2 THE PRESENT COUNT OF THE PRE-TRIGGER DATA COUNTERS. THE VALUE LATCHED IN D2 WILL BE READ BY THE ANALYZER PROCESSOR SO IT READS ONLY THAT MANY LOCATIONS BEFORE THE TRIGGER LOCATION IN THE CAPTURE RAMS WHEN THE DATA IS DISPLAYED FOR THE USER. IF THE PROCESSOR WERE TO INDESCRIMINATELY READ ALL 128 RAM LOCATIONS BEFORE THE TRIGGER, THEN SOME OR ALL (WHEN TRIGGERING ON ANY INSTRUCTION) OF THE DATA

WOULD BE IRRELEVANT TO THE TRIGGERED INFORMATION. IF THE LOGIC ANALYZER PARAMETERS CALL FOR MORE THAN ONE TRIGGER, THEN $\overline{\text{DATACNTLD}}$ WILL LATCH IN THE PRE-TRIGGER COUNT ON EACH TRIGGER, WHILE THE COUNTER CONTINUES UP TO 128. THE VALUE IN D2 IS THEN THE NUMBER, UP TO A MAXIMUM OF 128, OF VALID DATA LOCATIONS BEFORE THE LAST TRIGGER IN THE CAPTURE RAM.

THE NUMBER OF TRIGGERS DESIRED IS LOADED INTO THE TRIGGER COUNTERS D1 AND E2, BEFORE STARTING THE LOGIC ANALYZER, USING THE DECODE SIGNAL $\overline{\text{TRIGCNT}}$. EVERYTIME A TRIGGER IS ENCOUNTERED QTRIG WILL GO HIGH CLOCKING THE TRIGGER COUNTERS DOWN ONE. WHEN THE COUNT REACHES Ø AND THE QTRIG SIGNAL GOES BACK LOW, THE RIP OUTPUT OF D1 GOES LOW CAUSING TRIGUP TO GO HIGH.

TRIGUP GOING HIGH MEANS THE LAST DESIRED TRIGGER WAS ENCOUNTERED AND SO CLOCKS LATCH H2, WHICH CAUSES THE SIGNAL TRIGEN TO GO LOW. A LOW ON TRIGEN DISABLES QTRIG AT GATE K2 KEEPING ANY FURTHER TRIGGER DETECTION FROM AFFECTING THE LOGIC ANALYZER CONTROL CIRCUITRY.

A LOW ON TRIGEN ALSO ENABLES THE

THE POST-TRIGGER DATA COUNTERS, B1 AND C1. THESE WERE PREVIOUSLY SET TO A COUNT OF 127, 7F, BY THE SIGNAL $\overline{\text{DATACNTLD}}$ ON THE FIRST ENCOUNTERED TRIGGER. THE POST-TRIGGER DATA COUNTERS NOW COUNT DOWN CLOCKED BY $\overline{\text{QUALCLK}}$ COUNTING 127 DESIRED POST-TRIGGER INSTRUCTIONS AS THEY ARE STORED INTO THE CAPTURE RAM. WHEN THE COUNTERS B1 AND C1 REACH Ø BOTH OF THEIR M/M OUTPUTS GO HIGH AND SO THRU H1 THE SIGNAL DATACNTEND GOES HIGH.

TRIGUP IS HIGH AND NOW WITH DATACNTEND HIGH THRU H1 A HIGH IS LATCHED INTO F1 BY $\overline{\text{GBΦ2DLY}}$. THIS BRINGS THE SIGNAL ENDTRIGS HIGH, WHICH SETS THE DATAVALID LATCH INDICATING THAT A TRIGGER AND TRACE OPERATION BY THE LOGIC ANALYZER IS COMPLETE. ON THE RISING EDGE OF ENDTRIGS THRU GATE K8 LATCH J4 IS CLEARED BRINGING $\overline{\text{CAPRAMEN}}$ HIGH, WHICH DISABLES THE SIGNAL, $\overline{\text{CAPRAMCK}}$, THAT WRITES DATA INTO THE CAPTURE RAM.

A LOGIC ANALYZER OPERATION CAN BE STOPPED AT ANY TIME BY THE ANALYZER PROCESSOR USING THE SIGNAL $\overline{\text{LASTOP}}$. $\overline{\text{LASTOP}}$ SETS LATCH J2. THE OTHER LATCH J2 IS THEN SET BY $\overline{\text{GBΦ2}}$, WHICH WHILE HIGH

IS NANDED WITH THE Q OUTPUT OF THE SECOND J2 LATCH. THIS CLEARS THE FIRST J2 LATCH AND THRU GATE J3 CLEARS LATCH J4 CAUSING $\overline{\text{CAPRAMEN}}$ TO GO HIGH, WHICH DISABLES $\overline{\text{CAPRAMCK}}$ FROM WRITING TO THE CAPTURE RAM.

WHEN A VALID TRIGGER IS ENCOUNTERED, MIDWAY THROUGH AN INSTRUCTION CYCLE WHEN GBCL2 GOES HIGH WHILE QTRIG IS HIGH, THE SIGNAL TRACK GOES HIGH. THIS CAUSES CHIP E4 TO LATCH THE CAPTURE RAM ADDRESS LOCATION AS THE TRIGGERED GAME INSTRUCTION IS BEING LOADED INTO THE CAPTURE RAM, LATCH E4 WHEN ENABLED BY THE ANALYZER PROCESSOR USING $\overline{\text{TALRD}}$ WILL PUT ON THE ANALYZER'S BUFFERED DATA BUSS THE ACTUAL ADDRESS IN THE CAPTURE RAM WHERE THE LAST TRIGGER'S DATA IS STORED. THE SIGNAL TRACK ALSO SETS THE TRCONT LATCH, L11, WHICH MAKES TRCONT GO HIGH INDICATING THAT A TRIGGER HAS BEEN ENCOUNTERED.

IF THE ANALYZER PROCESSOR STROBES SIGNAL $\overline{\text{STATRD}}$ IT CAN READ THRU BUFFER A2 THE STATUS OF 4 OF THE LOGIC ANALYZER'S SIGNALS : TRCONT, TRIGUP, CAPRAMEN, AND DATAVALID. THESE SIGNALS WHEN HIGH HAVE THE FOLLOWING MEANINGS. TRCONT

MEANS A TRIGGER WAS ENCOUNTERED. TRIGUP MEANS THE LAST OF THE DESIRED NUMBER OF TRIGGERS WAS ENCOUNTERED. CAPRAMEN MEANS A TRIGGER AND TRACE OPERATION IS IN PROCESS, DATAVALID MEANS THE LOGIC ANALYZER IS HALTED AND ITS OPERATION FINISHED. ALSO THRU A2 COMES THE STATE OF THE TTL COMPATIBLE 60 Hz SIGNAL AND THE SIGNAL PERR, WHICH WHEN HIGH INDICATES THE ANALYZER'S PROGRAM RAM HAS FAILED.

THE LOGIC ANALYZER CAN BE OPERATED IN A CONTINUOUS MODE, IN WHICH IT WILL NOT HALT ITSELF AND WILL TRIGGER AND TRACE INDEFINITELY. THE PREVIOUS DESCRIPTION WAS FOR THE ONE-SHOT MODE AND THE SIGNAL CONTMOD WAS LOW AND $\overline{\text{CONTMOD}}$ WAS HIGH. IN CONTINUOUS MODE CONTMOD IS HIGH AND $\overline{\text{CONTMOD}}$ IS LOW. THESE TWO SIGNALS IN CONTINUOUS MODE ALTER THE OPERATION OF THE LOGIC ANALYZER CONTROL CIRCUITRY SO THAT IT DIVIDES THE 256 CAPTURE RAM LOCATIONS IN HALF. ONE HALF OF THE CAPTURE RAM HOLDS UP TO 64 VALID GAME INSTRUCTIONS BEFORE THE PREVIOUSLY ENCOUNTERED TRIGGER, THE INSTRUCTION OF THE PREVIOUSLY ENCOUNTERED TRIGGER, AND THE 63

VALID INSTRUCTIONS AFTER THE PREVIOUSLY ENCOUNTERED TRIGGER. THE OTHER HALF IS BEING USED TO STORE THE GAME PROCESSOR'S CURRENT INSTRUCTIONS BEFORE THE TRIGGER AND WILL STORE THE TRIGGERED INSTRUCTION AND 63 INSTRUCTIONS FOLLOWING THE TRIGGER. AFTER A TRIGGER IS ENCOUNTERED AND 63 VALID POST-TRIGGER INSTRUCTIONS ARE STORED, THEN THE LATTER HALF OF THE CAPTURE RAM BECOMES THE FORMER HALF AND THE FORMER HALF IS AVAILABLE FOR A NEW TRIGGER AND TRACE OPERATION. THIS "LEAP-FROG" OPERATION WILL CONTINUE UNTIL THE LOGIC ANALYZER IS HALTED BY THE ANALYZER PROCESSOR. THE ACTUAL OPERATION OF THE LOGIC ANALYZER CONTROL CIRCUIT'S COUNTERS AND LATCHES IN THE CONTINVOUS MODE IS AN EXERCISE LEFT TO THE READER.

SYNC

RAS, CAS, $\overline{\text{LATCH}}$

PROCESSOR

DECODE

ACIA

PROGRAM ROM

PROGRAM RAM

PARITY CHECK

ANALYZER

DATA LATCH RAM

TRIGGER DECODE

CONTROL

COUNTERS

REGISTERS

GAME $\Leftrightarrow$ ANALYZER COMMUNICATION

GAME COMMUNICATION

STATUS SIGNALS AVAILABLE TO AND CONTROLED BY BOTH GAME & L.A.

ANALYZER SECTION

DATA CAPTURE RAM 256 x 36 WILL HOLD 256 INSTRUCTIONS OF

16 ADDRESS BITS

16 DATA BITS (8 DATA, 8 EXTERNAL)

4 EXTERNAL BITS

2 OPTIONAL

1 GAME PROCESSOR SYNC

1 GAME PROCESSOR R/$\bar{W}$

TRIGGER DECODE

EACH OF THE 36 BITS SELECTABLE AS CARE / DON'T CARE

EACH OF THE 36 BITS EXCLUSIVE ORED TO 36 BIT COMPARE REGISTER

← START AND STOP CIRCUITRY ARMS OR DISARMS ANALYZER

← COUNTERS:

CAPTURE RAM ADDRESS

TRIGGER

POST TRIGGER WORDS

PRE TRIGGER VALID WORDS

L.A. SYNC

$\overline{1.25\ MHz}$ FOR PROCESSOR Φ∅
IF — 64F FOR DYNAMIC RAM REFRESH
$\overline{RAS}$, $\overline{CAS}$, & RADSEL FOR ADDRESSING
OF DYNAMIC RAM
$\overline{LATCH}$ SPECIALLY DECODED SYNC SIGNAL
FOR THE PRE-TRIGGER VALID DATA
COUNTER LATCH (ANALYZER SECTION)

PROCESSOR

6502A RUNNING AT 1.25 MHz
STANDARD WATCHDOG RESET CIRCUIT
NMI's AT 16.7 ms INTERVAL, HARD
IRQ's FOR COMMUNICATION

DECODE

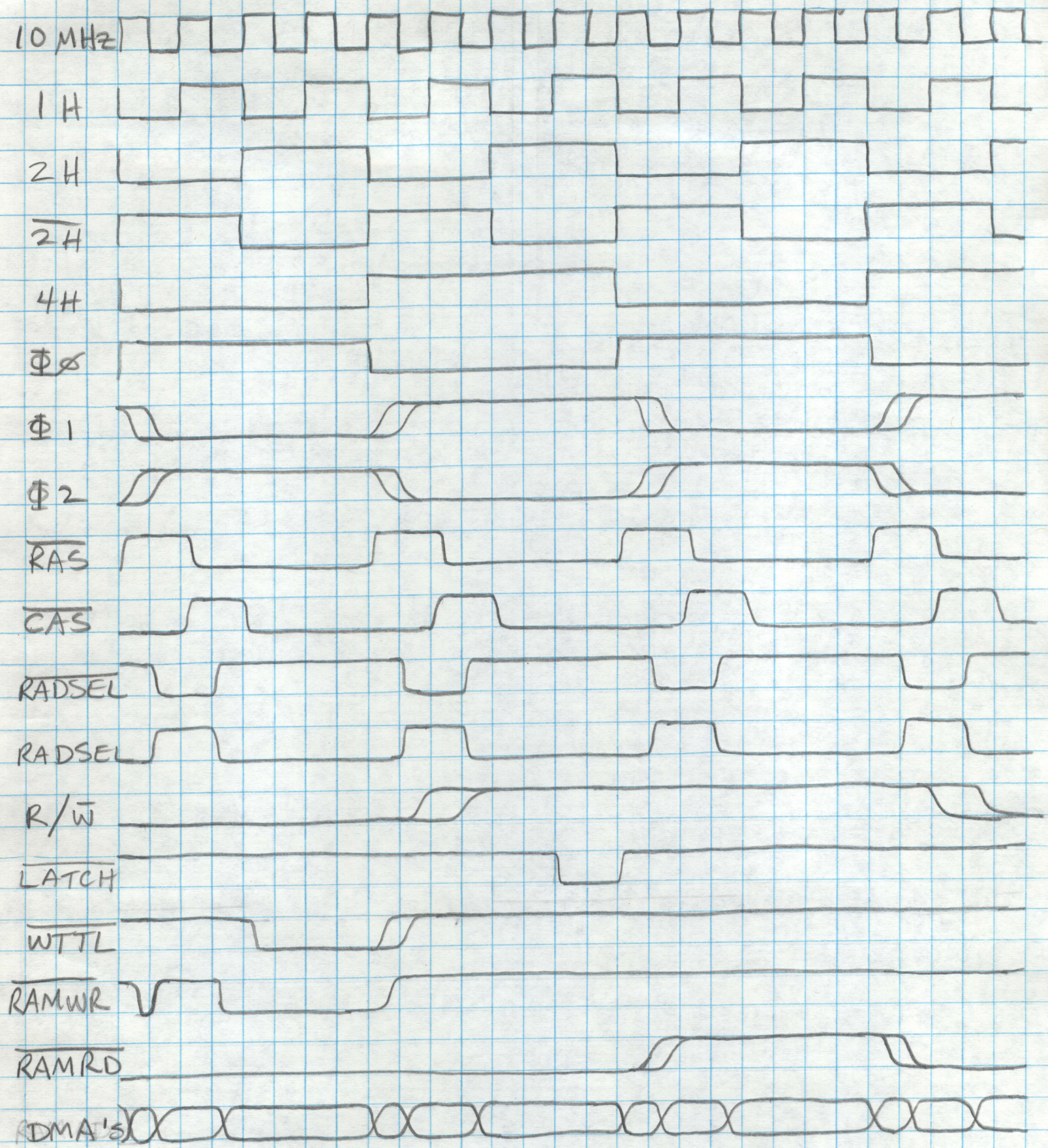
CLEAN WRITE SIGNALS USING $\overline{WTTL}$
READ SIGNALS NOT CLEAN

ACIA

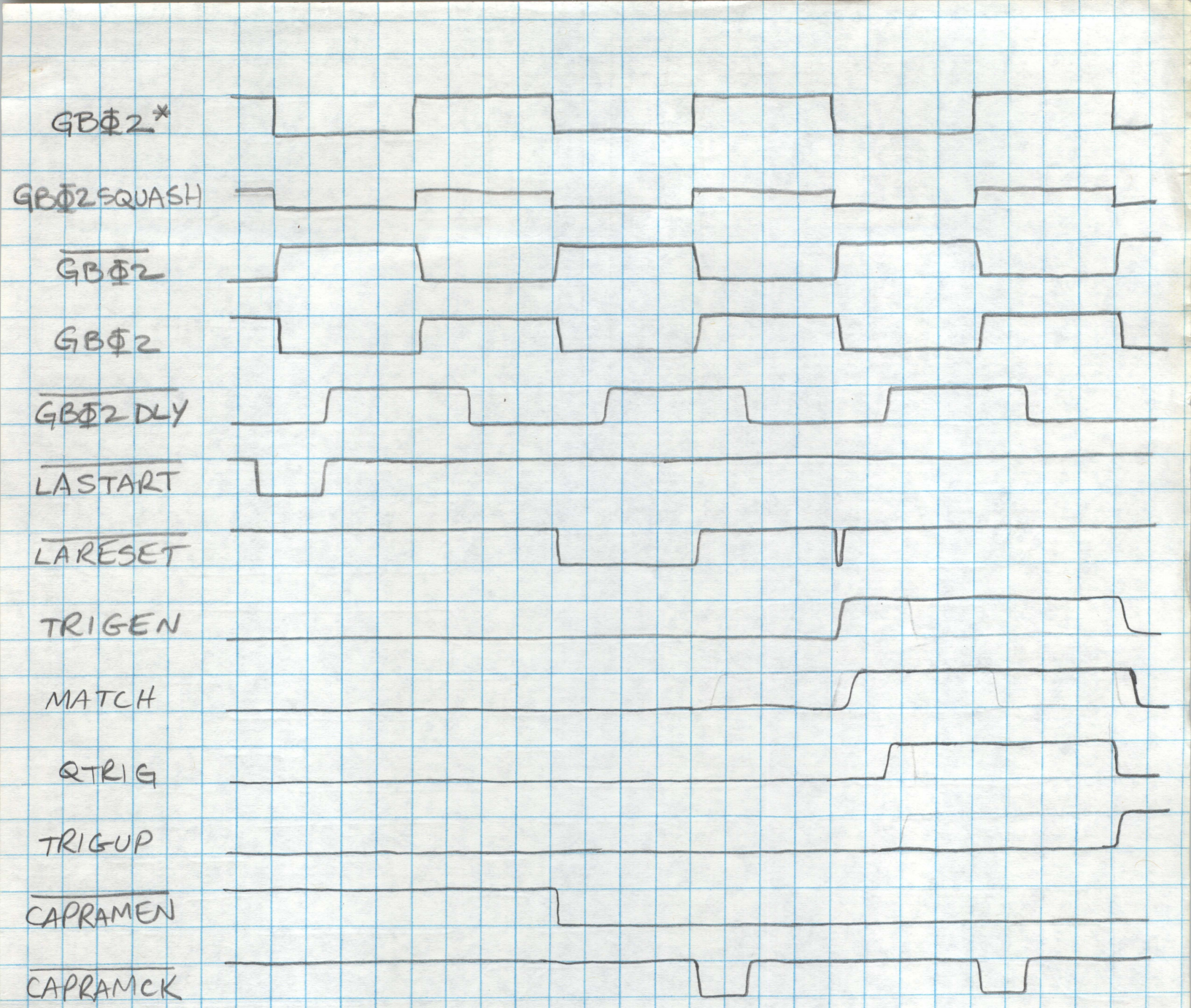
STANDARD. CIRCUIT USING 68B50

PROGRAM ROM 8K, 4K PRESENTLY USED

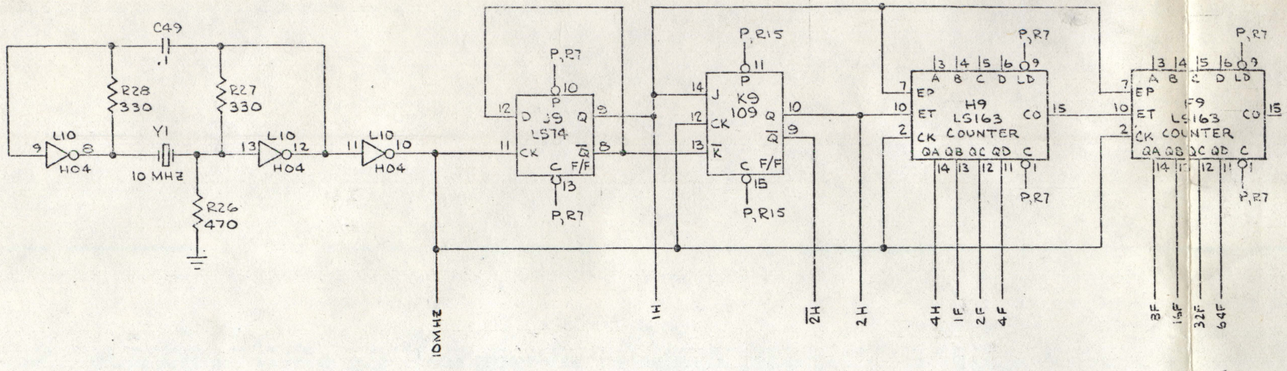
PROGRAM RAM 16K DYNAMIC WITH PARITY CHECK

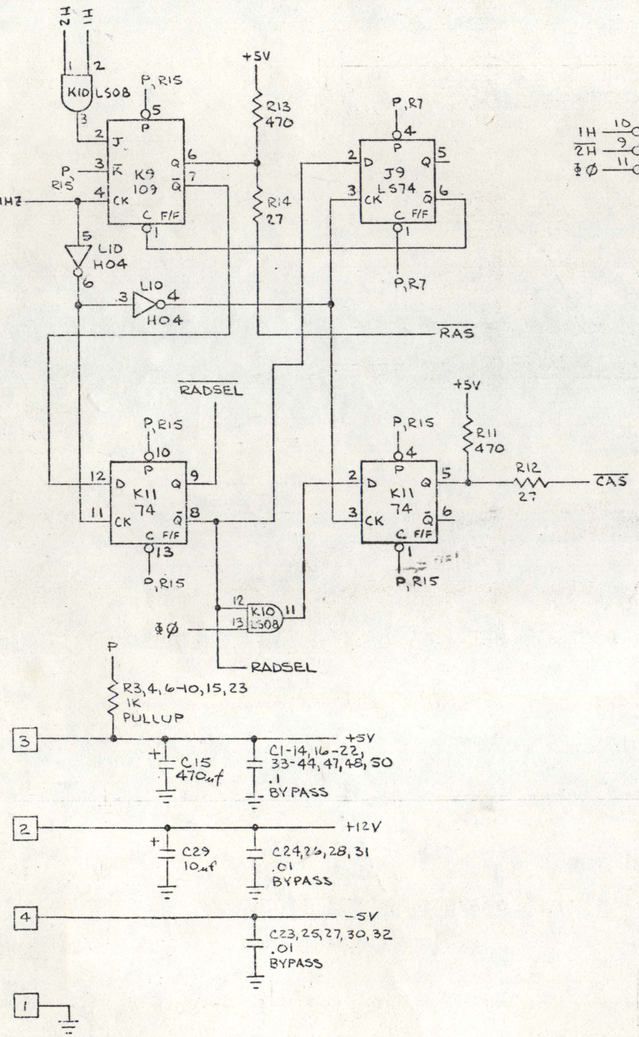


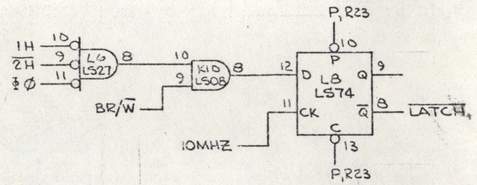
ANALYZER PROGRAM TIMING


GBΦ2*
GBΦ2SQUASH
GBΦ2
GBΦ2
GBΦ2 DLY
LASTART
LARESET
TRIGEN
MATCH
QTRIG
TRIGUP
CAPRAMEN
CAPRAMCK

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
1	PROTOTYPE RELEASE 1/5		
2	UPDATE 8-7-79		







MEMORY MAP

ADDRESS HEXIDECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-3FFF	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	W	D	D	D	D	D	D	D	D	WORKING RAM (16K BYTES)
9000	1	0	0	1	X	X	X	X	X	X	X	X	0	0	0	0	W	D	D	D	D	D	D	D	D	LOW ADDRESS BYTE MASK
9001	1	0	0	1	X	X	X	X	X	X	X	X	0	0	0	1	W	D	D	D	D	D	D	D	D	LOW ADDRESS BYTE COMPARE
9002	1	0	0	1	X	X	X	X	X	X	X	X	0	0	1	0	W	D	D	D	D	D	D	D	D	HIGH ADDRESS BYTE MASK
9003	1	0	0	1	X	X	X	X	X	X	X	X	0	0	1	1	W	D	D	D	D	D	D	D	D	HIGH ADDRESS BYTE COMPARE
9004	1	0	0	1	X	X	X	X	X	X	X	X	0	1	0	0	W	D	D	D	D	D	D	D	D	LOW DATA BYTE MASK
9005	1	0	0	1	X	X	X	X	X	X	X	X	0	1	0	1	W	D	D	D	D	D	D	D	D	LOW DATA BYTE COMPARE
9006	1	0	0	1	X	X	X	X	X	X	X	X	0	1	1	0	W	D	D	D	D	D	D	D	D	HIGH DATA BYTE MASK
9007	1	0	0	1	X	X	X	X	X	X	X	X	0	1	1	1	W	D	D	D	D	D	D	D	D	HIGH DATA BYTE COMPARE
9008	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	0	W	X	X	X	X	X	X	X	X	SYNC TRACE ENABLE
9008	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	0	W	D	D	D	D	D	D	D	X	R/W TRACE ENABLE
9008	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	0	W	X	X	X	X	X	X	X	X	TRIGGER TRACE ENABLE
9008	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	0	W	X	X	X	D	X	X	X	X	EXTERNAL 1 TRACE ENABLE
9008	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	0	W	X	X	X	X	D	X	X	X	EXTERNAL 2 TRACE ENABLE
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	1	W	X	X	X	X	X	X	X	X	SYNC MASK
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	1	W	X	X	X	X	X	D	X	X	R/W MASK
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	1	W	X	X	X	X	X	X	D	X	EXTERNAL 2 MASK
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	0	0	1	W	X	X	X	X	X	X	X	D	EXTERNAL 1 MASK
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	0	1	0	W	X	X	X	X	X	X	X	X	SYNC COMPARE
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	0	1	1	W	X	X	X	X	X	D	X	X	R/W COMPARE
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	1	0	0	W	X	X	X	X	D	X	X	X	EXTERNAL 2 COMPARE
9009	1	0	0	1	X	X	X	X	X	X	X	X	1	1	0	1	W	X	X	X	D	X	X	X	X	EXTERNAL 1 COMPARE
900A	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	0	W	X	X	X	X	X	X	X	X	SPARE
900B	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	W	X	X	X	X	X	X	X	X	SPARE
900C	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	W	D	D	D	D	D	D	D	D	TIMER RESET
900D	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	W	D	D	D	D	D	D	D	D	TRIGGER COUNT LOAD
900E	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	W	X	X	X	X	X	X	D	X	LA CONT BIT 1: TRIG ON DATA 2; 0: TRIG ON DATA 1
900F	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	W	X	X	X	X	X	X	X	D	LA CONT BIT 1: COUNT MODE, 0: ONE SHOT MODE
900F	1	0	0	1	X	X	X	X	X	X	X	X	1	1	1	1	W	D	D	D	D	D	D	D	D	DEVELOPMENT SYSTEM I/O DATA WRITE
A000-A0FF	1	0	1	0	0	0	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	LOW BYTE ADDRESS CAPTURE RAM
A100-A1FF	1	0	1	0	0	0	1	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	HIGH BYTE ADDRESS CAPTURE RAM
A200-A2FF	1	0	1	0	0	1	0	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	LOW BYTE DATA CAPTURE RAM
A300-A3FF	1	0	1	0	0	1	1	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	HIGH BYTE DATA CAPTURE RAM
A400-A4FF	1	0	1	0	1	0	0	A	A	A	A	A	A	A	A	A	R	X	X	X	X	D	D	D	D	EXTERNAL DATA CAPTURE RAM D7: SYNC, D6: R/W, D5: EXTERNAL 2, D4: EXTERNAL 1
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	D	Y	Y	Y	Y	Y	Y	Y	STATUS READ D5: SSDSTMP
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	U	Y	Y	Y	Y	Y	Y	Y	GSDSTMP
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	D	Y	Y	Y	Y	Y	Y	X	LOGIC ANALYZER DATA VALID
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	D	X	X	X	X	X	X	X	CAPTURE RAM WRITE ENABLE
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	X	Y	Y	Y	Y	Y	Y	X	TRIGGER ENCOUNTER FLAG
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	X	X	X	X	X	X	X	X	SPARE
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	X	X	X	X	X	X	D	Y	50 MS
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	0	R	X	Y	Y	Y	Y	Y	Y	D	PARITY ERROR
A000	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	1	W	X	X	X	X	X	X	X	X	GAME PROCESSOR RESET SIGNAL LATCH
A001	1	0	1	0	1	X	0	X	0	X	0	X	0	X	0	1	W	X	X	X	X	X	X	X	X	DSSTMP SIGNAL UNMASK
A002	1	0	1	0	1	X	0	X	0	X	0	X	0	X	1	0	W	X	X	X	X	X	X	X	X	NMI SIGNAL TO GAME BOARD
A003	1	0	1	0	1	X	0	X	0	X	0	X	0	X	1	1	W	X	X	X	X	X	X	X	X	DSSSTMP SIGNAL MASK
C000	1	1	0	0	0	X	X	X	X	X	X	X	X	X	0	0	W	X	X	X	X	X	X	X	X	LOGIC ANALYZER START
C001	1	1	0	0	0	X	X	X	X	X	X	X	X	X	0	1	W	X	X	X	X	X	X	X	X	LOGIC ANALYZER STOP
C002	1	1	0	0	0	X	X	X	X	X	X	X	X	X	1	0	W	X	X	X	X	X	X	X	X	PARITY ERROR FLAG RESET
C003	1	1	0	0	0	X	X	X	X	X	X	X	X	X	1	1	W	X	X	X	X	X	X	X	X	WATCHDOG RESET
D000	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	0	R	D	D	D	D	D	D	D	D	ACIA STATUS REGISTER
D000	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	0	W	D	D	D	D	D	D	D	D	ACIA CONTROL REGISTER
D001	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	1	R	D	D	D	D	D	D	D	D	ACIA RX DATA REGISTER
D001	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	1	W	D	D	D	D	D	D	D	D	ACIA TX DATA REGISTER
8000-8FFF	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	PROGRAM MEMORY SPACE (32K)
E001	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	TRIGGERED ADDRESS POINTER
E002	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	R	D	D	D	D	D	D	D	D	TRIGGERED VALID COUNT
E003	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	R	D	D	D	D	D	D	D	D	DEVELOPMENT SYSTEM I/O DATA READ
E000	1	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	R	D	D	D	D	D	D	D	D	CAPTURE RAM ADDRESS COUNTER

PRELIMINARY

OUTSTANDING ECNs	

SYNC

A034221	SFTNR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES ±1°
SURFACE FINISH ✓ .X ± .1 .XX ± .03 .XXX ± .005

DO NOT SCALE DRAWING
DRAWN BY DATE
CHECKED
ENGINEER
PROJECT ENGINEER
MFG ENGINEER

MATERIAL:
FINISH:

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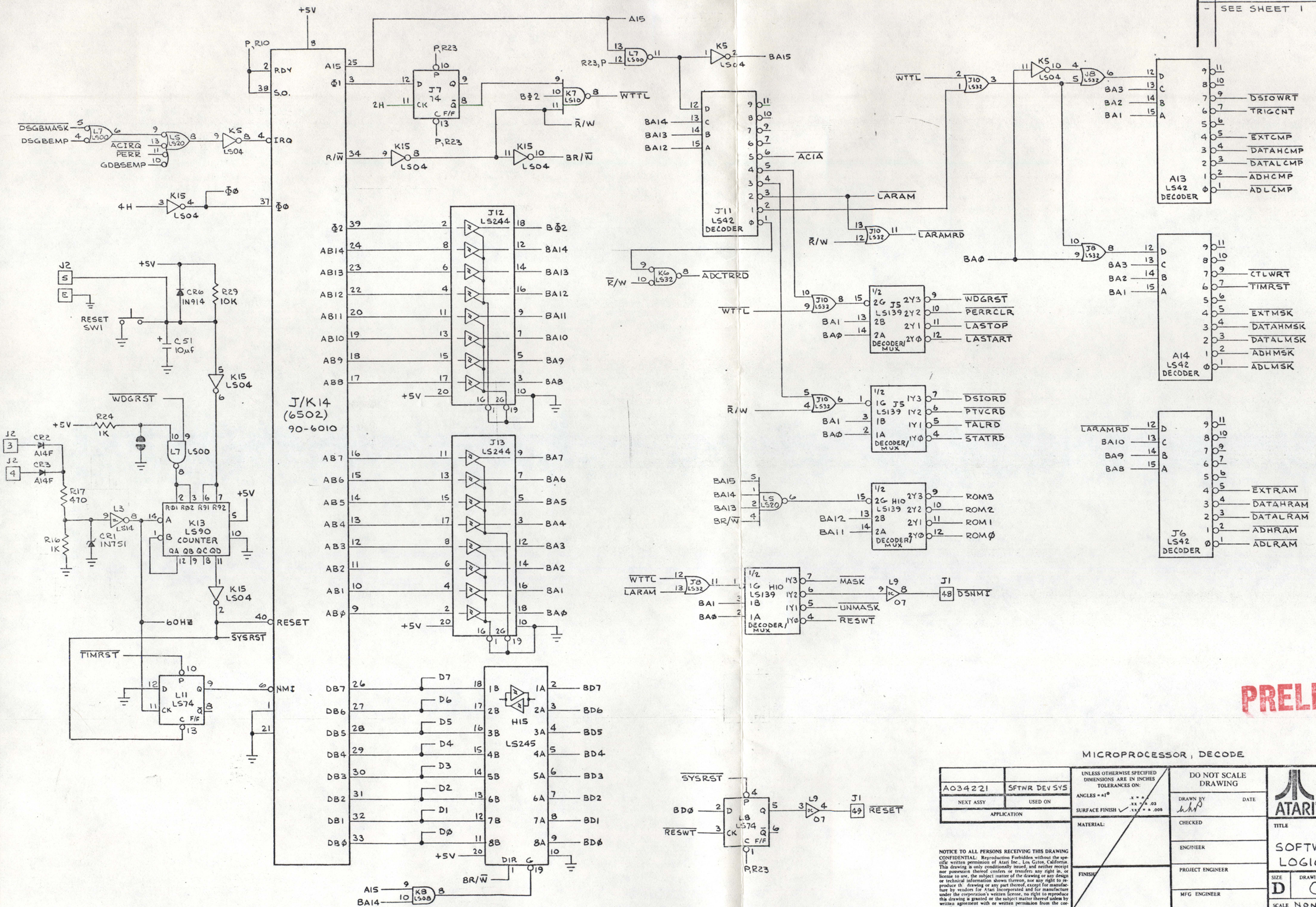
Sunnyvale, Calif. 94086
A Warner Communications Company

TITLE SCHEMATIC, SOFTWARE DEV. SYS., LOGIC ANALYZER P.C.BD

SIZE	DRAWING NO.	REV
D	034221-01	2

SCALE NONE SHEET 1 OF 7

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
-	SEE SHEET 1		



PRELIMINARY

OUTSTANDING ECNs	

MICROPROCESSOR, DECODE

A034221	SFTWR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES = ±1°
SURFACE FINISH
MATERIAL:
FINISH

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ENGINEER
PROJECT ENGINEER
MFG ENGINEER

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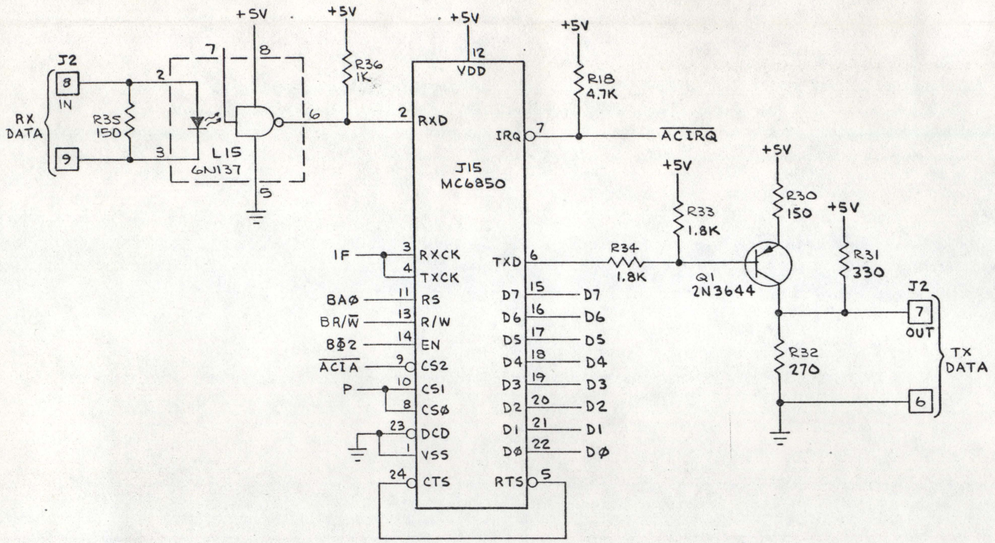
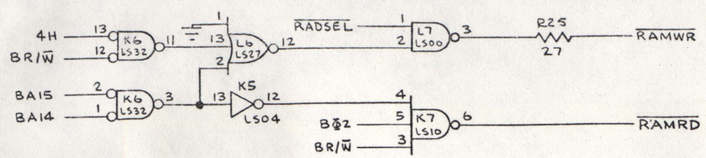
SIZE	DRAWING NO.	REV
D	034221-01	2

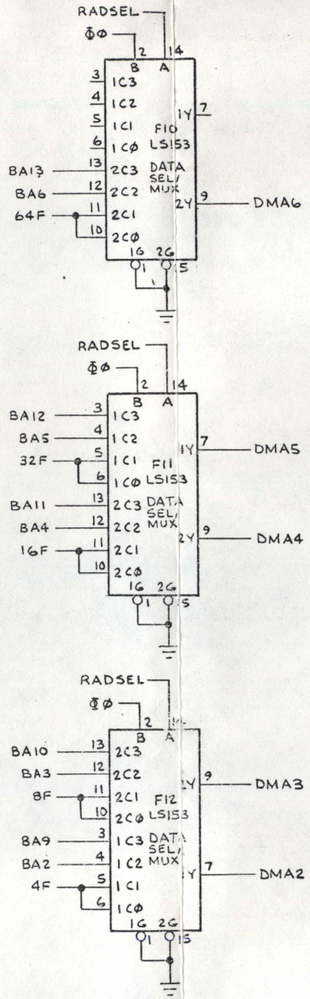
SCALE NONE SHEET 2 OF 7

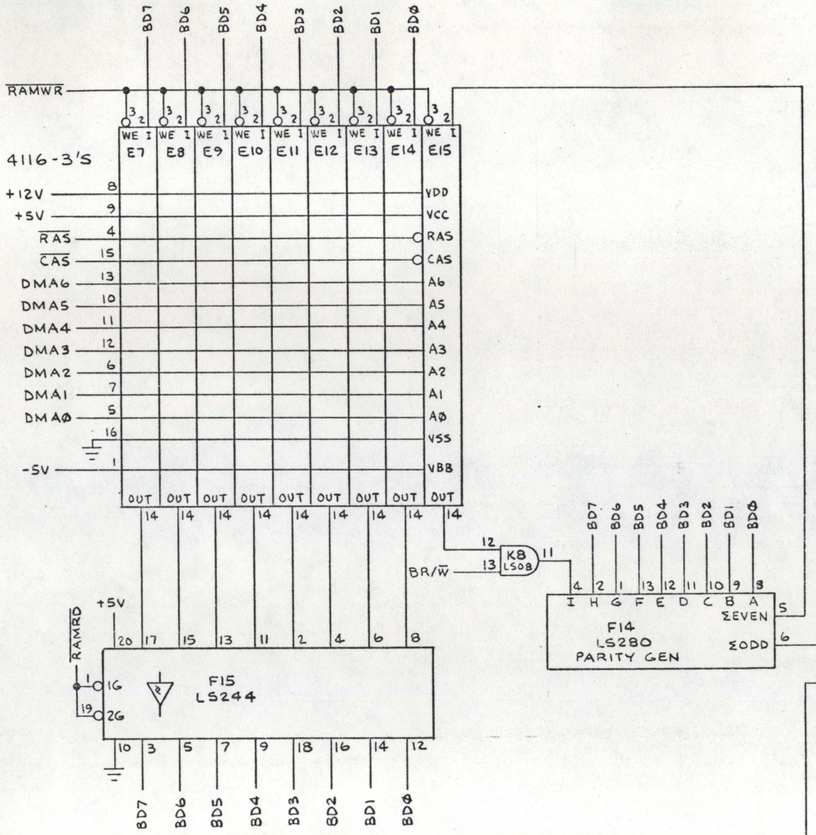
DRAWING NO. | SHEET | REV

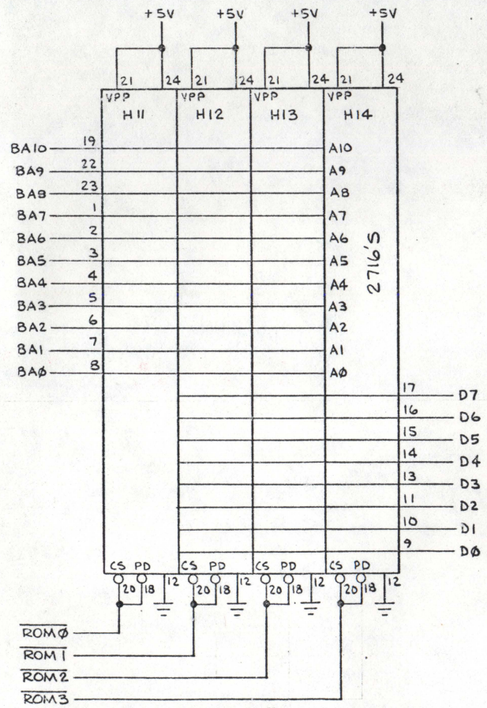
SYM	REVISIONS DESCRIPTION	DATE	APPROVED
-	SEE SHEET 1		











PRELIMINARY

MEMORIES (PROG, MUXED RAM)

OUTSTANDING ECNs	

A034221	SFTWR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES = ±1°
SURFACE FINISH
MATERIAL:
FINISH:

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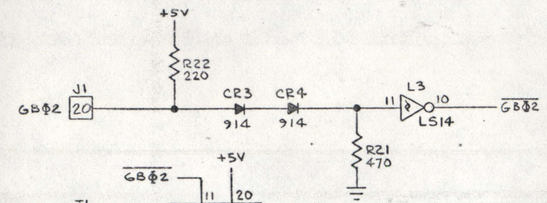
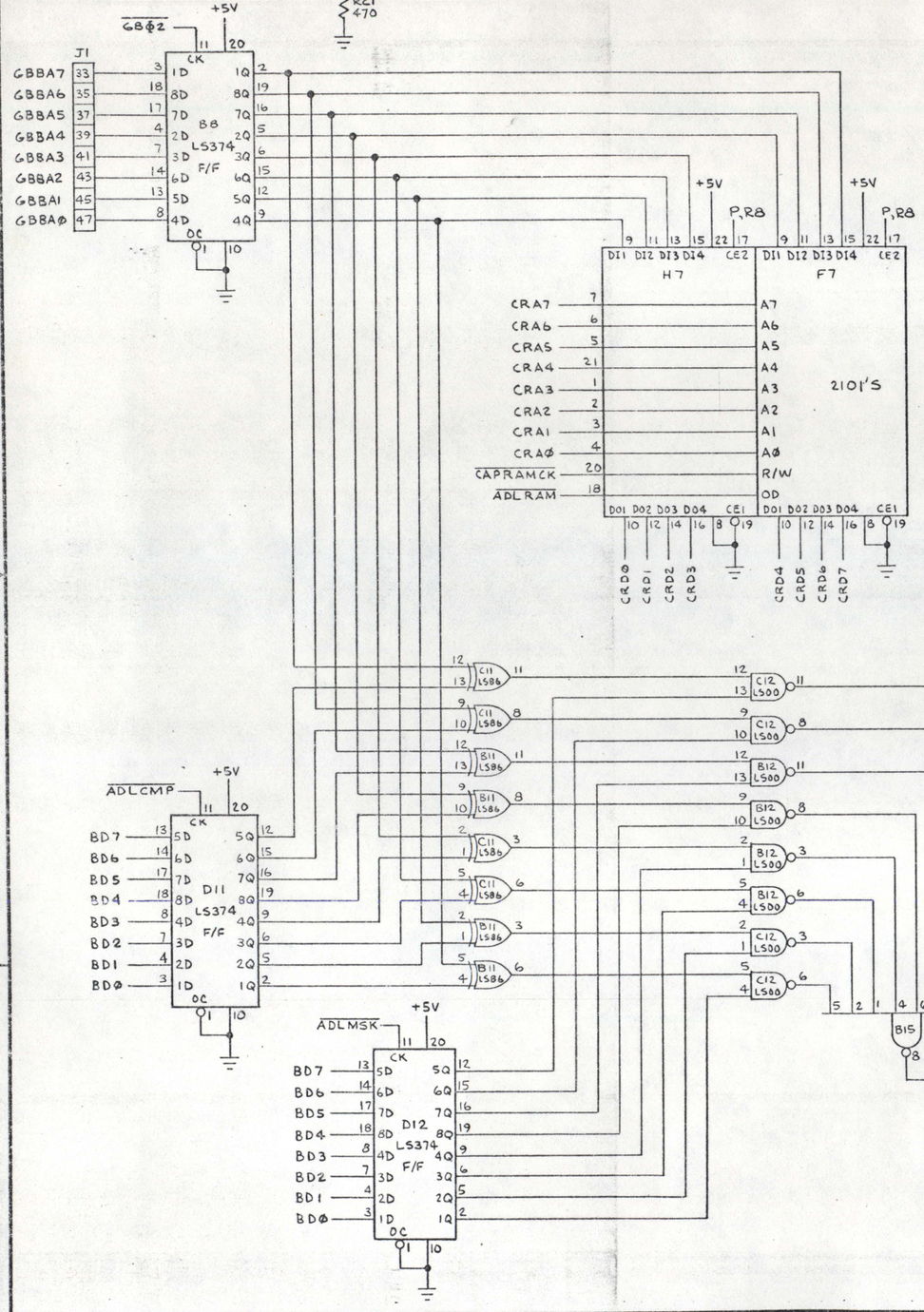
SIZE	DRAWING NO.	REV
D	034221-01	2

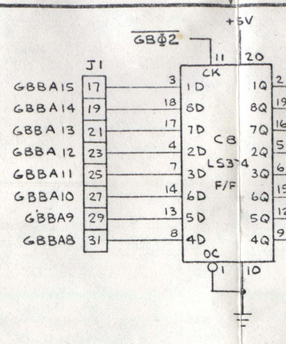
SCALE NONE SHEET 3 OF 7

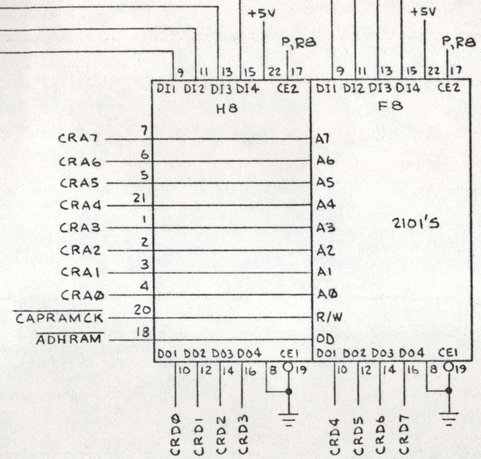
DRAWING NO.
SHEET
REV

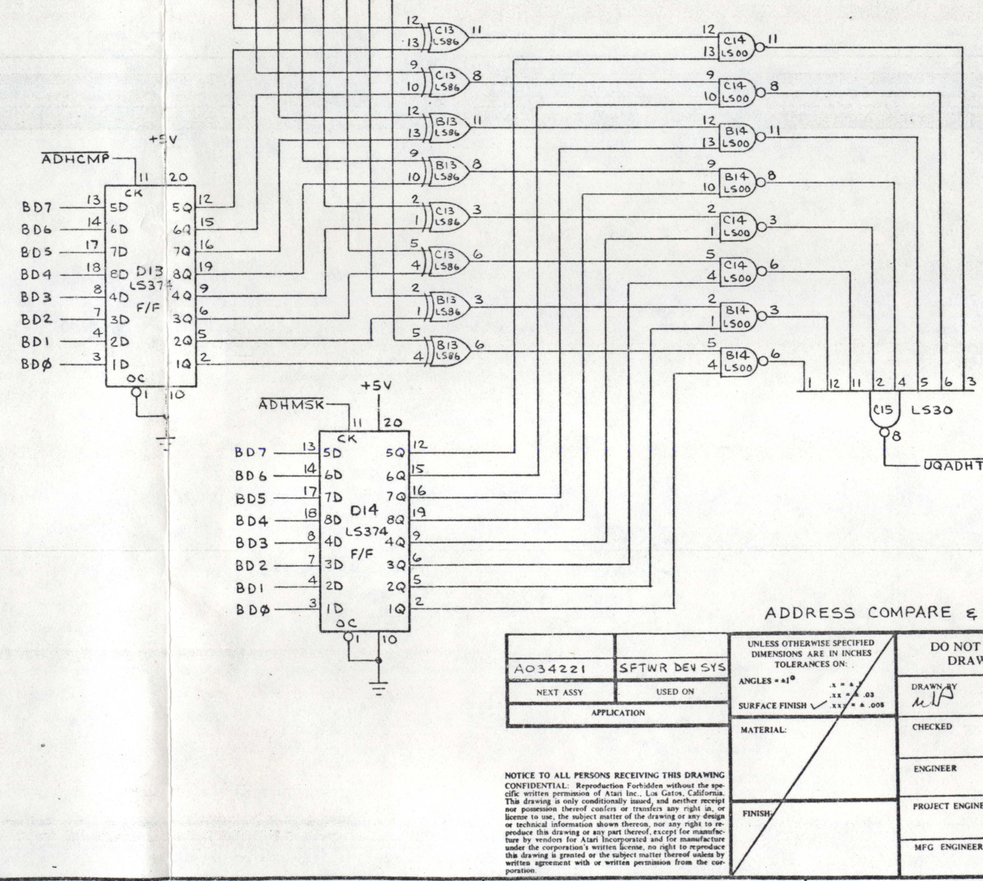
SYM	REVISIONS DESCRIPTION	DATE	APPROVED
-	SEE SHEET 1		











PRELIMINARY

ADDRESS COMPARE & RAM

OUTSTANDING ECNs	

A034221	SFTWR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES ± 1°
SURFACE FINISH
.X ± .1
.XX ± .03
.XXX ± .005
MATERIAL:
FINISH:

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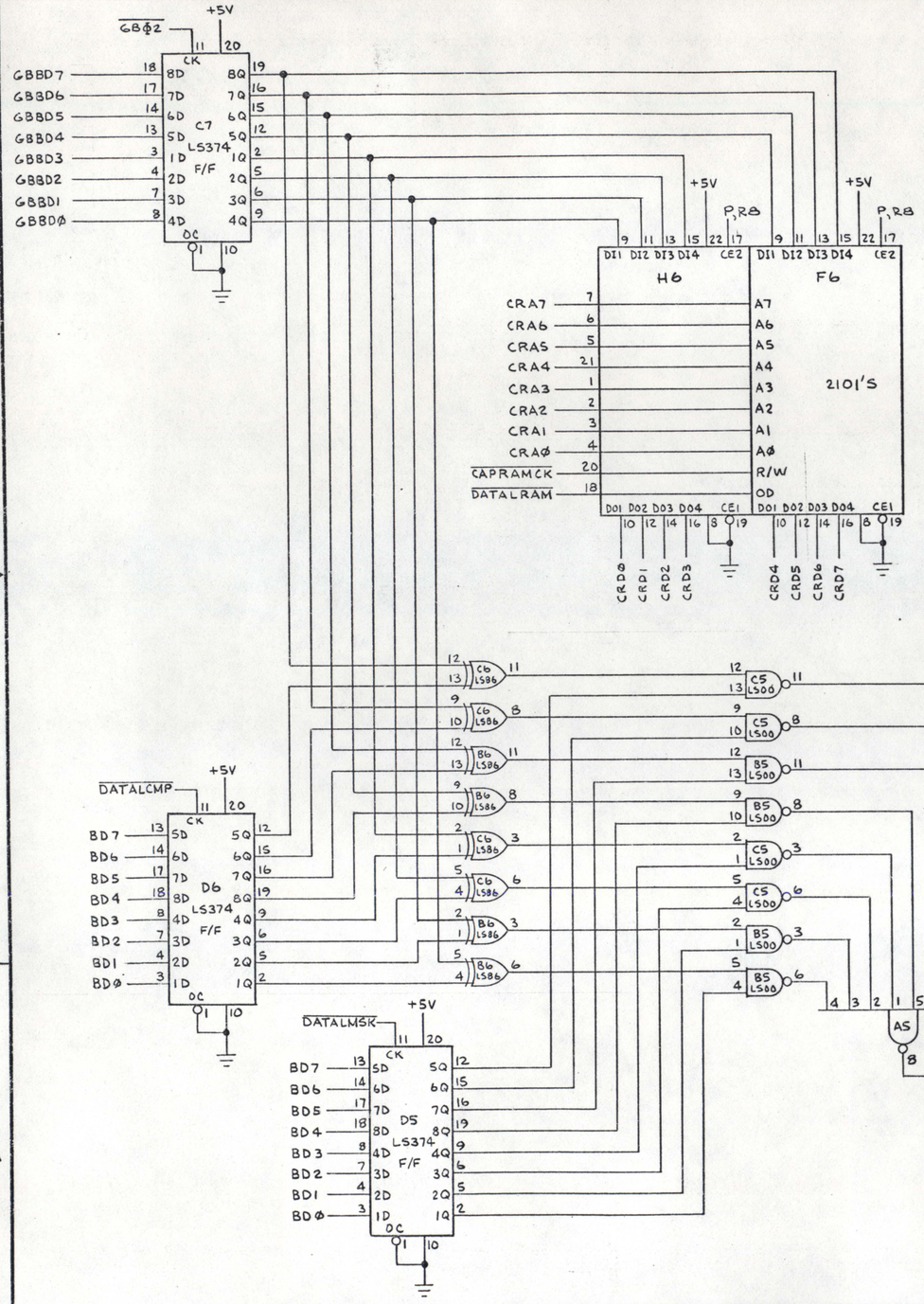
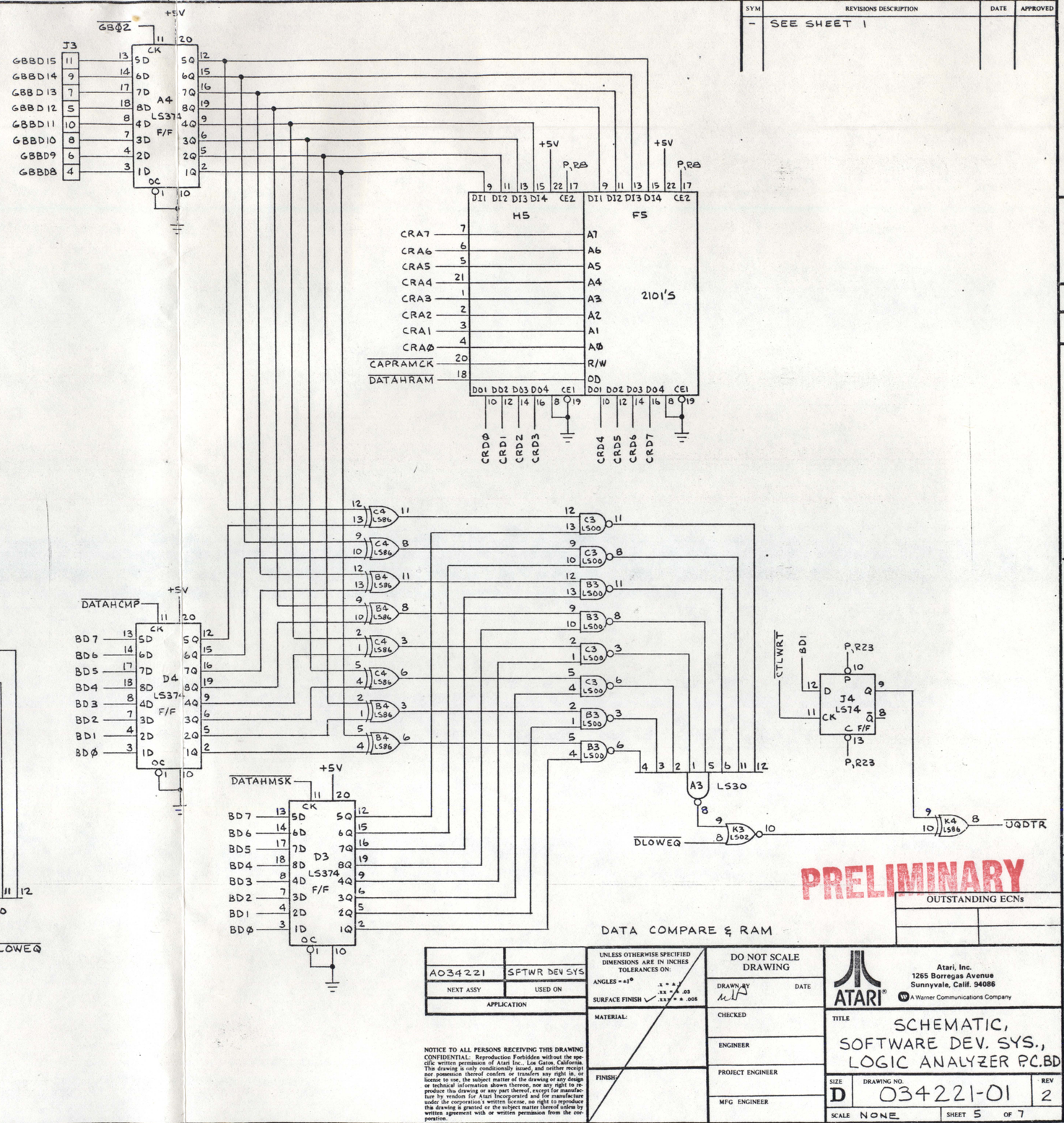
SIZE	DRAWING NO.	REV
D	034221-01	2

SCALE NONE SHEET 4 OF 7

DRAWING NO. | SHEET | REV

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
-	SEE SHEET 1		





PRELIMINARY

OUTSTANDING ECNs	

DATA COMPARE & RAM

A034221	SFTWR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES = ±1°
SURFACE FINISH
.X = ± .1
.XX = ± .03
.XXX = ± .005
MATERIAL:
FINISH:

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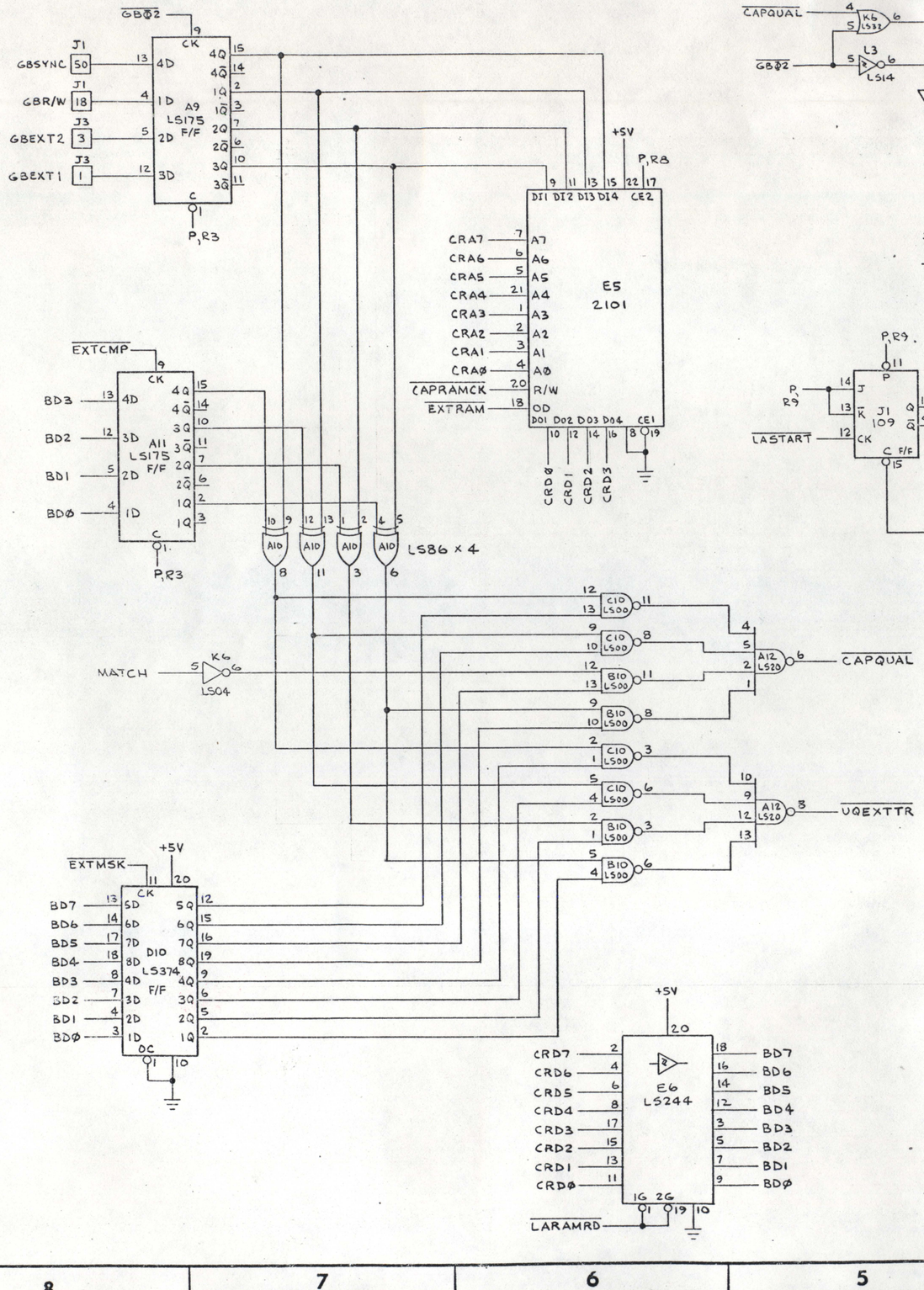
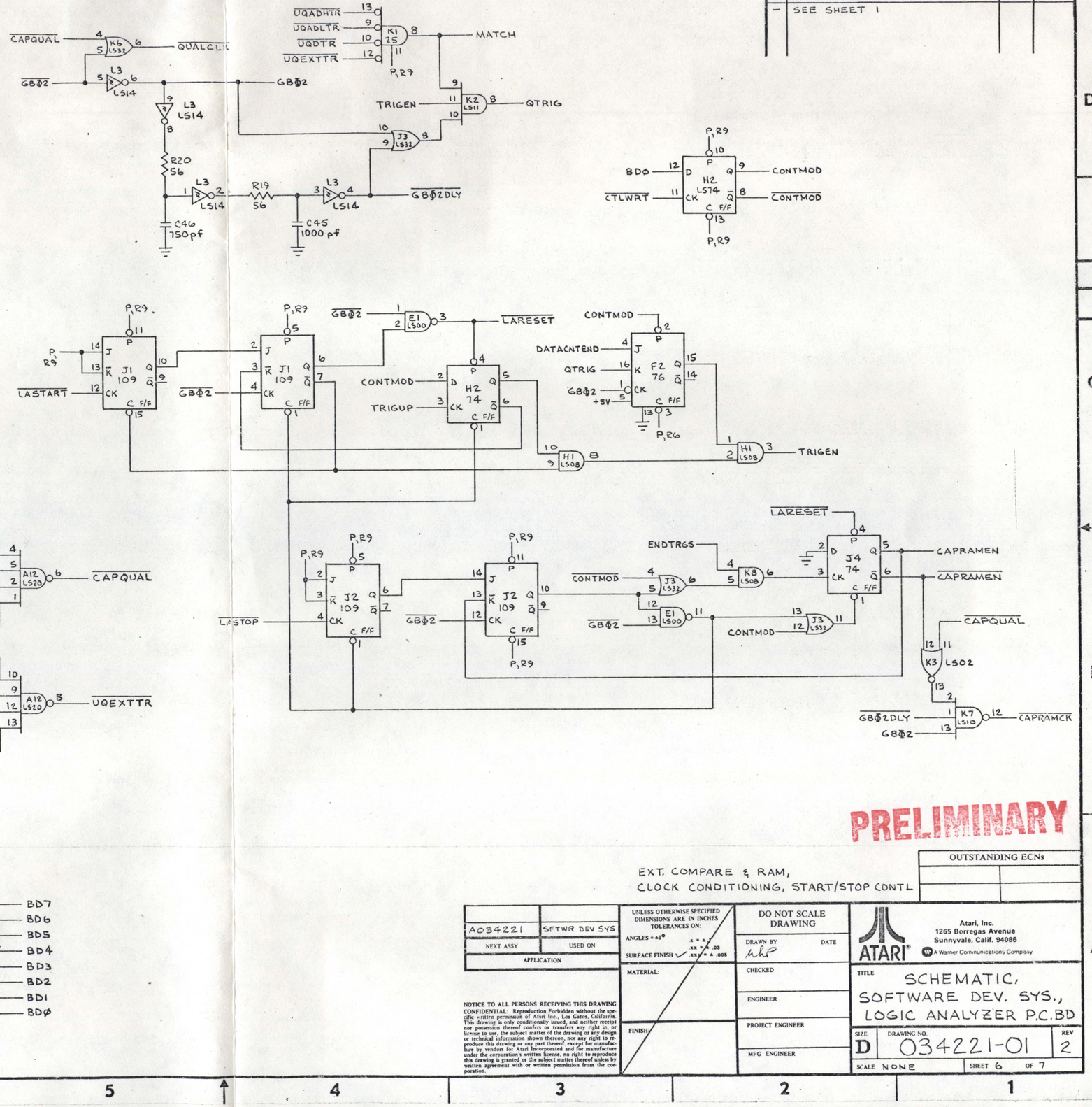
SIZE	DRAWING NO.	REV
D	034221-01	2

SCALE NONE | SHEET 5 OF 7

DRAWING NO. | SHEET | REV

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
–	SEE SHEET 1		





PRELIMINARY

EXT. COMPARE & RAM,
CLOCK CONDITIONING, START/STOP CONTL

OUTSTANDING ECNs	

A034221	SFTWR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES = ±1°
.X = ± .1
.XX = ± .03
.XXX = ± .005
SURFACE FINISH ✓
MATERIAL:
FINISH:

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PROJECT ENGINEER
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SIZE	DRAWING NO.	REV
D	034221-01	2

SCALE NONE SHEET 6 OF 7

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
--	SEE SHEET 1		

QTRIG, GBBSDLY, E1 LS00, DATACNTLD

TRIGEN, DATACNTEND, J3 LS32, P

TRIGUP, LATCH, PTVCRD, L6 LS27

CONTMOD, K5 LS04, K10 LS08

QTRIG, DATACNTLD, E3 LS157 MUX

P,R6

BD0, BD1, BD2, BD3, E2 LS191 COUNTER M/M RIP, C1 LS191 COUNTER

DATACNTLD, QUALCLK

TRIGCNT, QTRIG, PR4

BD4, BD5, BD6, BD7, D1 LS191 COUNTER

CONTMOD, C2 LS191 COUNTER, B1 LS191 COUNTER, B2 LS191 COUNTER

PRCNTLD, QUALCLK

TRIGUP, DATACNTEND, H1 LS08

CONTMOD, E1 LS00, TRIGUP

PTVCRD, D2 LS374 F/F

+5V, R2 560, R1 560

DSIOWRT, GBIORD 46, SYSRST, GBIORD, MASK, UNMASK, GBIOWRT 42, SYSRST, DSIORD

A6 279 S-R LATCH

DSGBEMP, DSGBMASK, GBDSEMP

GBBD7, GBBD6, GBBD5, GBBD4, GBBD3, GBBD2, GBBD1, GBBD0

GBIOWRT, DSIORD, D8 LS374 F/F

BD0, BD1, BD2, BD3, BD4, BD5, BD6, BD7

J1: 1 GBBD7, 3 GBBD6, 5 GBBD5, 7 GBBD4, 9 GBBD3, 11 GBBD2, 13 GBBD1, 15 GBBD0

DSIOWRT, D7 LS374 F/F, GBIORD

ENDTRGS

P,R6, F1 74 F/F, GBBSDLY

P,R6, F1 74 F/F, DATAVALID

LARESET

ADCQ7, ADCQ6, ADCQ5, ADCQ4, ADCQ3, ADCQ2, ADCQ1, ADCQ0, A1 LS244, BD7, BD6, BD5, BD4, BD3, BD2, BD1, BD0

ADCTRRD

P,R6, P,R6, F2 76 F/F

CONTMOD, TRIGEN, LARESET, ADCQ7, E3 LS157 MUX, PRCNTLD

LARAMRD, BA7, ADCQ6, BA6, ADCQ5, BA5, ADCQ4, BA4, F4 LS157 DATA SEL/MUX, CRA7, CRA6, CRA5, CRA4

QTRIG, GBBSQ2, K8 LS08

P,R6, CAPRAMEN, H3 LS191 COUNTER, ADCQ0, ADCQ1, ADCQ2, ADCQ3

QUALCLK, F3 LS191 COUNTER, ADCQ4, ADCQ5, ADCQ6, ADCQ7

+5V, ADCQ6, ADCQ5, ADCQ4, ADCQ3, ADCQ2, ADCQ1, ADCQ0, E4 LS374 F/F, BD7, BD6, BD5, BD4, BD3, BD2, BD1, BD0, TALRD

LARAMRD, ADCQ3, BA3, ADCQ2, BA2, ADCQ1, BA1, ADCQ0, BA0, H4 LS157 DATA SEL/MUX, CRA3, CRA2, CRA1, CRA0

+5V, R5 560, GBSTRD 44

DSGBEMP, GBDSEMP, B7 8T97, GBBD7, GBBD6

+5V, DSGBEMP, GBDSEMP, DATAVALID, CAPRAMEN, TRIGUP, 60HZ, PERR, A2 LS244, BD7, BD6, BD5, BD4, BD3, BD1, BD0, STATRD

PRELIMINARY

OUTSTANDING ECNs

TRIGGER COUNTERS, GAME BOARD IO

A034221	SFTWR DEV SYS
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES ± 1°
X ± .1
XX ± .03
XXX ± .005
SURFACE FINISH
MATERIAL:
FINISH:

DO NOT SCALE DRAWING

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SIZE D | DRAWING NO. 034221-01 | REV 2

SCALE NONE | SHEET 7 OF 7