National Semiconductor

MM5280 4096-Bit (4096 x 1) Dynamic RAM

General Description

National's MM5280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

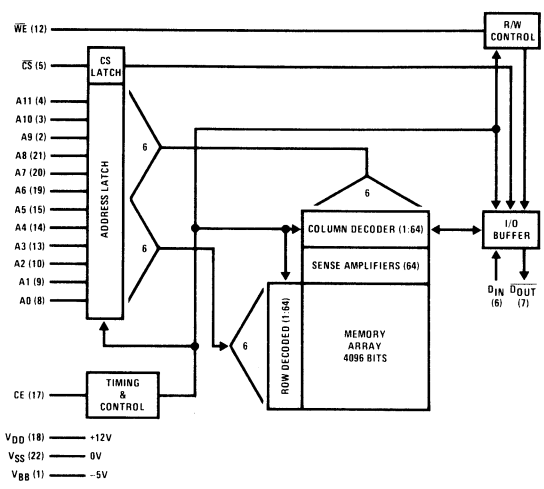
The MM5280 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

Features

- Organization: 4096 x 1
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

Block Diagram



Memory Inverts From Data In to Data Out

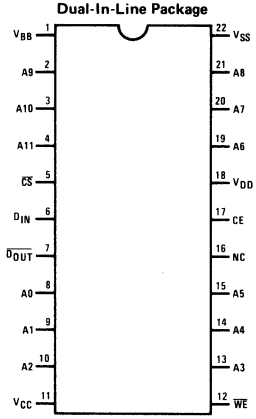
Pin Names

A0–A11	Address Inputs *	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

* Refresh Address A0–A5

Connection Diagram

Dual-In-Line Package

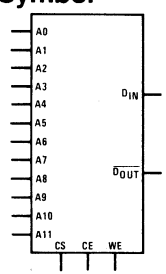


TOP VIEW

Order Number MM5280N
See NS Package N22A

Order Number MM5280J
See NS Package J22A

Logic Symbol



Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Operating Conditions

	MIN	MAX	UNITS
Operating Temperature Range	0	+70	°C
V_{DD} Voltage	10.8	13.2	V
V_{CC} Voltage	4.5	5.5	V
V_{BB} Voltage	−5.5	−4.5	V

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} (Note 2) = −5V ±10%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	40	mA
$I_{DD\,AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
$I_{DD\,AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

AC Electrical Characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$			180	ns
t_{ACC}	Address to Output Access				200	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

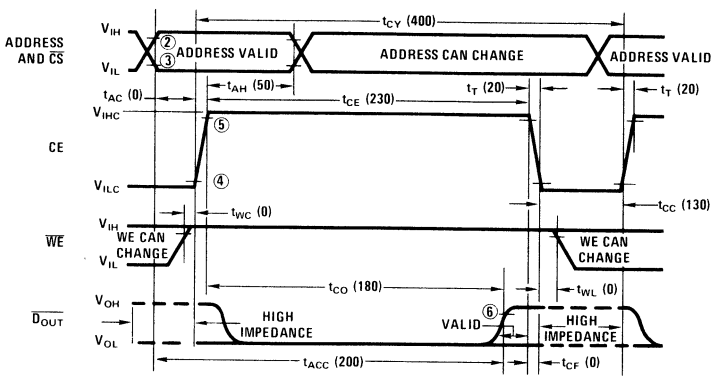
AC Electrical Characteristics (Continued)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5\% \pm 10\%$

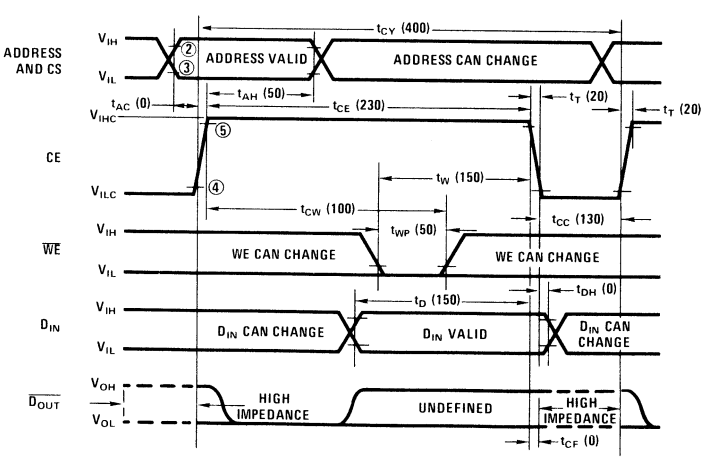
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	100			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

Switching Time Waveforms

Read and Refresh Cycle①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

AC Electrical Characteristics (Continued)

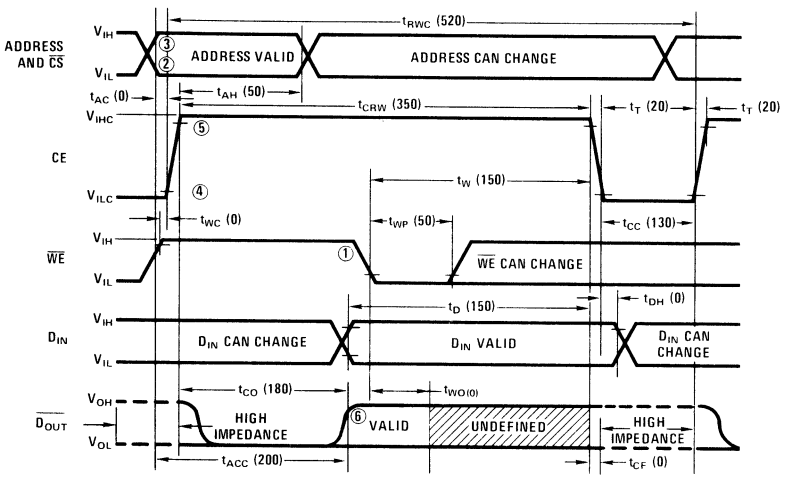
$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5\% \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	520			ns
t_{CRW}	CE Width During RMW		350		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				200	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

Switching Time Waveforms (Continued)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.