ON TARGET
Gottlieb
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# POWER DISTRIBUTION, VIDEO

Power distribution for the GG-III Video System is associated with two separate assemblies: (1) The Bottom Panel Assembly and (2) The Power Supply Assembly (A3). The Power Supply, used to supply all voltages, is extremely tolerable to input line voltage variations. All output source voltages are guaranteed to be stable for line voltages varying from 95V AC to 135V AC 60HZ. The regulated logic +5V DC level is rated at 6 amps maximum and includes over-voltage crowbar protection. Four LED's on the Power Supply indicate that the associated voltages to the regulators are present.

## BOTTOM PANEL ASSY.

The input AC line voltage is filtered and wired to the 115V AC primary winding tap and the common tap of the transformer on the Bottom Panel. The secondary winding supplies five separate voltages. The isolated 115V AC supplies the monitor voltage as well as the Illumination Assembly voltage.

The 9V AC RMS winding is full wave rectified and filtered to +11.5V DC average voltage. It is directly routed to the Power Supply via the Filter Board. The 6.3V AC RMS fused winding is also rectified and supplies the +4.5V DC average voltage. The negative side of the bridge is sent to the Power Supply Board for grounding while both the positive and the negative sides of the bridge are sent to the front door to operate the coin chute lights. The 15V AC as well as the 35V AC are both routed directly to the Power Supply via the Filter Board.

## POWER SUPPLY ASSY. (A3)

The +11.5V DC entering the Power Supply Board is regulated to +5V DC by Q11, Q12 and U11 and is adjustable by VR1. R15 and VR1 along with R16 divide the regulator output voltage to +2.5V DC at the reference pin of U11, the programmable zener. As the output voltage rises, the voltage on the reference pin on U11 will rise. To compensate the rising output, U11 then draws more source current away from the base of Q12. This in turn turns off Q11 which drops the output voltage.

As the output voltage of the regulator falls, the reference pin voltage falls, turning off U11. This will increase current flow through Q12 which in turn will increase current from the emitter to collector on Q11, raising the output voltage.

The over-voltage crowbar circuit mentioned earlier consists of C14, D12, R17, R18 and SCR11. The SCR requires 1.4V gate to cathode in order to turn on. The zener is rated at 5.6V. Therefore a voltage of 7V on the +5V DC line will trigger the SCR (7V - 5.6 rated zener volts = 1.4V). Once the SCR is on, the +5V DC line is shorted to ground, allowing the fuse to open, preventing over-voltage damage to the TTL. R17 is a current limiting resistor for the SCR and R18 is the zener resistor. C14 filters out voltage spikes that could trigger the SCR.

The 35V AC RMS is rectified and filtered and is regulated to +30V DC via D26, Q21 and R23. D26 sets up 30V DC for the base of Q21 which is an emitter follower arrangement. Since the emitter follower has a voltage gain that is less than unity, the only volt-

# POWER DISTRIBUTION, VIDEO (CONT.)

age lost is from base to emitter which is approximately a 0.8V junction drop.

The center-tapped 15V AC RMS is utilized to supply three voltages. It is full wave rectified by D41 and D42 in order to supply the +20V DC average voltage used for the coin meters. It is also full wave rectified by D31-D34 in order to supply the plus and minus 12V DC. The positive side of the bridge feeds the LM340T (U31) +12V DC regulator while the negative side of the bridge is sent to the LM320 (U41) which regulates the -12V DC. D36 and D44 are used as protection diodes in the event that the output of the regulator exceeds the input.

# TROUBLESHOOTING Q*bert™ (PART TWO)

Favorable response to our last issue of "ON TARGET" has prompted us to print another symptom/possible cause table along with further discussion pertaining to Gottlieb's GG-III Video System Logic Board (A1).

FOREGROUND

Foreground generation on the GG-III System is initiated with three foreground registers (E1-2, E2-3, E4) all addressed via the microprocessor through program control. These registers are the Foreground Horizontal Position Register (E1-2), the Foreground Object Select Register (E2-3) and the Foreground Vertical Position Register (E4).

When the appearance of an object is required on a scan line, as detected by the Vertical Position Detector, the address generated by the Foreground Horizontal Position Register is copied into the Line Object Position RAM (H1-H4) and the address generated by the Foreground Object Select Register is copied into the Line Object Select RAM (J1-J6). The Line Object Position RAM contains the horizontal position of the object for the next scan line while the Line Object Select RAM contains the address for the Object ROM to address the desired object.

Since the foreground object size is 16 pixels by 16 lines, the Vertical Position Detector must generate enable pulses for 16 successive lines. The high order 4 bits of the Foreground Vertical Position Register and the Vertical Counter are summed (E5) and feed the Line RAM Enable Pulse Generator (E6, J8). When the sum values of E5 are all high, the write enable is generated. This pulse enables the transfer of data from the Foreground Horizontal Position Register to the Line Object Position RAM as well as the transfer of data from the Foreground Object Select Register to the Line Object Select RAM via the read/write ($\overline{WR}$) signal (FBA4) and the chip select ($\overline{CS}$) signal (S2) from the multiplexer (G9). For each pulse generated, information for the next scan line is loaded into the Line RAM.

When the Line RAM Enable Pulse Generator generates a pulse, it increments the 5-bit Line RAM Address Counter. This counter produces the addresses for the Line Object Position RAM's. When the Line Object Position RAM is being read, the 8-bit Line Buffer Address Counter (H5, H6) is loaded (every 1.6 usec). Before any new horizontal information can be loaded into the Line RAM, the counter must increment 16 times in order to address the 16 pixels that the foreground object will occupy that frame time.

The low order 4-bits of the Foreground Vertical Position Register and the Vertical Counter are summed (F5) and address the object information to the Foreground Object ROM (K4, K5, K6, K7-8) via the multiplexer (G5) and the Object ROM Address Latches (K1-K3).

# TROUBLESHOOTING Q*bert™ (PART TWO)

The Foreground Object ROM's receive their addressing from three sources: (1) The high order 8-bits from the Foreground Object Select Register, (2) 4-bits from the Vertical Position Detector and (3) The least significant bit (RA0) comes from the 800ns counter (L12). This counter will output every 4 clock cycles. The information out of the Object ROM's is loaded into four parallel to serial shift registers (L4-5, L5-6, L6-7, L7-8). Every clock cycle the outputs of the four shift registers are checked for data. If any output data, a write enable pulse (K12, K13, K9) is generated allowing data to transfer to the Line Object Buffers.

BACKGROUND

The Background Character Registers (E7) data is copied into the Background Buffer RAM (E10-11) during the first half of the vertical blanking time through DMA transfer (E9-10). Once the data is read by the Buffer RAM, the Character Register is ready to be loaded with new information. The data in the Buffer RAM is an 8-bit object number. This object number addresses the Background Character ROM (E11-12, E13) which contains pixel definition for the background character. The Character ROM will output 8-bits of information for two pixels for the 8 pixel by 8 line character. The horizontal counter, H1 and H2, and the vertical counter, V0, V1 and V2 are used so that the background object is displayed at the correct vertical and horizontal positions on the screen for each frame.

| SYMPTOMS | POSSIBLE CAUSES |
|---|---|
| PICTURE ROLLS VERTICALLY | D17, E16, E17, F16, J14, J17 |
| GLITCHING | D3, E5, G7, G9, J6, J16, J17, L13 |
| MISSING COLORS ON CHARACTERS | G10, G13-G15, K11-K13, L7-8 |
| CHARACTERS VERTICALLY SEPARATED | D15, D16, E4-E6, E15, J2, J5, J6, SIP 71 |
| INCORRECT VERTICAL POSITION OF CHARACTERS | E4, F5 |
| VERTICAL LINES ON SCREEN | J10, J11, K9, K11 |
| INCORRECT HORIZONTAL POSITION OF CHARACTERS | E1-2, G1, G2, H1-H6, H8, SIP 72 |
| CHARACTERS HORIZONTALLY SEPARATED | H3, L11, L12 |
| MISSING CHARACTERS | D3, E2-3, L12 |
| BLANK SCREEN (BLACK OR BLUE) | F15-F17, J16, J17 |
| BLURRY CHARACTERS | E15, E16, G5, J5, J6 |

## FLASHBACK

Gottlieb introduced the Vari-target in February 1969 on the four-player game COLLEGE QUEENS. It was the first target whose scoring value was entirely dependent upon the force of the hit. AIRPORT, introduced a month later and a two-player version of COLLEGE QUEENS, was one of the rare cases where the two- and four-player versions of a game had different themes. BASEBALL, the first single-player to have Vari-targets, didn't come along until April 1970.

## FIXIN' IT BY PHONE

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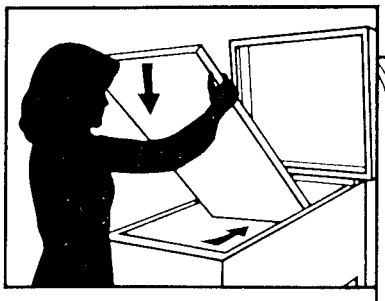
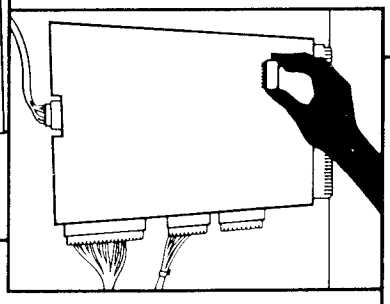
**1**



Complete, new playfield exchanges with old one and plugs into existing wiring harness.

**8 minutes**

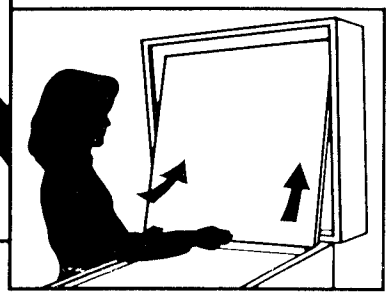
**2**



New game and sound proms insert into existing control and sound boards.

**5 minutes**

**3**



New backglass is installed in place of original one.

**2 minutes**

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