

SOUND/SPEECH, CIRCUIT ANALYSIS

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POWER SOURCES

Four input voltages are required for the Sound Speech Board. +30VDC for the LM379 Amplifier, +12VDC for the DAC'S, SC01A voice chip and LM741's, -12VDC also goes to the DAC's and LM741's, and +5VDC is used for the 6502 CPU, 6532 RIOT and all TTL. +30VDC, +12VDC and -12VDC are supplied to the A6J1 edge connector by the A7 auxiliary power supply. The +5VDC originates at the A2 power supply.

POWER UP

Upon applying power, the reset signal (Pin 40 6502, Pin 34 6532) is held low for at least 30ms. At this time, the processor is in a disabled state. This eliminates power on transience problems and allows time for the clock to stabilize. When the reset line goes high, the CPU is initialized internally through software to control orderly start-up. Crystal Y1 is oscillating at 3.579 MHz. Immediately it is squared up by U25, then divided by four by U2 74LS74, which makes the system operating speed 894 kHz.

SOUND SPEECH BOARD ENABLING

Sound enables S1, S2...*S32 (high at A6J1 connector), are inverted by U16 (74LS04), then input at ports PA0-PA5 of U15 respectively. At the same time, S1-S8 are norred at U17 (74LS30). When one of these four inputs goes low, PA7 of U15 (an edge detecting input) sees a low to high transition. When this transition occurs, the IRQ line goes low and the CPU reads ports PA0-PA5. The state of these ports (1's or 0's) determines which memory locations will be accessed.

Ports PB0-PB5 of U15 are used as inputs for SB1, the operator adjustable switch Pack.

*** NOTE:**

Sound 16 and Sound 32 may be enabled by lamp driver transistors. An LM393 dual comparator is used to insure a TTL low at U16 (74LS04) when enabled.

DATA ROUTING

Instructions for sound and speech are stored in the EPROMs U5 and U6 and transferred red to the CPU at t he start of the instruction cycle. A chip enable signal, CE (NOT) Pin 18, enables either EPROM for specific addresses.

Addressing is decoded and routed to the board hardware through U4 (74LS138), 3 to 8 line decoder, device select. G1 enable on U4 is tied high and G2A and G2B are tied low. Particular devices are selected according to the binary condition of AB12(A), AB13(B), and AB14(C). At least one device or area is being selected at all times. See Figures 1 and 2.

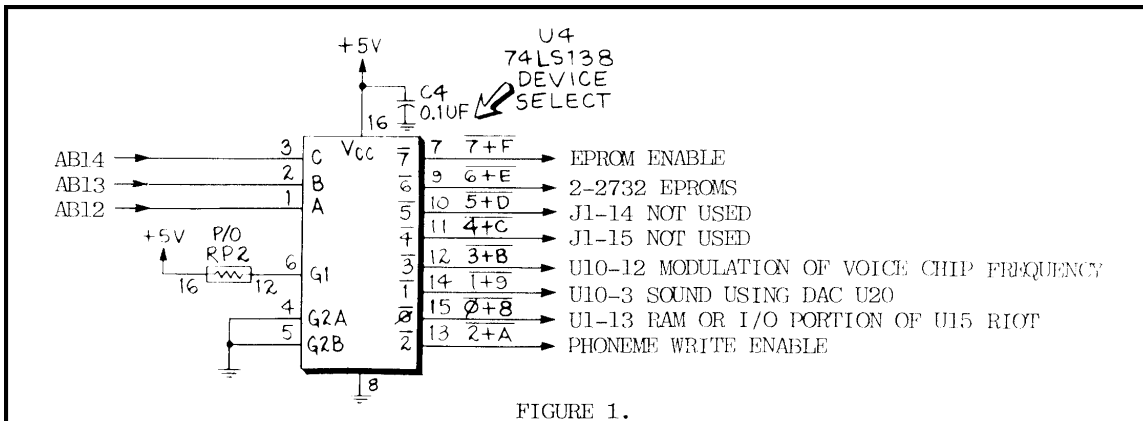


FIGURE 1.

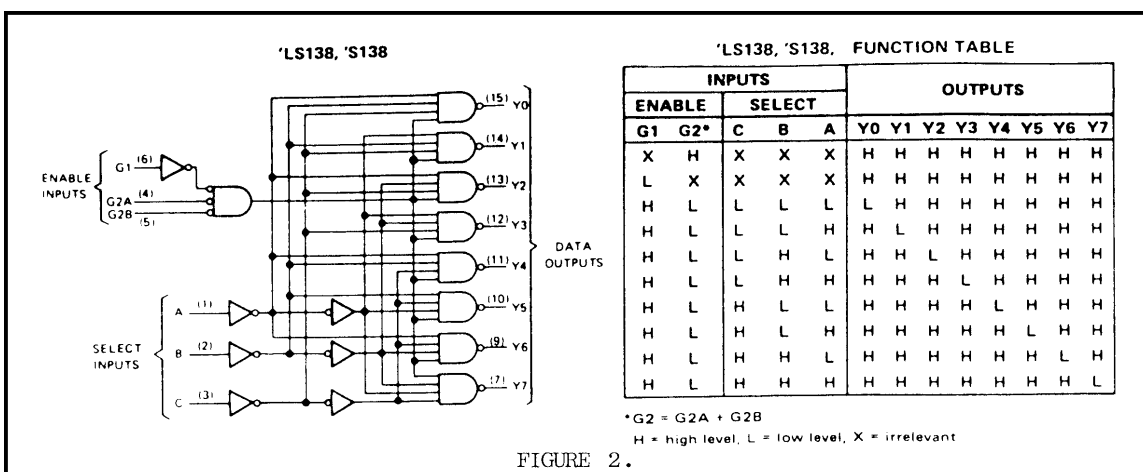


FIGURE 2.

Sound and speech are divided into two operating sections. To create sound, \$1000 is placed on the addressbus. The combination of address \$1000 and the 1+9 signal, enable the U7 and U8 latches. Data on the "D" inputs (6 inputs high) are then transferred to the "Q" outputs. This transfer process occurs whenever a new value is to be sent to the DAC. U20 is an 8-bit DAC with 8 input lines. Information from U7 and U8 is immediately transformed to a proportional output current through U20. All lines at a binary "1" condition would equal maximum current; all other combinations would produce a linearly proportional current. U22 is used as a current-to-voltage converter.

R13 is a 10K trimpot used for amplitude range adjustment. Pin 6 of U22 is the signal output and leads to R15, a 10K volume control pot which is used in conjunction with R16 to mix and balance the voice and sound. From there, the signal goes to Pin 9 of U23, a LM379 audio amplifier that provides 6 watts of power into an 8-ohm load.

SPEECH SYNTHESIS

U14 SC01A is a phoneme synthesizer capable of reproducing a single phoneme (basic unit of speech) on commands. 64 phonemes are able to be produced by setting P0-P5 to the proper phoneme code and then applying a strobe signal. A string of consecutive

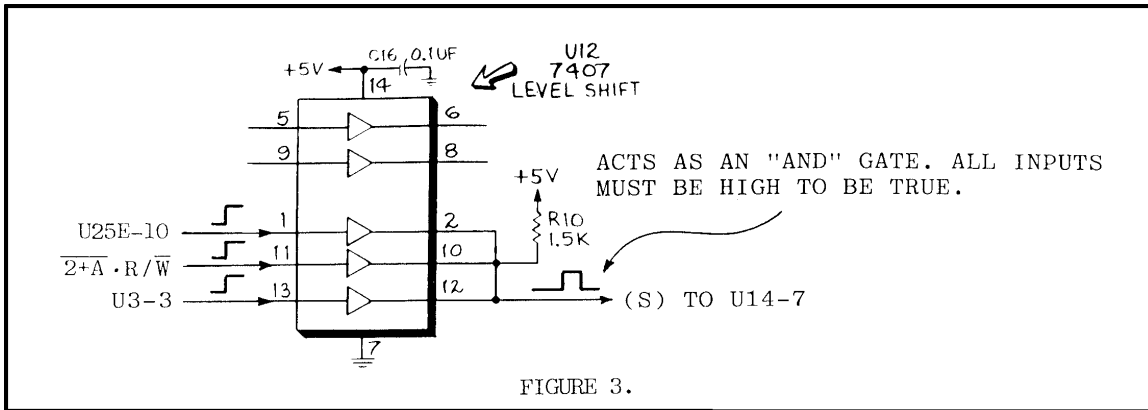
phonemes creates speech. Two latches, U11 and U18, the U19 DAC, Q1 and Q2, and U21 analog inverter comprise a software controlled variable clock signal to the SC01A. R6 is a 10K trimpot used for frequency adjustment.

As the clock frequency to Pins 15 and 16 of the SC01A changes, the frequency of the currently produced phoneme also changes, resulting in a variance in the base speech frequency. Sound effects may also be produced with the SC01A by changing the clock frequency. The SC01A will automatically signal the CPU that it has processed the current phoneme and needs immediate attention by toggling the A/R line Pin 8.

When a high to low transition occurs on this line (A/R), the SC01A is informing the CPU that phoneme data has been received. What the CPU actually senses is a low to high transition because of the inversion of the signal through the Q3 transistor. This indicates timing out of old phoneme data and is concurrent with a request for new phoneme data.

At this point, new data is sent out from the CPU through U13 level shift. Each of the data lines DB0-DB5 are pulled up by RP1 because the phoneme data must be at a +5V DC level for the SC01A to operate properly. This is also true for the strobe signal (S) and (L1) and (L2) inputs of the SC01A.

Latching of the phoneme data occurs on the rising edge of the (S) strobe signal (Pin 7 of the SC01A). 2+A and the R/W signal are combined together at Pins 5 and 6 of U10B 74LS02. This signal is buffered by U12 and anded with the Phase 1 clock and the clock output of U25E-10. The result is that all three inputs must be high for a high output (refer to Figure 3.). When any input is low, the output will be low.



This gating ensures correct timing of the (S) strobe signal. When a change in pitch is desired, the "G" enable, Pin13 of U9 goes high and data is transferred to the U12 level shift where it is buffered and then sent to the L1 and L2 inputs of the SC01A.

SC01A signal outputs, Pins 20, 21, 22 are tied together and sent to R16, 10K pot. As explained in the sound section, they are mixed with the sound output, and amplified by U23 LM379 dual power amplifier and output on A6J1 Pin 7.