

### Description

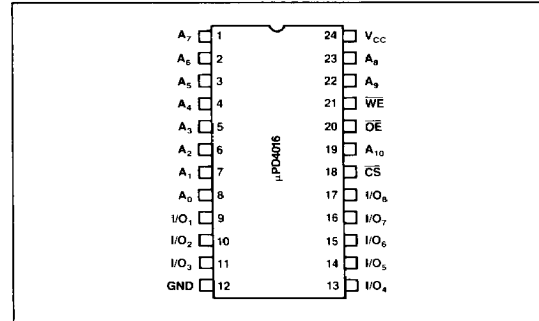
The μPD4016 is a 16,384-bit static Random-access Memory device organized as 2,048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with nonclocked static memories. The μPD4016 has a three-state output and offers a standby mode with an attendant 75% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The μPD4016 is packaged in a 600-mil-wide standard 24-pin dual-in-line package which is plug-compatible with 16K EPROMS.

### Features

- Scaled NMOS technology
- Completely static memory: no clock, no refresh
- Equal access and cycle times
- Single +5V power supply
- Automatic power-down
- All inputs and outputs directly TTL-compatible
- Common I/O capability
- OE eliminates need for external bus buffers
- Three-state outputs
- Plug-compatible with 16K 5V EPROMS (600 mil)
- Low power dissipation in standby mode
- Available in a standard 24-pin dual-in-line package (600-mil width)
- 4 performance ranges:

Device	Access Time	R/W Cycle Time	Power Supply	
			Active	Standby
μPD4016C-1	250ns	250ns	60mA	15mA
μPD4016C-2	200ns	200ns	60mA	15mA
μPD4016C-3	150ns	150ns	60mA	15mA
μPD4016C-5	120ns	120ns	60mA	15mA

### Pin Configuration



### Pin Identification

No.	Pin Symbol	Description
1-8, 22, 23	A <sub>0</sub> -A <sub>10</sub>	Address Inputs
9-11, 13-17	I/O <sub>1</sub> -I/O <sub>8</sub>	Data Input/Output
12	GND	Ground
18	CS	Chip Select
20	OE	Output Enable
21	WE	Write Enable
24	V <sub>CC</sub>	+5V Power Supply

### Truth Table

CS	OE	WE	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
L	L	L	Write	D <sub>IN</sub>	Active

### Absolute Maximum Ratings\*

Temperature Under Bias	-10°C to +85°C
Storage Temperature, T <sub>ST</sub>	-55°C to +125°C
Voltage on any Pin with Respect to Ground	-1.5V to +7V
DC Output Current, I <sub>O</sub>	20mA
Power Dissipation, P <sub>D</sub>	1W

\*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





## Capacitance ①

T<sub>A</sub> = 25°C; f = 1MHz

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input Capacitance	C <sub>IN</sub>			5	pF	V <sub>IN</sub> = 0V
I/O Capacitance	C <sub>IO</sub>			7	pF	V <sub>IO</sub> = 0V

Note: ① This parameter is sampled and not 100% tested.

## DC Characteristics

T<sub>A</sub> = 0°C to +70°C; V<sub>CC</sub> = 5V ± 10%

Parameter	Symbol	Limits			Unit	Test Conditions ①
		Min	Typ	Max		
Input Leakage Current	I <sub>I</sub>			10	μA	V <sub>CC</sub> = Max V <sub>IN</sub> = GND to V <sub>CC</sub>
Output Leakage Current	I <sub>O</sub>			10	μA	V <sub>CC</sub> = Max; CS = V <sub>IH</sub> V <sub>OUT</sub> = GND to V <sub>CC</sub>
Operating Current	I <sub>CC</sub>			60	mA	V <sub>CC</sub> = Max; CS = V <sub>IL</sub> (outputs open)
Standby Current	I <sub>SB</sub>			15	mA	V <sub>CC</sub> = Min to Max; CS = V <sub>IH</sub>
Input Low Voltage	V <sub>IL</sub>	-1.5		0.8	V	
Input High Voltage	V <sub>IH</sub>	2.0		6.0	V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 4mA
Output High Voltage	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = 1mA
Output Short-circuit Current	I <sub>OS</sub>			70	mA	V <sub>OUT</sub> = GND to V <sub>CC</sub>

Note: ① Input pulse levels: 0.8V to 2.2V  
Input rise and fall times: 10ns  
Input timing reference levels: 1.5V  
Output timing reference levels: 1.5V

Figure 1. Loading Conditions Test Circuit

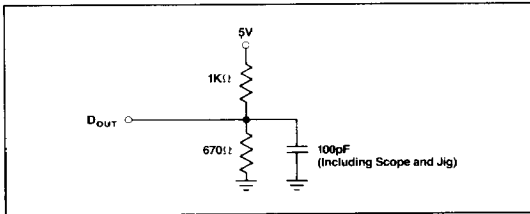
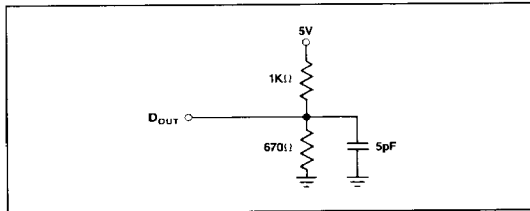


Figure 2. Input Pulse Test Circuit



## AC Characteristics

T<sub>A</sub> = 0°C to +70°C; V<sub>CC</sub> = 5V ± 10%

### Read Cycle

Parameter	Symbol	Limits ①								Unit	Notes
		4016-5		4016-3		4016-2		4016-1			
Read Cycle Time	t <sub>RC</sub>	120		150		200		250		ns	②
Address Access Time	t <sub>AA</sub>		120		150		200		250	ns	
Chip Select Access Time	t <sub>ACS</sub>		120		150		200		250	ns	③
Output Hold from Address Change	t <sub>OH</sub>	10		10		10		10		ns	
Chip Selection to Output in Low-Z	t <sub>LZ</sub>	10		10		10		10		ns	④ ⑤
Chip Deselection to Output in High-Z	t <sub>HZ</sub>		45		50		60		80	ns	④ ⑤
Output Enable to Output Valid	t <sub>OE</sub>		50		70		90		110	ns	
Output Enable to Output in Low-Z	t <sub>OLZ</sub>	10		10		10		10		ns	④ ⑤
Output Disable to Output in High-Z	t <sub>OHZ</sub>		45		50		60		80	ns	④ ⑤
Chip Selection to Power-up Time	t <sub>PU</sub>	0		0		0		0		ns	⑤
Chip Deselection to Power-down Time	t <sub>PD</sub>		60		70		90		110	ns	⑤

### Write Cycle

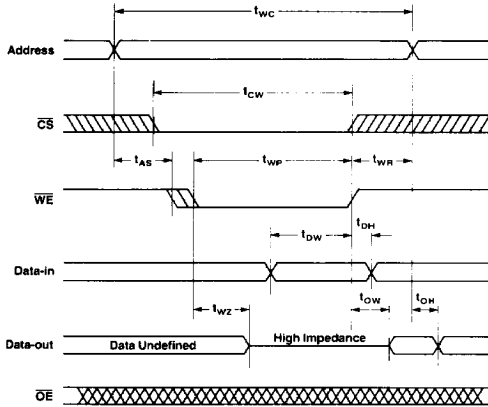
Parameter	Symbol	Limits ①								Unit	Notes
		4016-5		4016-3		4016-2		4016-1			
Write Cycle Time	t <sub>WC</sub>	120		150		200		250		ns	
Chip Selection to End of Write	t <sub>CW</sub>	90		120		160		200		ns	
Address Valid to End of Write	t <sub>AW</sub>	80		90		120		150		ns	
Address Set-up Time	t <sub>AS</sub>	0		0		0		0		ns	
Write Pulse Width	t <sub>WP</sub>	70		80		100		130		ns	⑥
Write Recovery Time	t <sub>WR</sub>	10		10		10		10		ns	
Data Valid to End of Write	t <sub>DW</sub>	45		50		60		80		ns	
Data Hold Time	t <sub>DH</sub>	0		0		0		0		ns	
Write Enabled to Output in High-Z	t <sub>WZ</sub>		45		50		60		80	ns	⑤ ⑦
Output Active from End of Write	t <sub>OW</sub>	10		10		10		10		ns	⑤ ⑦

Notes: ① See Part No. Package Width table below  
 ② All read cycle timings are referenced from the last valid address to the first transition address.  
 ③ Address valid prior to or coincident with CS transition low.  
 ④ Transition is measured - 200mV from steady-state voltage with specified load of Figure 1.  
 ⑤ This parameter is sampled and not 100% tested.  
 ⑥ If CS and OE are both low before write enabled, t<sub>WP</sub> = t<sub>WZ</sub> + t<sub>OW</sub>.  
 ⑦ Transition is measured - 200mV from steady-state voltage with specified load of Figure 2.

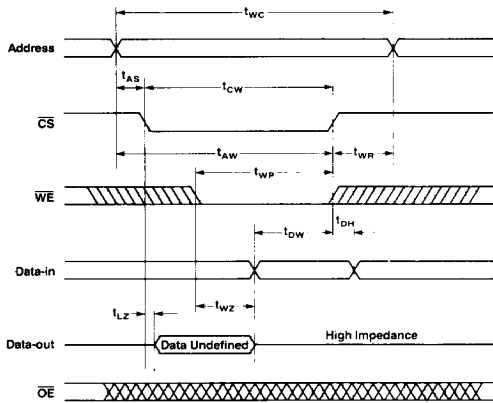
7

Timing Waveforms

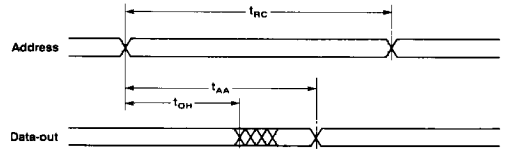
Write Cycle No. 1 ( $\overline{WE}$  Controlled)



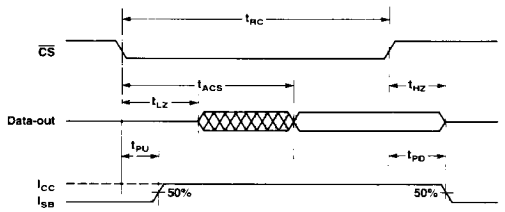
Write Cycle No. 2 ( $\overline{CS}$  Controlled)



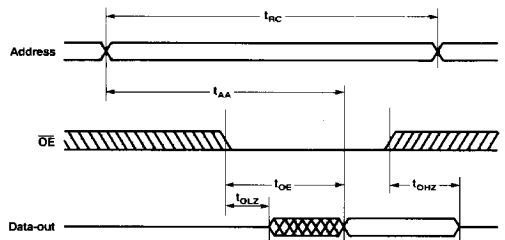
Read Cycle No. 1 ① ② ③



Read Cycle No. 2 ① ③ ④



Read Cycle No. 3 ① ②



- Notes: ①  $\overline{WE}$  is high for read cycles.  
 ② Device is continuously selected,  $\overline{CS} = V_{IL}$ .  
 ③  $OE = V_{IL}$ .  
 ④ Address valid prior to or coincident with  $\overline{CS}$  transition low.