Synertek.

MICRO-PROCESSORS

Features

- Single 5 V ±5% power supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus

- Instruction decoding and control
- Addressable memory range of up to 65 K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1 MHz, 2 MHz, 3 MHz and 4 MHz operation
- On-chip clock options
  * External single clock input
  * Crystal time base input
- 40 and 28 pin package versions
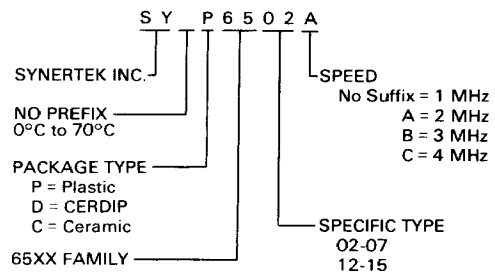- Pipeline architecture

Description

The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the SY6500 family are software compatible within the group and are bus compatible with the MC6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The external clock versions are geared for the multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz, 3 MHz and 4 MHz maximum operating frequencies.

Members of the Family

PART NUMBERS	CLOCKS	PINS	IRQ	NMI	RYD	ADDRESSING
SY6502	On-Chip	40	√	√	√	64 K
SY6503	''	28	√	√		4 K
SY6504	''	28	√			8 K
SY6505	''	28	√		√	4 K
SY6506	''	28	√			4 K
SY6507	''	28			√	8 K
SY6512	External	40	√	√	√	64 K
SY6513	''	28	√	√		4 K
SY6514	''	28	√			8 K
SY6515	''	28	√		√	4 K

Ordering Information

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S Y   P 6 5 0 2 A
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SYNERTEK INC.

NO PREFIX
0°C to 70°C

PACKAGE TYPE
P = Plastic
D = CERDIP
C = Ceramic

65XX FAMILY

SPEED
No Suffix = 1 MHz
A = 2 MHz
B = 3 MHz
C = 4 MHz

SPECIFIC TYPE
02-07
12-15

Only 6502 and 6512 are available in 3 and 4 MHz

Comments on the Data Sheet

The data sheet is constructed to review first the basic "Common Characteristics" — those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

SY6500 Internal Architecture
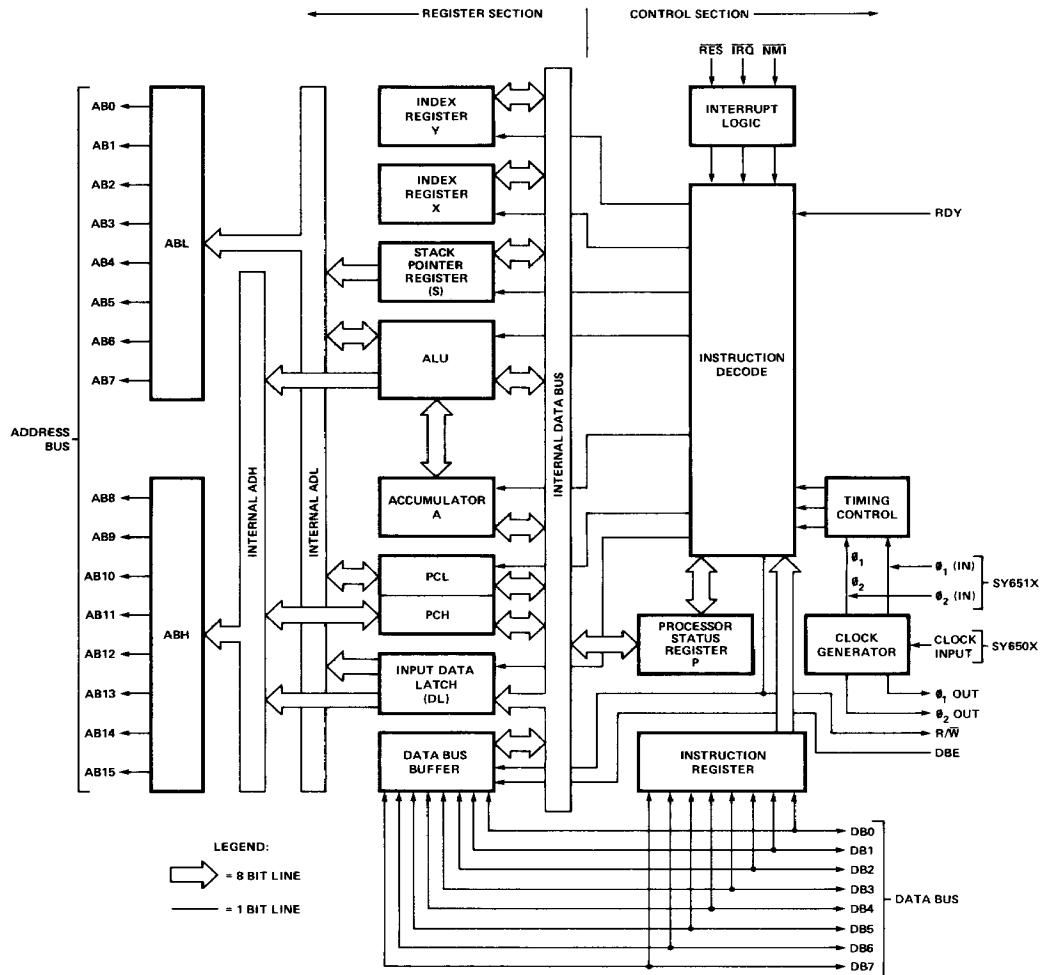
NOTE:
1. CLOCK GENERATOR IS NOT INCLUDED ON SY651X.
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE SY6500 PRODUCTS.

Absolute Maximum Ratings*

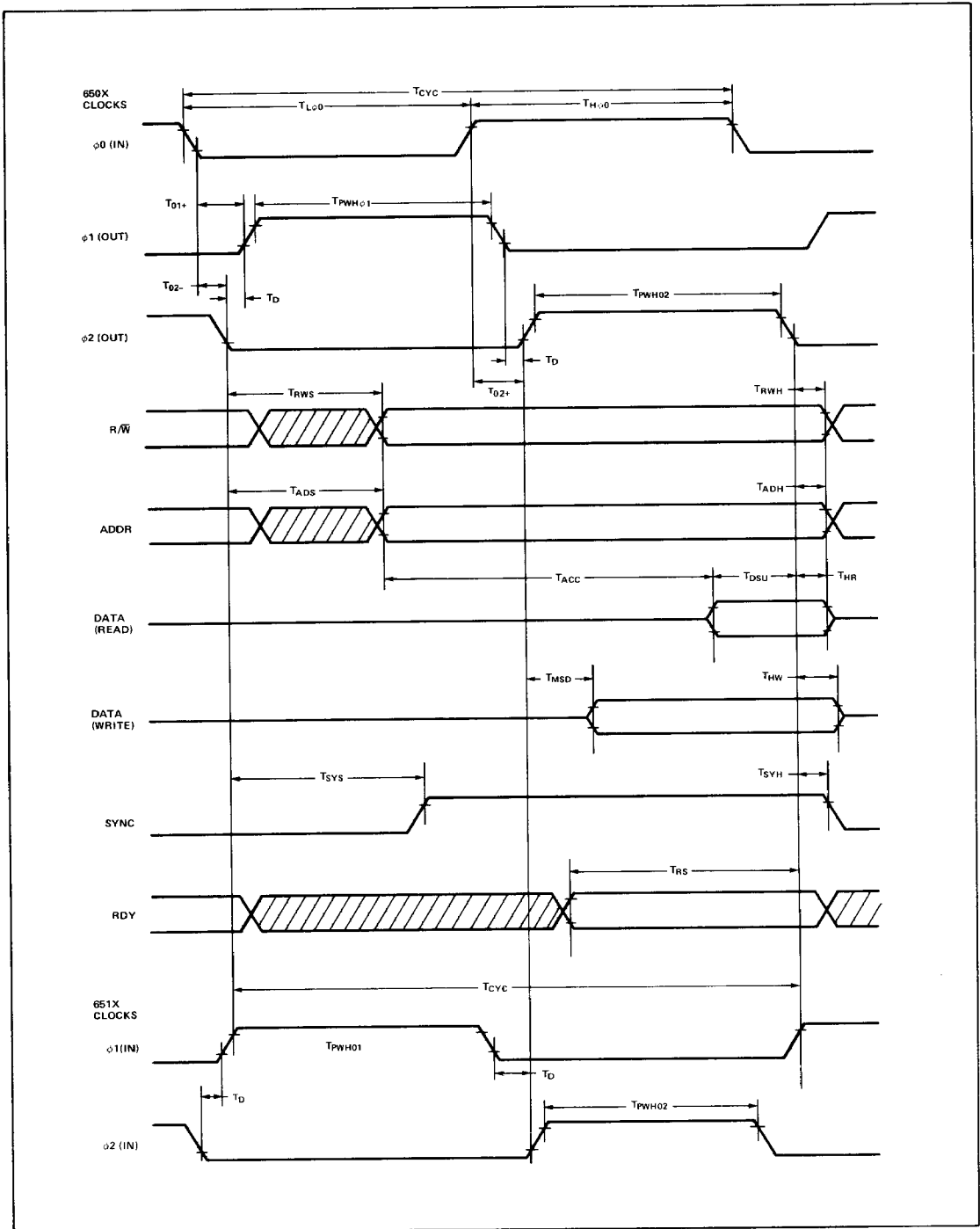| Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

Comment*

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

D.C. Characteristics (V_{CC} = 5.0V ±5%, T_A = 0-70°C)

($\emptyset_1$, $\emptyset_2$ applies to SY651X, $\emptyset_{o\,(in)}$ applies to SY650X)

Symbol	Characteristic			Min.	Max.	Unit
V_{IH}	Input High Voltage					
	Logic and $\emptyset_o$ (in) for	1,2,3 MHz		+2.0	V_{CC}	V
	all 650X devices	4 MHz		+3.3	V_{CC}	V
	$\emptyset_1$ and $\emptyset_2$ only for all 651X devices. Logic as 650X	All Speeds		V_{CC} −0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage					
	Logic, $\emptyset_{o\,(in)}$	(650X)		−0.3	+0.8	
	$\emptyset_1$, $\emptyset_2$	(651X)		−0.3	+0.2	V
I_{IL}	Input Loading					
	(V_{in} = 0 V, V_{CC} = 5.25 V)			−10	−300	µA
	RDY, S.O.					
I_{in}	Input Leakage Current					
	(V_{in} = 0 to 5.25 V, V_{CC} = 0)					
	Logic (Excl. RDY, S.O.)			—	2.5	µA
	$\emptyset_1$, $\emptyset_2$	(651X)		—	100	µA
	$\emptyset_{o\,(in)}$	(650X)		—	10.0	µA
I_{TSI}	Three-State (Off State) Input Current					
	(V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V)					
	DB0-DB7			—	±10	µA
V_{OH}	Output High Voltage					
	(I_{LOAD} = −100µAdc, V_{CC} = 4.75 V)	1,2,3 MHz		2.4	—	V
	SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	4 MHz		2.0	—	V
V_{OL}	Output Low Voltage					
	(I_{LOAD} = 1.6mAdc, V_{CC} = 4.75 V)	1,2,3 MHz		—	0.4	V
	SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	4 MHz		—	0.8	V
P_D	Power Dissipation	1 MHz and 2 MHz		—	700	mW
	(V_{CC} = 5.25V)	3 MHz		—	800	mW
		4 MHz		—	900	mW
C	Capacitance					
	(V_{in} = 0, T_A = 25°C, f = 1 MHz)					
C_{in}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE			—	10	
	DB0-DB7			—	15	
C_{out}	A0-A15, R/$\overline{W}$, SYNC			—	12	pF
$C_{\emptyset_o(in)}$	$\emptyset_{o\,(in)}$	(650X)		—	15	
$C_{\emptyset_1}$	$\emptyset_1$	(651X)		—	50	
$C_{\emptyset_2}$	$\emptyset_2$	(651X)		—	80	

MICRO PROCESSORS

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650X CLOCKS

φ0 (IN)

T_{CYC}

$T_{L\phi 0}$

$T_{H\phi 0}$

φ1 (OUT)

$T_{\phi 1+}$

$T_{PWH\phi 1}$

φ2 (OUT)

$T_{\phi 2-}$

T_D

$T_{PWH\phi 2}$

T_D

R/W̄

T_{RWS}

$T_{\phi 2+}$

T_{RWH}

ADDR

T_{ADS}

T_{ADH}

T_{ACC}

T_{DSU}

T_{HR}

DATA (READ)

T_{MSD}

T_{HW}

DATA (WRITE)

T_{SYS}

T_{SYH}

SYNC

T_{RS}

RDY

651X CLOCKS

T_{CYC}

φ1(IN)

$T_{PWH\phi 1}$

T_D

T_D

$T_{PWH\phi 2}$

φ2 (IN)

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Dynamic Operating Characteristics

($V_{CC} = 5.0 \pm 5\%$, $T_A = 0°$ to $70°C$)

Parameter	Symbol	1 MHz Min.	1 MHz Max.	2 MHz Min.	2 MHz Max.	3 MHz Min.	3 MHz Max.	4 MHz Min.	4 MHz Max.	Units
651X										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	µs
$\emptyset_1$ Pulse Width	$T_{PWH\emptyset_1}$	430	—	215	—	150	—			ns
$\emptyset_2$ Pulse Width	$T_{PWH\emptyset_2}$	470	—	235	—	160	—			ns
Delay Between $\emptyset_1$ and $\emptyset_2$	T_D	0	—	0	—	0	—			ns
$\emptyset_1$ and $\emptyset_2$ Rise and Fall Times[1]	T_R, T_F	0	25	0	20	0	15			ns
650X										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	µs
$\emptyset_{O(IN)}$ Low Time[2]	$T_{L\emptyset_o}$	480	—	240	—	160	—	110	—	ns
$\emptyset_{O(IN)}$ High Time[2]	$T_{H\emptyset_o}$	460	—	240	—	160	—	115	—	ns
$\emptyset_o$ Neg to $\emptyset_1$ Pos Delay[5]	T_{O1+}	10	70	10	70	10	70	10	70	ns
$\emptyset_o$ Neg to $\emptyset_2$ Neg Delay[5]	T_{O2-}	5	65	5	65	5	65	5	65	ns
$\emptyset_o$ Pos to $\emptyset_1$ Neg Delay[5]	T_{O1-}	5	65	5	65	5	65	5	65	ns
$\emptyset_o$ Pos to $\emptyset_2$ Pos Delay[5]	T_{O2+}	15	75	15	75	15	75	15	75	ns
$\emptyset_{o(IN)}$ Rise and Fall Time[1]	T_{RO}, T_{FO}	0	30	0	20	0	15	0	10	ns
$\emptyset_{1(OUT)}$ Pulse Width	$T_{PWH\emptyset_1}$	$T_{L\emptyset_o}$-20	$T_{L\emptyset_o}$	$T_{L\emptyset_o}$-20	$T_{L\emptyset_o}$	$T_{L\emptyset_o}$-20	$T_{L\emptyset_o}$	$T_{L\emptyset_o}$-20	$T_{L\emptyset_o}$	ns
$\emptyset_{2(OUT)}$ Pulse Width	$T_{PWH\emptyset_2}$	$T_{L\emptyset_o}$-40	$T_{L\emptyset_o}$-10	$T_{L\emptyset_o}$-40	$T_{L\emptyset_o}$-10	$T_{L\emptyset_o}$-40	$T_{L\emptyset_o}$-10	$T_{L\emptyset_o}$-40	$T_{L\emptyset_o}$-10	ns
Delay Between $\emptyset_1$ and $\emptyset_2$	T_D	5	—	5	—	5	—	5	—	ns
$\emptyset_1$ and $\emptyset_2$ Rise and Fall Times[1,3]	T_R, T_F	—	25	—	25	—	15	—	15	ns
650X, 651X										
R/$\overline{W}$ Setup Time	T_{RWS}	—	225	—	140	—	110	—	90	ns
R/$\overline{W}$ Hold Time	T_{RWH}	30	—	30	—	15	—	10	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	—	90	ns
Address Hold Time	T_{ADH}	30	—	30	—	15	—	10	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	—	110	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	20	75	—	70	ns
Write Data Hold Time	T_{HW}	60	150	60	150	30	130	20	—	ns
Sync Setup Time	T_{SYS}	—	350	—	175	—	100	—	90	ns
Sync Hold Time	T_{SYH}	30	—	30	—	15	—	15	—	ns
RDY Setup Time[4]	T_{RS}	200	—	200	—	150	—	120	—	ns

NOTES:

1. Measured between 10% and 90% points.
2. Measured at 50% points.
3. Load = 1 TTL load +30 pF.
4. RDY must never switch states within T_{RS} to end of $\emptyset_2$.
5. Load = 100 pF.
6. The 2 MHz devices are identified by an "A" suffix.
7. The 3 MHz devices are identified by a "B" suffix.
8. The 4 MHz devices are identified by a "C" suffix.

TIMING DIAGRAM NOTE:

Because the clock generation for the SY650X and SY651X is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters are referred to these lines and scale variations in the diagrams are of no consequence.

MICRO-PROCESSORS

Pin Functions

Clocks ($\emptyset_1$, $\emptyset_2$)

The SY651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The SY650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (A_0-A_{15}) (See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB_0-DB_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\emptyset_2$) clock, thus allowing data output from microprocessor only during $\emptyset_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the SY6512, only.

Ready (RDY)

This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\emptyset_1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\emptyset_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during $\emptyset_2$ time.

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during $\emptyset_2$ (phase 2) and will begin the appropriate interrupt routine on the $\emptyset_1$ (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\emptyset_1$.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\emptyset_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\emptyset_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)

This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for data transfer out of the processor.

Programming Characteristics

INSTRUCTION SET — ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
BCC	Branch on Carry Clear		
BCS	Branch on Carry Set	NOP	No Operation
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	ORA	"OR" Memory with Accumulator
BMI	Branch on Result Minus		
BNE	Branch on Result not Zero	PHA	Push Accumulator on Stack
BPL	Branch on Result Plus	PHP	Push Processor Status on Stack
BRK	Force Break	PLA	Pull Accumulator from Stack
BVC	Branch on Overflow Clear	PLP	Pull Processor Status from Stack
BVS	Branch on Overflow Set		
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag		
CMP	Compare Memory and Accumulator	SBC	Subtract Memory from Accumulator with Borrow
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SEC	Set Carry Flag
		SED	Set Decimal Mode
DEC	Decrement Memory by One	SEI	Set Interrupt Disable Status
DEX	Decrement Index X by One	STA	Store Accumulator in Memory
DEY	Decrement Index Y by One	STX	Store Index X in Memory
		STY	Store Index Y in Memory
EOR	"Exclusive-or" Memory with Accumulator		
		TAX	Transfer Accumulator to Index X
INC	Increment Memory by One	TAY	Transfer Accumulator to Index Y
INX	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
INY	Increment Index Y by One	TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Pointer
JMP	Jump to New Location	TYA	Transfer Index Y to Accumulator
JSR	Jump to New Location Saving Return Address		

MICRO PROCESSORS

ADDRESSING MODES

Accumulator Addressing

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero page Addressing

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing — (X, Y indexing)

This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing — (X, Y indexing)

This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

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Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as (Indir-ect,X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

In indirect indexed addressing (referred to as (Indir-ect),Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

Programming Characteristics

PROGRAMMING MODEL

INSTRUCTION SET — OP CODES, EXECUTION TIME, MEMORY REQUIREMENTS

MNEMONIC	OPERATION	IMMEDIATE (OP N #)	ABSOLUTE (OP N #)	ZERO PAGE (OP N #)	ACCUM (OP N #)	IMPLIED (OP N #)	(IND, X) (OP N #)	(IND) Y (OP N #)	Z PAGE X (OP N #)	ABS, X (OP N #)	ABS, Y (OP N #)	RELATIVE (OP N #)	INDIRECT (OP N #)	Z PAGE Y (OP N #)	CONDITION CODES N Z C I D V
A D C	A + M + C → A (4)(1)	69 2 2	6D 4 3	65 3 2			61 6 2	71 5 2	75 4 2	7D 4 3	79 4 3				✓ ✓ ✓ − − ✓
A N D	A ∧ M → A (1)	29 2 2	2D 4 3	25 3 2			21 6 2	31 5 2	35 4 2	3D 4 3	39 4 3				✓ ✓ − − − −
A S L	C ◄ 7 0 ◄ 0		0E 6 3	06 5 2	0A 2 1				16 6 2	1E 7 3					✓ ✓ ✓ − − −
B C C	BRANCH ON C=0 (2)											90 2 2			− − − − − −
B C S	BRANCH ON C=1 (2)											B0 2 2			− − − − − −
B E Q	BRANCH ON Z=1 (2)											F0 2 2			− − − − − −
B I T	A ∧ M		2C 4 3	24 3 2											M₇ ✓ − − − M₆
B M I	BRANCH ON N-1 (2)											30 2 2			− − − − − −
B N E	BRANCH ON Z=0 (2)											D0 2 2			− − − − − −
B P L	BRANCH ON N=0 (2)											10 2 2			− − − − − −
B R K	(See Fig 1)					00 7 1									− − − ✓ − −
B V C	BRANCH ON V=0 (2)											50 2 2			− − − − − −
B V S	BRANCH ON V-1 (2)											70 2 2			− − − − − −
C L C	0 → C					18 2 1									− − 0 − − −
C L D	0 → D					D8 2 1									− − − − 0 −
C L I	0 → I					58 2 1									− − − 0 − −
C L V	0 → V					B8 2 1									− − − − − 0
C M P	A-M (1)	C9 2 2	CD 4 3	C5 3 2			C1 6 2	D1 5 2	D5 4 2	DD 4 3	D9 4 3				✓ ✓ ✓ − − −
C P X	X-M	E0 2 2	EC 4 3	E4 3 2											✓ ✓ ✓ − − −
C P Y	Y-M	C0 2 2	CC 4 3	C4 3 2											✓ ✓ ✓ − − −
D E C	M-1 → M		CE 6 3	C6 5 2					D6 6 2	DE 7 3					✓ ✓ − − − −
D E X	X-1 → X					CA 2 1									✓ ✓ − − − −
D E Y	Y-1 → Y					88 2 1									✓ ✓ − − − −
E O R	A ⊻ M → A (1)	49 2 2	4D 4 3	45 3 2			41 6 2	51 5 2	55 4 2	5D 4 3	59 4 3				✓ ✓ − − − −
I N C	M+1 → M		EE 6 3	E6 5 2					F6 6 2	FE 7 3					✓ ✓ − − − −
I N X	X + 1 → X					E8 2 1									✓ ✓ − − − −
I N Y	Y + 1 → Y					C8 2 1									✓ ✓ − − − −
J M P	JUMP TO NEW LOC		4C 3 3										6C 5 3		− − − − − −
J S R	(See Fig. 2) JUMP SUB		20 6 3												− − − − − −
L D A	M → A (1)	A9 2 2	AD 4 3	A5 3 2			A1 6 2	B1 5 2	B5 4 2	BD 4 3	B9 4 3				✓ ✓ − − − −

MNEMONIC	OPERATION	IMMEDIATE (OP N #)	ABSOLUTE (OP N #)	ZERO PAGE (OP N #)	ACCUM (OP N #)	IMPLIED (OP N #)	(IND, X) (OP N #)	(IND) Y (OP N #)	Z PAGE X (OP N #)	ABS, X (OP N #)	ABS, Y (OP N #)	RELATIVE (OP N #)	INDIRECT (OP N #)	Z PAGE Y (OP N #)	CONDITION CODES N Z C I D V
L D X	M → X (1)	A2 2 2	AE 4 3	A6 3 2							BE 4 3			B6 4 2	✓ ✓ − − − −
L D Y	M → Y (1)	A0 2 2	AC 4 3	A4 3 2					B4 4 2	BC 4 3					✓ ✓ − − − −
L S R	0 → 7 0 → C		4E 6 3	46 5 2	4A 2 1				56 6 2	5E 7 3					0 ✓ ✓ − − −
N O P	NO OPERATION					EA 2 1									− − − − − −
O R A	A ∨ M → A (1)	09 2 2	0D 4 3	05 3 2			01 6 2	11 5 2	15 4 2	1D 4 3	19 4 3				✓ ✓ − − − −
P H A	A → Ms S-1 → S					48 3 1									− − − − − −
P H P	P → Ms S-1 → S					08 3 1									− − − − − −
P L A	S + 1 → S Ms → A					68 4 1									✓ ✓ − − − −
P L P	S + 1 → S Ms → P					28 4 1									(RESTORED)
R O L	◄ 7 0 ◄ C		2E 6 3	26 5 2	2A 2 1				36 6 2	3E 7 3					✓ ✓ ✓ − − −
R O R	C → 7 0		6E 6 3	66 5 2	6A 2 1				76 6 2	7E 7 3					✓ ✓ ✓ − − −
R T I	(See Fig. 1) RTRN INT.					40 6 1									RESTORED
R T S	(See Fig. 2) RTRN SUB					60 6 1									− − − − − −
S B C	A-M-C̄ → A (1)	E9 2 2	ED 4 3	E5 3 2			E1 6 2	F1 5 2	F5 4 2	FD 4 3	F9 4 3				✓ ✓ (3) − − ✓
S E C	1 → C					38 2 1									− − 1 − − −
S E D	1 → D					F8 2 1									− − − − 1 −
S E I	1 → I					78 2 1									− − − 1 − −
S T A	A → M		8D 4 3	85 3 2			81 6 2	91 6 2	95 4 2	9D 5 3	99 5 3				− − − − − −
S T X	X → M		8E 4 3	86 3 2										96 4 2	− − − − − −
S T Y	Y → M		8C 4 3	84 3 2					94 4 2						− − − − − −
T A X	A → X					AA 2 1									✓ ✓ − − − −
T A Y	A → Y					A8 2 1									✓ ✓ − − − −
T S X	S → X					BA 2 1									✓ ✓ − − − −
T X A	X → A					8A 2 1									✓ ✓ − − − −
T X S	X → S					9A 2 1									− − − − − −
T Y A	Y → A					98 2 1									✓ ✓ − − − −

(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
    ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BELOW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
    ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

- X   INDEX X
- Y   INDEX Y
- A   ACCUMULATOR
- M   MEMORY PER EFFECTIVE ADDRESS
- Ms MEMORY PER STACK POINTER
- +   ADD
- −   SUBTRACT
- ∧   AND
- ∨   OR
- ⊻   EXCLUSIVE OR
- ✓   MODIFIED
- −   NOT MODIFIED
- M₇ MEMORY BIT 7
- M₆ MEMORY BIT 6
- N   NO CYCLES
- #   NO BYTES

SY6502 — 40 Pin Package

```
        Vss  1        40  RES
        RDY  2        39  Ø2 (OUT)
    Ø1 (OUT) 3        38  S.O.
         IRQ 4        37  Ø0 (IN)
        N.C. 5        36  N.C.
         NMI 6        35  N.C.
        SYNC 7        34  R/W
         Vcc 8        33  DB0
        AB0  9        32  DB1
        AB1 10        31  DB2
        AB2 11        30  DB3
        AB3 12        29  DB4
        AB4 13        28  DB5
        AB5 14        27  DB6
        AB6 15        26  DB7
        AB7 16        25  AB15
        AB8 17        24  AB14
        AB9 18        23  AB13
       AB10 19        22  AB12
       AB11 20        21  Vss
```

Features

- 65K Addressable Bytes of Memory
- IRQ Interrupt   • NMI Interrupt
- On-the-chip Clock
  - √ TTL Level Single Phase Input
  - √ Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used for single cycle execution)
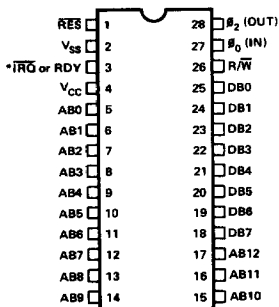- Two Phase Output Clock for Timing of Support Chips

SY6503 — 28 Pin Package

```
        RES  1        28  Ø2 (OUT)
        Vss  2        27  Ø0 (IN)
        IRQ  3        26  R/W
        NMI  4        25  DB0
        Vcc  5        24  DB1
        AB0  6        23  DB2
        AB1  7        22  DB3
        AB2  8        21  DB4
        AB3  9        20  DB5
        AB4 10        19  DB6
        AB5 11        18  DB7
        AB6 12        17  AB11
        AB7 13        16  AB10
        AB8 14        15  AB9
```
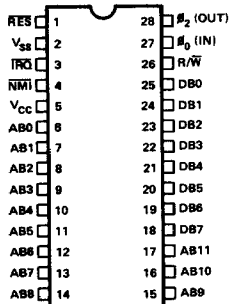
Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bi-Directional Data Bus

SY6504 & SY6507 — 28 Pin Package

```
        RES  1        28  Ø2 (OUT)
        Vss  2        27  Ø0 (IN)
  *IRQ or RDY 3       26  R/W
        Vcc  4        25  DB0
        AB0  5        24  DB1
        AB1  6        23  DB2
        AB2  7        22  DB3
        AB3  8        21  DB4
        AB4  9        20  DB5
        AB5 10        19  DB6
        AB6 11        18  DB7
        AB7 12        17  AB12
        AB8 13        16  AB11
        AB9 14        15  AB10
```

Features

- IRQ Interrupt (6504 only)
- RDY Signal (6507 only)
- 8K Addressable Bytes of Memory (AB00-AB12)
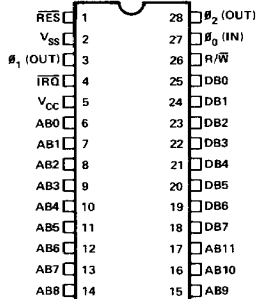- On-the-chip Clock
- 8 Bit Bi-Directional Data Bus

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SY6505 — 28 Pin Package

```
RES    1        28  ø₂ (OUT)
Vss    2        27  ø₀ (IN)
RDY    3        26  R/W̄
ĪRQ    4        25  DB0
Vcc    5        24  DB1
AB0    6        23  DB2
AB1    7        22  DB3
AB2    8        21  DB4
AB3    9        20  DB5
AB4   10        19  DB6
AB5   11        18  DB7
AB6   12        17  AB11
AB7   13        16  AB10
AB8   14        15  AB9
```
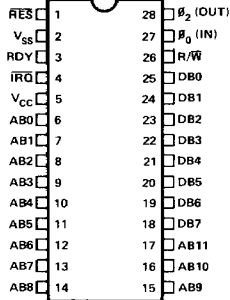
Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
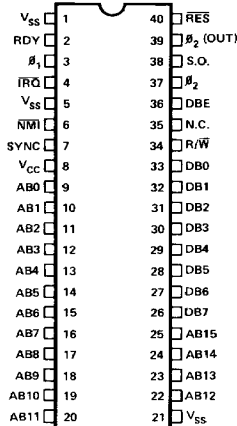- ĪRQ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus

SY6506 — 28 Pin Package

```
RES      1        28  ø₂ (OUT)
Vss      2        27  ø₀ (IN)
ø₁(OUT)  3        26  R/W̄
ĪRQ      4        25  DB0
Vcc      5        24  DB1
AB0      6        23  DB2
AB1      7        22  DB3
AB2      8        21  DB4
AB3      9        20  DB5
AB4     10        19  DB6
AB5     11        18  DB7
AB6     12        17  AB11
AB7     13        16  AB10
AB8     14        15  AB9
```

Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- ĪRQ Interrupt
- Two phases off
- 8 Bit Bi-Directional Data Bus

SY6512 — 40 Pin Package

```
Vss     1        40  RES
RDY     2        39  ø₂ (OUT)
ø₁      3        38  S.O.
ĪRQ     4        37  ø₂
Vss     5        36  DBE
NMI     6        35  N.C.
SYNC    7        34  R/W̄
Vcc     8        33  DB0
AB0     9        32  DB1
AB1    10        31  DB2
AB2    11        30  DB3
AB3    12        29  DB4
AB4    13        28  DB5
AB5    14        27  DB6
AB6    15        26  DB7
AB7    16        25  AB15
AB8    17        24  AB14
AB9    18        23  AB13
AB10   19        22  AB12
AB11   20        21  Vss
```
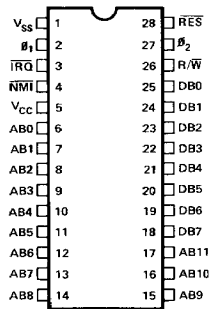
Features

- 65K Addressable Bytes of Memory
- ĪRQ Interrupt
- NMI Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus
- SYNC Signal
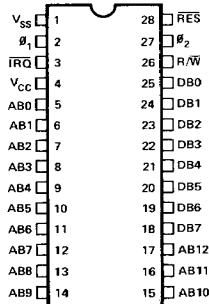- Two phase input
- Data Bus Enable

MICRO PROCESSORS

SY6513 — 28 Pin Package

```
VSS    1        28  RES
Ø1     2        27  Ø2
IRQ    3        26  R/W
NMI    4        25  DB0
VCC    5        24  DB1
AB0    6        23  DB2
AB1    7        22  DB3
AB2    8        21  DB4
AB3    9        20  DB5
AB4   10        19  DB6
AB5   11        18  DB7
AB6   12        17  AB11
AB7   13        16  AB10
AB8   14        15  AB9
```

Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bi-Directional Data Bus

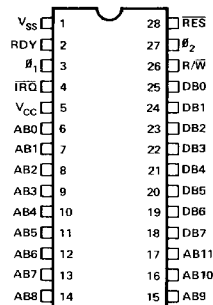## SY6514 — 28 Pin Package

```
VSS    1        28  RES
Ø1     2        27  Ø2
IRQ    3        26  R/W
VCC    4        25  DB0
AB0    5        24  DB1
AB1    6        23  DB2
AB2    7        22  DB3
AB3    8        21  DB4
AB4    9        20  DB5
AB5   10        19  DB6
AB6   11        18  DB7
AB7   12        17  AB12
AB8   13        16  AB11
AB9   14        15  AB10
```

Features

- 8K Addressable Bytes of Memory (AB00-AB12)
- Two phase clock input
- IRQ Interrupt
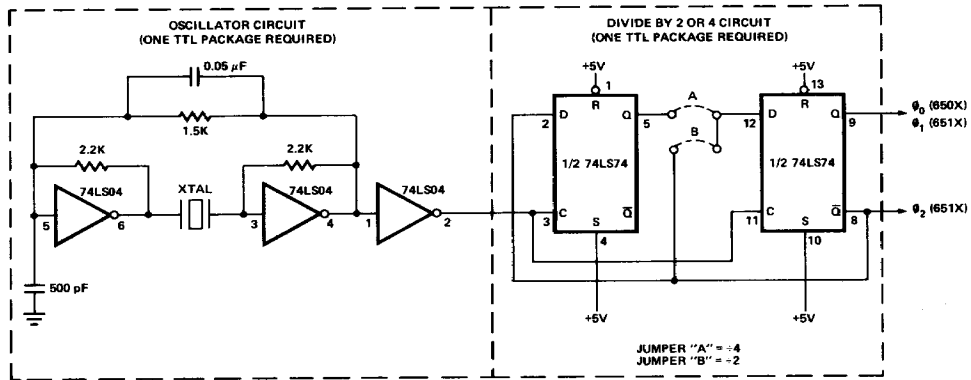- 8 Bit Bi-Directional Data Bus

SY6515 — 28 Pin Package

```
VSS    1        28  RES
RDY    2        27  Ø2
Ø1     3        26  R/W
IRQ    4        25  DB0
VCC    5        24  DB1
AB0    6        23  DB2
AB1    7        22  DB3
AB2    8        21  DB4
AB3    9        20  DB5
AB4   10        19  DB6
AB5   11        18  DB7
AB6   12        17  AB11
AB7   13        16  AB10
AB8   14        15  AB9
```
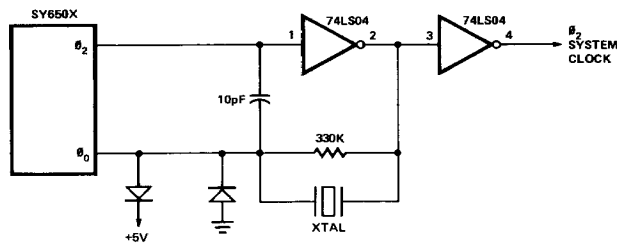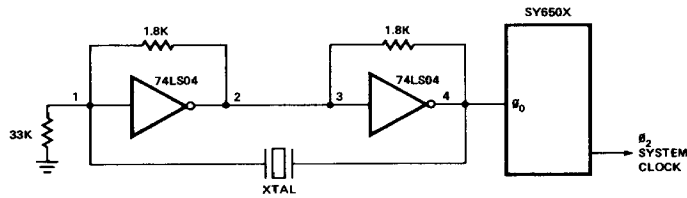
Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- IRQ Interrupt
- 8 Bit Bi-Directional Data Bus

Synertek.

Clock Generation Circuits*

*For further details refer to Synertek SY6500 Applications Information Note AN2. Crystals used are CTS Knight MP Series or equivalents. (Series Mode)

OSCILLATOR CIRCUIT
(ONE TTL PACKAGE REQUIRED)

DIVIDE BY 2 OR 4 CIRCUIT
(ONE TTL PACKAGE REQUIRED)

JUMPER "A" = ÷4
JUMPER "B" = ÷2

CRYSTAL FREQUENCY	OUTPUT FREQUENCY	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz

MICRO-PROCESSORS