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[54] **INTEGRATED CIRCUIT MICROPROCESSOR WITH PARALLEL BINARY ADDER HAVING ON-THE-FLY CORRECTION TO PROVIDE DECIMAL RESULTS**

[75] Inventors: **Charles Ingerham Peddle**, Audubon; **Wilbur L. Mathys**, Spring City; **William D. Mensch, Jr.**, Norristown; **Rodney H. Orgill**, Hatfield, all of Pa.

[73] Assignee: **MOS Technology, Inc.**, Norristown, Pa.

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[51] **Int. Cl.**[2] **G06F 7/385**

[58] **Field of Search** 235/173–174

[56] **References Cited**

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Primary Examiner—R. Stephen Dildine, Jr.

[57] **ABSTRACT**

Disclosed is an integrated circuit microprocessor with a parallel binary adder whose output can be corrected on-the-fly to provide decimal results. The correction is by logical gating which operates selectively and on-the-fly, that is, while the sum from the output of the binary adder is being transferred to an accumulator. As a result, the same binary adder can provide the binary sum of the operands supplied to it, or the binary coded decimal sum of bcd operands, or the binary coded decimal difference of bcd operands, in a single operating cycle and without the need to recycle the sum of the operands through the adder. This single cycle correction significantly speeds up the operation of the invented microprocessor as compared to known prior art microprocessors which recycle the adder output when a binary coded decimal sum or difference is required.

8 Claims, 4 Drawing Figures