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Technical Data

Dialog BOi27

9010A Micro-System Troubleshooter

Avoiding Potential Problems When Getting Started

Introduction

This document is intended to be used in conjunction with the 9010A Operator's Manual when getting started on troubleshooting *your* own system. It is not intended to be a substitute for the manual.

This document covers common precautions to be observed and the error messages you may encounter when plugging the 9010A interface into your unit-under-test (UUT) for the first time. More detailed information is contained in your Operator's Manual. Should applications assistance be necessary, please contact your Fluke Sales Engineer.

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I. Initial Considerations

Before starting, there are a few important points to consider with regard to the 9010A and its interaction with your system. While most users will find that they can begin troubleshooting with no extraordinary efforts, some special purpose designs and applications may require special handling. The user needs to be aware of these situations and how to handle them.

A. Starting Off With a Known Good Unit-Under-Test (UUT)

When documentation is unavailable or it is desired that the LEARN feature be used, it is important that a known good UUT is tested. In the event a faulty UUT is used, false information is likely to be learned. This occurs since the LEARN algorithm acts upon the information returned from a series of read and write operations. If misinformation is fed into the algorithm, erroneous values are returned.

B. Multiple Processor Systems

It is common in today's technology to design a system with multiple processors. In the typical case where the processors talk to each other through a communication port, the 9010A is easily used by plugging into each processor socket one-by-one and testing up to the communication port. In the less typical case, where processors share memory, additional precautions must be taken. In these cases it is possible that one processor may interfere with the task being performed by the other. While handshake lines generally insure that two processors are not on the bus at the same time, one processor may corrupt data in memory, and prevent the other processor from successfully performing a test such as a RAM test. In these rare cases, it is necessary for the user to somehow prevent the two processors from accessing the same memory locations. This may be done by tying a line on the UUT or possibly by WRITING data to a particular location to disable one of the microprocessors.

C. Systems With Watchdog Timers

Systems designed with watchdog timers must be individually checked to see what this timer (reset line) is tied to. If the timer is only tied to the processor, it can be

ignored in the SET UP mode. If the timer is tied to devices other than the processor then it must physically be disabled by tying the line either high or low.

D. Multiple Page Memories

Sometimes, one page of memory is not sufficient for system operation. In such cases the designer incorporates multiple pages of memory. The processor switches between these banks or pages in order to properly address them. The LEARN operation is not designed to find these multiple pages of memory. However, the 9010A can easily test multiple pages of memory. A common technique is to use an I/O port to switch between banks of memory. Using the 9010A WRITE key, the desired bank can be selected for testing. It is then necessary to select either the ROM TEST or the RAM TEST as appropriate. This sequence of selecting a memory bank through a WRITE and then testing the bank of memory through RAM TEST or ROM TEST can easily be put together by the user in a 9010A program.

E. I/O Ports Connected To Active Stimulus

Due to the series of reads and writes performed by LEARN, I/O ports are stimulated when LEARN occurs across those addresses. If this I/O port is connected to a stimulus device, the device will be activated. If this port is connected to a memory device such as a disk drive, then the disk will very possibly be written on.

F. Enableable Lines

Sometimes, enableable lines (such as READY and HOLD on the 8080 Microprocessor) interfere with the LEARN process. This may occur if, for example, the board is out of the system, and the board needs to be in the system to have READY driven to the active state If this is the case, a POD TIMEOUT message will appear on the 9010A If this condition occurs, the READY and HOLD lines may be disabled through the SET-Cl-' procedure. The SET-UP menu items on the 8080 are ENABLE READY? and ENABLE HOLD? Answer NO to each of these one at a time and see which one(s) allow the pod and board to function.

G. Warning

Plug the pod into the 9010A only when power is off. Plug the pod into the UUT only when the 9010A is powered on. Failure to do this may cause damage to the pod or the 9010A.

II. Initial Setup

After taking into account any of these initial considerations, a brief setup procedure is recommended in order to verify the integrity ot the 9010A and configure the UUT and the 9010A in such a way as to make them complimentary This is accomplished first by powering up the 9010A which performs a self test on itself, Next, a self test of the pod is performed by locking the pod into the self test socket and pressing BUS TEST on the 9010A. Finally, plug the pod into the UUT and again select BUS TEST.

A. Fail On Power Up

When the 9010A is turned on, a self test is performed verifying its integrity. If the message indicates a failure exists in the 9010A, refer to the service manual or contact your local Fluke Service Center.

B. Pod Self Test Fail

If, when performing a pod self test, the message refers to a pod self test failure, the pod has failed. Refer to the pod manual or contact your local Fluke Service Center.

C. Pod Time Out

The pod timeout message can occur both during a pod self test or during operation with a UUT. This message indicates that power at the microprocessor plug is OK, but the pod is not communicating with the 9010A mainframe. Check first to make sure that the microprocessor plug is plugged in firmly wirh no pins bent under or missing (either into the self-test sucker or the UUT) During a pod self test, this message means the pod has failed and needs to be serviced Occurence of this message during UUT operation may signify one of several symptoms. Again, check to make sure the microprocessor plug is plugged in firmly. Make sure the microprocessor socket has no pins bent under. Next, disable the forcing lines in the SET-UP mode. If the UUT requires an 8080 pod, the forcing lines would be READY and HOLD. SET-Up

allows you to disable these lines before they enter the processor. (Thus, preventing these line:, from stopping the pod processor.) Answer NO to the SET-UP questions, ENABLE READY and ENABLE HOLD. If this doesn't clear the problem, the UUT clock should be checked for functionality.

This can be easily done with the troubleshooting probe. Assuming the clock is working, the problem may be caused by a UUT clock that is slower than that expected by the 9010A. In this case the pod (which is running off the UUT clock) does not respond in a timely manner to commands from the 9010A. Provision is made in SET-UP to change the pod timeout. Select YES, then enter a greater timeout number with 60,000 being the maximum timeout available.

D. UUT Power Fail

This message can occur both during pod self test or during operation with a UUT. It means that the power supply at the UUT microprocessor socket is out of tolerance and the pod is not communicating with the 9010A mainframe. Check first to be sure the pod cable is plugged firmly into the 9010A. During self test, be sure the microprocessor plug is tightly held in by the pod self test ZIF socket. It is possible the thumbwheel was not properly tightened and has come loose. It' this message appears during UUT operation, it means that the power supply is out of tolerance at the UUT processor socket and the pod is not communicating with the 9OlOA. The UUT should be checked for broken power traces, and bad connections. Then, follow the procedure for POD TIMEOUT above. If the pod cable is properly plugged into the 9010A and the pod UUT cable is securely plugged into the UUT, then the "UUT POWER FAIL" message indicates that the UUT microprocessor clock circuit is not working due to a bad UUT power supply. Note that the UUT power fail message cannot be disabled in SET-UP.

E. Bad Power Supply

The 9010A constantly monitors the UUT's power to within a 10% window. If the power supplied to the processor does not fall within this window, the 9010A will halt and display this message. First the UUT should be checked to determine whether a problem exists or whether this is the way the UUT has been designed. (The UUT may be designed to run with a low Vcc.) If this is the UUT design, the 9010A can be made to stop monitoring UUT power through the SET-UP mode. One of the menu selections asks if you want to trap on a bad power supply. Selection of NO will now stop the 9010A from monitoring the UUT's processor power. Note that SET-UP cannot be used to disable the UUT power fail message.

F. Active Forcing Line

Often times UUT's are designed with watchdog timers or some other form of reset circuitry which continually try to force the processor into a certain state. If this circuitry affects only the processor, it can be disabled through the set up commands as described in section IF. If this circuitry affects other devices on the UUT such as the ROM or RAM, then the circuit must be disabled by tying it either high or low. In tying forcing lines high or low, only one at a time should be manipulated. If, after tying the first line, the UUT and 9010A work together, do not tie any other lines. These lines often are used to add wait states and if disabled, the UUT may not function properly.

G. Active Interrupts

When an interrupt occurs, the 9010A tells you that this has happened. It is possible that the UUT has interrupts pending all the time. In order for the 9010A to successfully interact with the UUT, these interrupts must be ignored. A menu selection in the set up mode allows the 9010A to disregard all pending interrupts. The selection is SET - TRAP ACTIVE INTERRUPT? Selection of NO will now allow the 9010A and UUT to function compatibly.

H. Control Error

The control error message indicates a faulty UUT control line. One or more of the control lines are not properly drivable. included in the message are the faulty bits. This information can then be correlated with the decal on the pod case describing which bit is which control line. From here the UUT must be inspected to determine

the cause of the drivability problem.

I. Address Bit Tied

Address bits may be tied high, low, or together. The full text of the message will describe the particular situation and which lines are affected. Those lines must then be traced on the UUT until the situation causing those lines to be faulty is found.

J. Data Bit Tied

Data bits may be tied high, low, or together. The full text of the message will describe the particular situation and which lines are affected. Those lines must then be traced on the UUT until the situation causing those lines to be faulty is found.

III. Learn

At this point, the 9010A should be plugged into a known good UUT and the BUS TEST should have come back with a message OK. LEARN can now be properly executed to provide documentation for the UUT.

A. Learn Fail

When an error occurs during LEARN, the 9010A logs that fact. The operator may attempt to troubleshoot the error or continue with the LEARN. If LEARN is continued, the display LEARN FAIL comes up as a reminder of the failure during the learn process. This message does not mean that the attempted LEARN was faulty, only that a driveability error of some kind occurred. However, if a failure occurs during the LEARN operation, LEARN parameters may be incorrect.

B. Fatal Abort

LEARN has a finite amount of memory space in which to store its descriptors. (It can store up to 100 descriptors.) In the very rare case when the allocated memory space is depleted, LEARN stops with the message FATAL ABORT. The user may be able to accomplish a successful LEARN by selectively LEARNing sections of address space, or the information may be entered manually using the VIEW function.

IV. View

Once LEARN is complete, the VIEW keys can he used to look at the information which was acquired during the LEARN process. Remember that LEARN often acquires many lines of information. If the MORE annunciator is flashing, select the MORE key for the next line of information.

A. Finding Nothing

Sometimes UUT's are designed with energy-saving switches to turn off power to memory devices on the board when not in use. In some cases, the power switch may be controlled by an I/O port requiring a certain value to be written out using the WRITE key.

B. Finding Many Small Sections of I/O

When LEARN is interfered with, strange results can occur. If the UUT has a watchdog timer that is connected to the RAM and not disabled, LEARN will see many small sections of I/O. In this case, UUT documentation should be checked for timers and reset circuitry.

C. Does Not Find All I/O Locations

LEARN is limited in its ability to find all I/O locations. Only those locations with at least one bit read/writeable will be found. Therefore, read only I/O, and write only I/O will be missed. If UUT documentation exists, these locations may be tested manually.

D. False ROM

Occasionally, a PIA or PIO will power up in a strange mode on a UUT. When this occurs, LEARN will see those locations as read-only locations and report them as ROM. The VIEW function can be used to deliminatc any extraneous descriptors (CLEAR).

V. Preprogrammed Tests

Upon completion of LEARN, the necessary address parameters are stored in the 9010A's memory for the preprogrammed tests. Any test selection and ENTER will perform that test over the address ranges stored. If an error occurs, the 9010A will halt and inform the user of the UUT error. For more extensive information, bee section 4H of the 9010A Operator's Manual.

A. Control Error

A control error indicates the 9010A could not successfully drive one or more of the control lines of the UUT. Indicated in the

message are those bits not properly drivable. This information can be directly correlated to those lines affected using the decal on the pod case. Now the probe and UUT schematic can be used to isolate the fault.

B. Address Error

An address error indicates the 9010A could not successfully drive one or more of the address lines of the UUT. Indicated in the message are those bits tied high, tied low, or tied together. Now the probe and UUT schematic can be used to isolate the fault.

C. Data Error

A data error indicates the 9010A could not successfully drive one or more of the data lines of the UUT. Indicated in the message are those data bits tied high, tied low, or tied together. Now the probe and UUT schematic can be used to isolate the fault.

D. Read/Write Error

The RAM test checks for the read/writeability of all RAM locations. The I/O test also checks for the read/writeability of specified bits for the I/O locations. If one of those bits is not read/writeable the 9010A displays the error along with the faulty bit or bits. Now the probe and UUT schematic can be used to isolate the fault.

E. RAM Bits Tied

When a RAM test finds two data lines tied within the RAM itself or up to the output side of a buffer this error message along with the bits at fault is displayed. These bits in turn can be translated into the faulty lines. Now the RAM can be replaced or the probe can be used to track down the error.

F. RAM Decode Error

When a RAM test finds address lines that are not decodeable such as from an open line or lines tied together, this error message along with the bits at fault is displayed. These bits in turn can be translated into the faulty lines. Now the RAM can be replaced or the probe can be used to track down the error.

G. RAM Pattern Error

A RAM pattern error detects a soft RAM failure. This indicates a pattern sensitive area within the RAM. Replacement of the RAM chip indicated by the address contained in the error display will usually solve the problem.

H. ROM Error

ROM test calculates a signature for the ROM addresses specified and compares it against the signature stored during the LEARN. If these unique signatures do not exactly match, the 9010A flags this as an error. The most likely causes are data lines tied between the buffers and the ROM's, or the ROM's themselves have gone bad. Replacing the ROM's or tracing with the probe should find the fault.

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