Synertek.

SY2159

1024 x 8 Static Random Access Memory

Features

- 120nsec Maximum Access Time
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access: 50 ns Max.
- Identical Cycle and Access Times
- Single +5V Supply (± 10%)
- Pin Compatible with 2716 16K EPROM
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- Output Enable Function ($\overline{OE}$)

Description

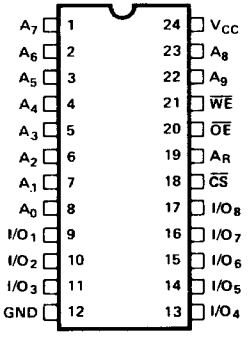
The Synertek SY2159 is s 8192 bit static Random Access Memory organized 1024 words by eight bits and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus.

The SY2159 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

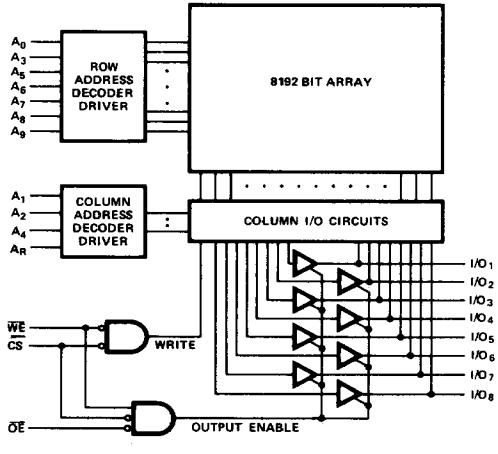
The SY2159 is offered in two versions. For the "A" version, the select reference input (A_R) must be at V_{IL} and for the "B" version, A_R must be at V_{IH}.

The SY2159 is pin compatible with 16K ROMs, EPROMs, and E^2PROMs thus offering the user the flexibility of switching between RAM, ROM, EPROM and E^2 with a minimum of board layout changes.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5V to +7V
Power Dissipation 1.0W
Electrostatic Discharge Rating (ESD)**
Inputs to Ground ..... ±2000V

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**Test Condition: MIL-STD-883B Method 3015.1

D.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	2159-2/-3/-4 Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$\overline{CS} = V_{IH}$, V_{CC} = Max, V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		95	mA	$T_A = 25°C$; V_{CC} = Max, $\overline{CS} = V_{IL}$
			100	mA	$T_A = 0°C$; Outputs Open
V_{IL}	Input Low Voltage	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1.0 mA

Capacitance

$T_A = 25°C$, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 5)

READ CYCLE

Symbol	Parameter	2159-2 Min.	2159-2 Max.	2159-3 Min.	2159-3 Max.	2159-4 Min.	2159-4 Max.	Unit	Conditions
t_{RC}	Read Cycle Time	120		150		200		ns	
t_{AA}	Address Access Time		120		150		200	ns	
t_{ACS}	Chip Select Access Time		50		60		70	ns	
t_{AOE}	Output Enable Access Time		50		60		70	ns	
t_{OH}	Output Hold from Address Change	10		10		10		ns	
t_{LZ}	Output Low Z Time	10		10		10		ns	Note 4
t_{HZ}	Output High Z Time	0	40	0	50	0	60	ns	Note 4

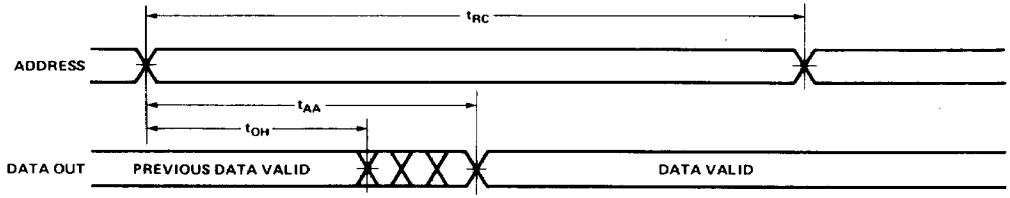
WRITE CYCLE

t_{WC}	Write Cycle Time	120		150		200		ns	
t_{CW}	Chip Select to End of Write	70		90		120		ns	
t_{AW}	Address Valid to End of Write	90		120		150		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	70		90		120		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DW}	Data Valid to End of Write	50		70		90		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	40	0	50	0	60	ns	Note 4
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 4

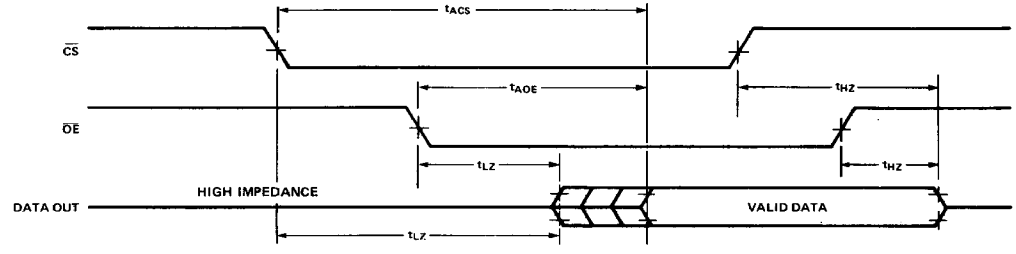
(See following page for notes)

Timing Diagrams

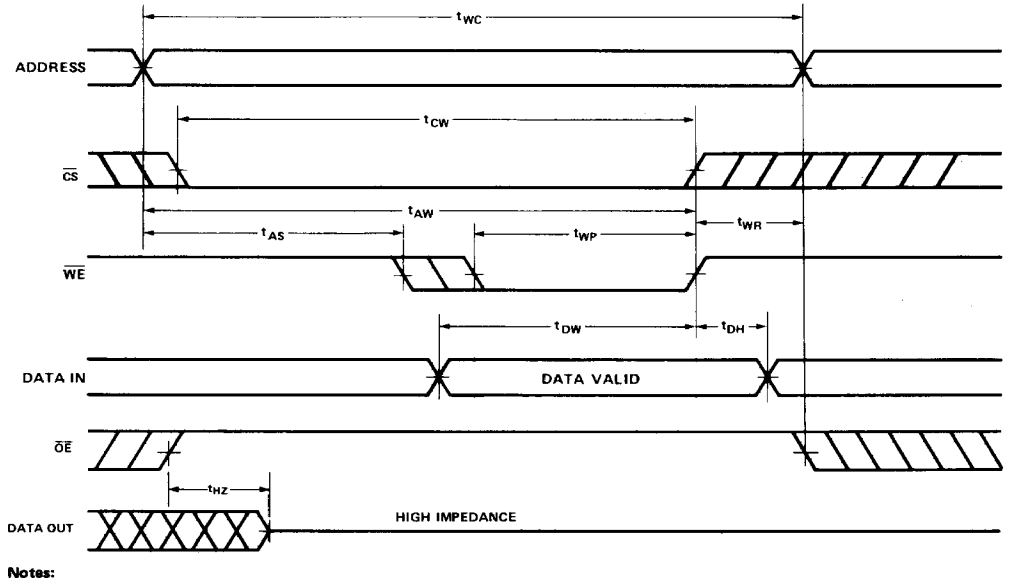
READ CYCLE NO. 1 (NOTES 1 and 2)



READ CYCLE NO. 2 (NOTE 1)



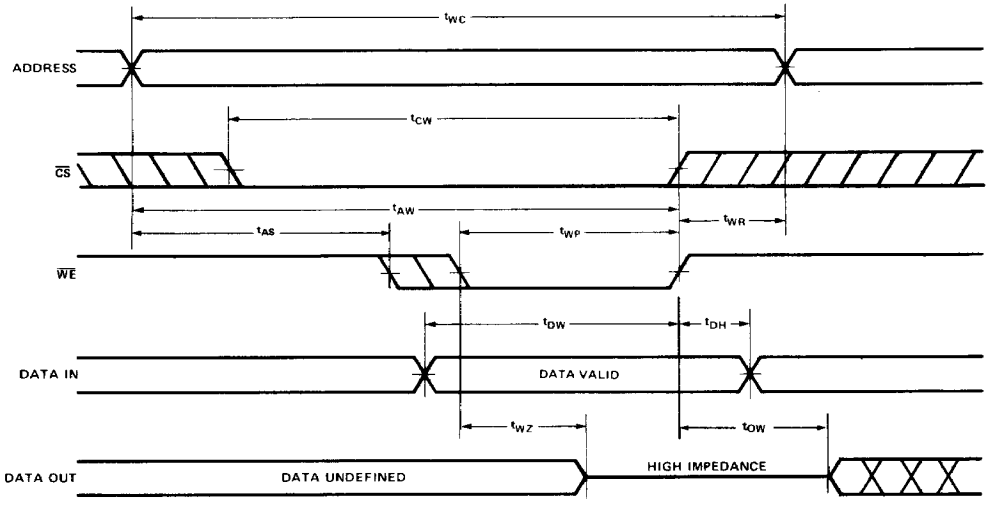
WRITE CYCLE NO. 1 (NOTE 3)



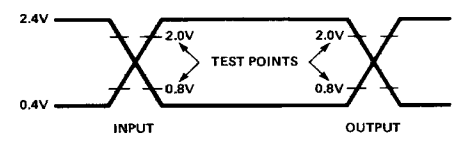
Notes:

1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS}$ = $\overline{OE}$ = V_{IL}.
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, hte outputs remain in the high impedance state.
4. Transition is measured ± 500 mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
5. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{OE}$ + V_{IL}) (NOTE 3)

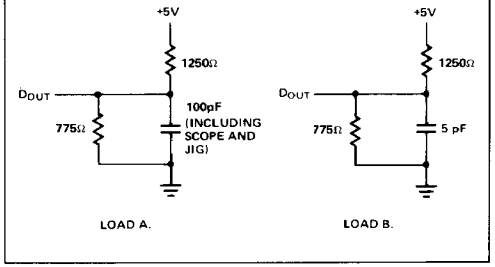


A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability 24 Pin Plastic

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Package Type	A_R
SYP2159A-2	120ns	100mA	Plastic	V_{IL}
SYP2159A-3	150ns	100mA	Plastic	V_{IL}
SYP2159A-4	200ns	100mA	Plastic	V_{IL}
SYP2159B-2	120ns	100mA	Plastic	V_{IH}
SYP2159B-3	150ns	100mA	Plastic	V_{IH}
SYP2159B-4	200ns	100mA	Plastic	V_{IH}