SERVICE MANUAL

SOLID STATE PINBALL GAMES

D. Gottlieb & Co.
A Columbia Pictures Industries Company

Designers and Manufacturers of Amusement Machines since 1927
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D. Gottlieb & Co.

System 80
Service Manual

SECTION I

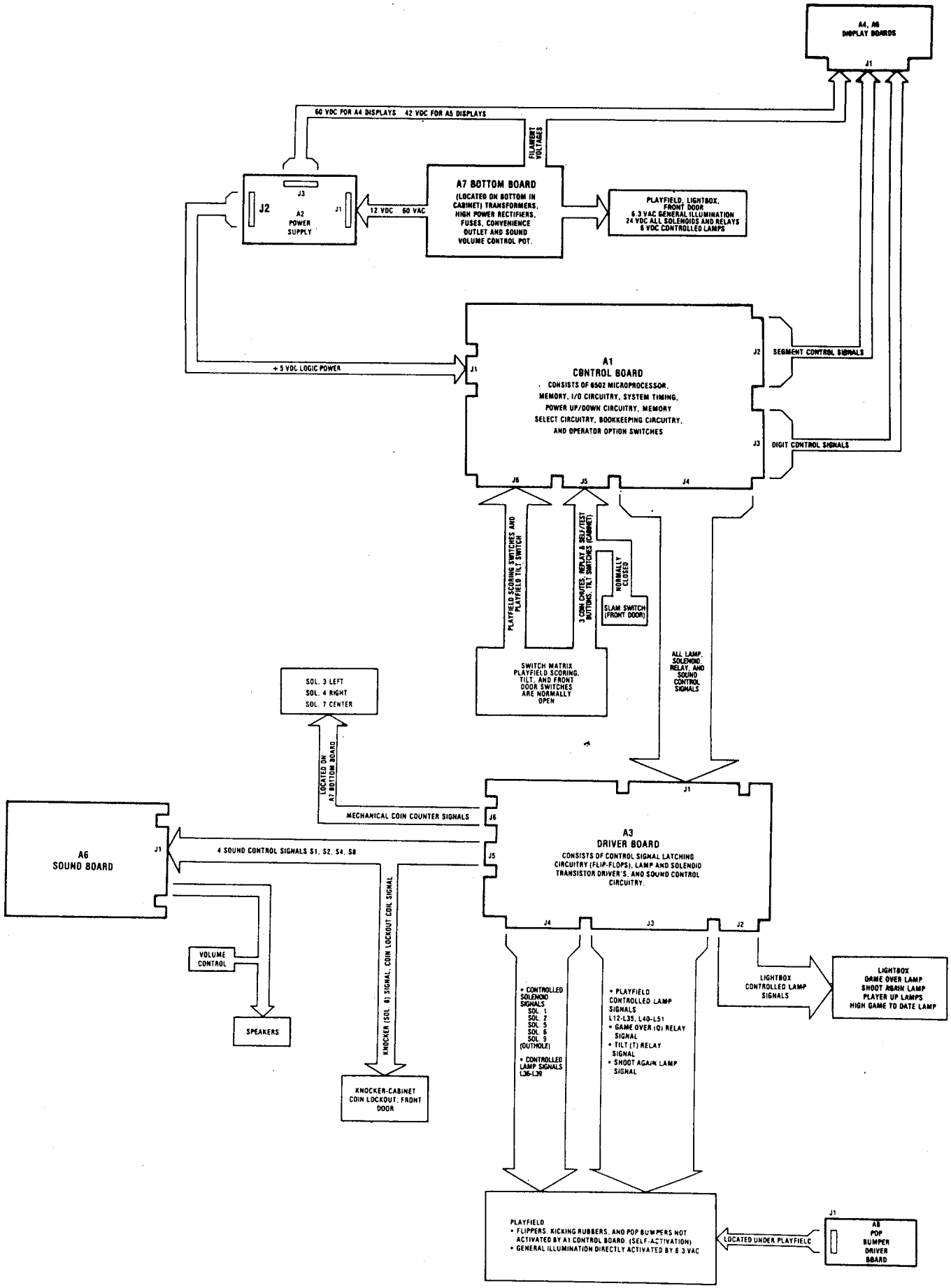
SYSTEM 80 OPERATION

The block diagram following depicts System 80 in its entirety. The A1 Control Board is the "brain" of the system, monitoring switch matrix and slam switch inputs (via connectors J5 and J6). It also issues the appropriate output control signals as determined by the system programming located in the ROM, RAM, and PROM memory chips. Output control signals exit the A1 Control Board through connectors J2, J3, and J4. Connectors J2 and J3 provide segment and digit control signals respectively to all display boards. Connector J4 provides all lamp, solenoid, relay and sound control signals to the A3 Driver Board.

The A3 Driver Board accepts all incoming control signals through connector J1. Incoming signals activate the appropriate power transistors to turn lamps and relays on or off and to pulse solenoids within the game. Sound control signals are inverted and transmitted to the A6 Sound Board. Output signals at connectors J2, J3, J4, J5, J6 are distributed as labeled in the System 80 Block Diagram.

Transformers and rectifiers on the Bottom Board convert the AC line voltage to specific A.C. and D.C. voltage levels. The Power Supply regulates voltage for the system logic components and the displays. Refer to the System 80 Power Distribution schematic in Section V.

The Pop Bumper Driver Boards are used to amplify and condition trigger signals to activate the pop bumpers and to protect pop bumper coils in case a switch should stick closed.



SYSTEM 80 BLOCK DIAGRAM

SECTION II

SERVICE AND REPAIR

A. GAME CHECK-OUT PROCEDURE

1. Preliminary checks
   a. Line cord into properly grounded outlet.
   b. All connectors in proper position and secure.
   c. TILT switches properly adjusted (normally open).
   d. SLAM switch properly adjusted (normally closed).
2. Power-on check—Turn ON-OFF switch ON.
   a. General illumination lamps turn on.
   b. LEDs on power supply are on.
   c. After five seconds, TILT and GAME OVER relays energize momentarily, then release.
   d. Score Displays come on all zeroes.
   e. Coin lockout coil energizes.
3. Self-test checks
   a. Press play-test switch (inside of front door).
      NOTE: If play-test switch is pressed a second time the game will advance to Step #1. To bypass the 15 bookkeeping steps and advance directly to the self-test, press the credit button after pressing the play-test switch.
   b. Check information and score levels in Steps 1-15.
   c. Check that the credit button will reset and increment score settings.
   d. Observe controlled lamps, relays, and coin lockout in self-test Step 16.
   e. Observe controlled solenoids in self-test Step 17.
   f. Observe any closed switch indications in self-test Step 18.
   g. Observe displays in self-test Step 19.
   h. Turn game off, then on; repeat steps a through c to check battery condition.
   i. Advance to self-test Step 20 and observe player 1 display for indication of any faulty memory devices.
4. Coin chute checks
   a. Check each coin chute for proper operation.
      NOTE: Refer to game manual for control board switch settings which regulate coin chutes.
   b. Check optional coin meters, if installed, for proper operation.

5. Game set-up sequence check
   a. Press credit button to start game.
   b. Observe credit button tune is played.
      NOTE: Selectable with control board switch.
   c. Observe single flashing zero on player 1 display, other score displays blank.
      Credits decrease by 1 on credit display.
      Ball-in-play displayed as ball #1.
   d. Observe GAME OVER relay is energized.
   e. Observe ball is kicked from outhole.
   f. Observe that playfield features reset.
6. Game feature check
   a. Manually close each playfield switch to check proper operation. Observe correct scoring and feature control.
   b. Close TILT switch and observe TILT indication. Close outhole switch and observe that TILT is cleared.
   c. Open SLAM switch and observe SLAM indication followed by game-over condition.

B. GAME TROUBLESHOOTING GUIDE

1. General Troubleshooting Suggestions
   To simplify the following troubleshooting charts, those checks which should always be performed when servicing a problem are listed below. These include voltage checks and verification of fuse condition.
   a. Check SLAM switch . . . There is one **normally closed** anti-cheat or SLAM switch on each game. That switch is on the front door and must have adequate tension to prevent normal vibration levels causing it to open.
   b. Check TILT switches . . . There are three **normally open** TILT switches on each game. One is on the playboard, a second is the pendulum bob assembly and the third is the ball roll switch. These switches must be adjusted properly to prevent normal vibration levels causing them to close.
   c. Check power supply outputs . . . Anytime the troubleshooting guide indicates this, check the output with the output cables removed from the power supply. Also check the inputs to the power supply before assuming it is defective because of an incorrect output.
   d. Check bottom board fuses . . . The bottom board fuses control specific parts of the game and should always be checked early in the troubleshooting procedure.

e. Check playfield fuses . . . The number of fuses and their values will change between game models.

f. Check cable connections . . . Always check for secure cable connections both at the various printed circuit boards and at the cable junctions throughout the game.

2. General Game Problems

SYMPTOM Game fails to power up when turned on.

NOTE: This is a general description of a problem which may have a variety of symptoms—anytime the game does not power up as it should, make the indicated checks.

CHECK

1. Inspect all connectors for proper position and secure connection.
2. Check bottom board fuses.
3. Check + 5VDC power supply output.
4. Check + 60VDC power supply output.
5. Check that the PROM(s) are installed properly.
6. If power supply voltages are normal, replace control board; if not, check power supply input voltages, and if necessary replace power supply.

SYMPTOM Game does not delay when turned on. Score displays come on immediately and status display is dark.

CHECK

1. Check SLAM switch.
2. Check TILT switches.
3. Check that coin lockout wireform is not grounding coin chute switches.
4. Check control board connector A1-J5 for security.
5. Replace control board.

SYMPTOM PLAY/TEST switch fails to start test sequence.

CHECK

1. Check SLAM switch.
2. Check TILT switches.
3. Check PLAY/TEST switch continuity.
4. Check PLAY/TEST switch isolation diode on bottom board.
5. Replace control board.

3. Display Problems

SYMPTOM One or more segments always on or always off.
CAUTION: ALWAYS TURN POWER OFF BEFORE REMOVING CONNECTORS FROM BOARDS.

CHECK
1. If problem appears on one display only, replace that display board.
2. If problem is common to more than one display, check wiring between displays and control board. Unplug display boards one at a time; if problem clears up on other displays, replace defective display board.
3. Replace control board.

SYMPTOM One or more digits always on or always off.

CHECK
1. Follow procedure for segment failure.

SYMPTOM ALL displays off.

CHECK
1. Check 60 VAC fuse on bottom board.
2. Check + 60 VDC output at power supply.
3. Replace control board.

SYMPTOM Score displays all off; status display OK.

CHECK
1. Check 5VAC at the displays.
2. Check + 8VDC output of power supply.
3. Check + 8VDC at center tap of bottom board transformer.
4. Check + 60VDC output of power supply. Excessive load or a zener short on the power supply + 42VDC output could cause this indication.

SYMPTOM Status display off, score displays OK.

CHECK
1. Check 3VAC at the display.
2. Check + 42VDC output of power supply.
3. Check + 5VDC at center tap of bottom board transformer.
4. Check setting of control board switches 18 and 28.
5. Replace status display.

SYMPTOM Data in bookkeeping steps 1-15 is incorrect or absent.
NOTE: A flashing number in steps 1-10 or 15 indicates the number **may** be incorrect.

CHECK

1. While in malfunctioning step, press credit button on front door to enter all zeroes, then advance to next step.
2. If step 11-14 is incorrect, reset to zero, then hold credit button in to increment score level before advancing to next step. If steps 11-14 change in value, a default value from the game PROM will automatically be entered to replace the lost data.
3. If data will not reset to zero, or if new score levels cannot be entered, replace control board.
4. After resetting incorrect steps, turn game off, then back on and examine data again. If data was retained, no problem exists. If not, replace control board.

SYMPTOM Coin chutes fail to operate correctly.

CHECK

1. REFER to "SWITCH PROBLEMS".

SYMPTOM Game fails to set up correctly when credit button is pressed.

CHECK

1. REFER to "SWITCH PROBLEMS".

SYMPTOM Intermittent game problems which are not listed elsewhere. (e.g., goes to GAME-OVER at random, faulty credit information, erratic game feature operation.

CHECK

1. Check for presence of diodes across **ALL** solenoid coils. Also check for loose or cold solder joints on diode connections to coils, check diodes are not internally open circuited.
2. Check that game is properly grounded.
3. Check that the PROM(s) are firmly inserted in socket.
4. Check 12VDC bridge and filter capacitor on bottom board.
5. Replace line filter on bottom board.
6. Check 5VDC adjustment on power supply.

4. Controlled Lamp Problems

SYMPTOM One or more lamps fail to operate or remain on all the time.

CHECK
1. Check bulbs of problem lamps.
2. Check sockets and wiring of problem lamps. Return ground wires are common to groups of lamp driver transistors on the driver board.
3. Replace driver board.
4. Replace control board.

SYMPTOM ALL controlled lamps on playfield fail to operate.

CHECK
1. Check fuse for + 6VDC rectifier on bottom board.
2. Check output of + 6VDC rectifier on bottom board.
3. Check TILT relay switch adjustment.
4. Check all driver board cable connections.
5. Replace driver board.
6. Replace control board.

5. Controlled Solenoid Problems

REMINDER: NOT ALL GAME SOLENOIDS ARE CONTROLLED BY THE ELECTRONICS. DETERMINE FIRST IF THE PROBLEM SOLENOID IS CONTROLLED OR NOT.

SYMPTOM ALL controlled solenoids inoperative.

CHECK
1. Check fuse for + 24VDC rectifier on bottom board.
2. Check output of + 24VDC rectifier.
3. Check for presence of + 24VDC at any controlled solenoid. If missing, check cable connections to driver board and playfield.
4. Replace driver board.
5. Replace control board.

SYMPTOM One or more (but not all) controlled solenoids fail to operate or remain energized all the time.

NOTE: DO NOT PERMIT MORE THAN 10 SECONDS CONTINUOUS OPERATION OF ANY COIL.

CHECK
1. Check coils of problem solenoids.
2. Check diodes on problem solenoids.
3. Check individual playboard solenoid fuses.
4. Replace driver board.
5. Replace control board.

6. Switch Problems

CAUTION!!! TURN POWER OFF BEFORE MAKING ANY SWITCH ADJUSTMENTS.
DO NOT FILE OR BURNISH GOLD PLATED SWITCH CONTACTS.

SYMPTOM Self-Test STEP 18 indicates one or more closed switches.

CHECK
1. Refer to appropriate game manual to determine location of indicated switches. Clean and adjust as required.
2. Replace control board.

SYMPTOM Coin chute switch fails to operate or gives incorrect response.

CHECK
1. Check coin chute switch adjustment.
2. Check switch isolation diodes on bottom board.
3. Check that coin lockout wireform is not grounding coin chute switch.
4. Check option switches on control board. Refer to game manual for correct settings.
5. Replace control board.

SYMPTOM One or more playboard switches fail to operate.

CHECK
1. Check switch adjustment.
2. Check isolation diodes on playboard terminal strips.
3. Check cable connections between playboard and control board.
4. Check for strobe or return lines shorted to ground.
5. Replace control board.

SYMPTOM One or more playboard switches gives incorrect response.

CHECK
1. Check for shorted strobe and return lines.
2. Check for shorted isolation diodes on playboard.
3. Replace PROM.
4. Replace control board.

7. Sound Board Problems.

NOTE: Self-test switch on the sound board generates an output **only** if option switches S1 and S2 on the sound board are in opposing positions.

SYMPTOM No sound.

CHECK
1. Check control board option switches S25, 26, and 27 for proper setting.
2. Check volume control setting on bottom board.
3. Check sound board fuse on bottom board.
4. Check + 5VDC, + 12VDC, and − 12VDC on sound board.
5. Measure 8 ohms across speaker terminals.
6. Replace sound board.

SYMPTOM Distorted sound.

CHECK
1. Check sound board fuse on bottom board.
2. Check speaker for tears in cone, measure 8 ohms across speaker terminals.
3. Replace sound board.

SYMPTOM Wrong tunes played.

CHECK
1. Check setting of sound board option switches.
2. Check S1, S2, S4, and S8 inputs to the sound board. All lines should pulse when sounds are triggered.
3. Replace sound board.
4. Replace driver board.
5. Replace control board.

8. Pop Bumper fails to operate.

SYMPTOM Coil never energizes.

CHECK
1. Check fuses under playfield.
2. Check adjustment of pop bumper cup switch. Switch must be open. then close and reopen.
3. Check coil and diode.
4. Replace pop bumper driver board located under the playfield.

SECTION III

THEORY OF OPERATION

A. CONTROL BOARD

System 80 is built around a Rockwell 6502 microprocessor which operates on a single 5VDC supply voltage. A brief description of each LSI component follows, which makes the entire system easier to understand.

The Rockwell 6502 is an 8-bit microprocessor which has many positive features: single supply voltage, full 16-bit address bus, two levels of interrupt priorities, and a two-phase clock which is generated onboard.

The microprocessor receives instructions off the data bus from peripheral devices; RAM, ROM, and PROM. It is an 8-bit bus, DB0-DB7, with the data being transferred while the $\phi 2$ clock is high. Addressing for all external memory is output from the microprocessor on the 16 address bus lines, AB0-AB15. In this particular application, AB14 and AB15 are not used. AB0 through AB6 are applied directly to the address bus, AB7 through AB13 are applied to the bus, however are also combined through various gating combinations for PROM select, RAM select, RIOT enable, etc. These lines are buffered by Z7 and Z10 since they are capable of driving only one TTL load each.

The microprocessor receives a clock signal on pin 37, ϕ_0 (IN) from Z2, pin 9. The clock signal is converted into a two-phase system clock internally and is output on pin 39, ϕ_2 (OUT) to other devices which require system timing.

The reset line, $\overline{RES}$, pin 40, is held low when power is first applied. Once V_{cc} reaches a level determined by the reset hardware, $\overline{RES}$ goes high and remains high as long as power remains on. This reset insures that as the microprocessor starts to operate the program counter is initialized to zero, and execution of the program begins at the proper address.

Interrupt request, $\overline{IRQ}$, pin 4, receives low going signals from the three RIOT devices when an interrupt needs to be serviced. The microprocessor then completes its current instruction and goes directly to the designated interrupt routine. The non-maskable interrupt, $\overline{NMI}$, is not used and is tied high through R10.

Read/Write control, pin 34, determines whether data on the bus is read from RAM or written into RAM. This signal is high to read, low to write, and goes to the three RIOT devices and the bookkeeping RAM.

All input-output functions of the microprocessor are handled by R6532 RAM INPUT-OUTPUT TIMER devices (RIOT). Each RIOT contains two 8-bit bidirectional data ports which can be used to transmit data from the microprocessor system to external circuitry or to receive data from external circuits and enter it into the microprocessor. The I/O lines are directly compatible with TTL or CMOS devices. Each line is capable of driving one TTL load.

Each RIOT also contains 1024 bits of RAM memory in a 128 x 8 configuration. Addressing is accomplished through the seven address lines, A0 to A6. $\overline{RS}$, pin 36, must be low for the RAM section to be enabled. When the READ/WRITE line, pin 35, is high, the RAM is in the read mode. When R/W is low, the RAM is in the write mode.

Two chip select lines CS1 and $\overline{CS2}$ are provided as enable lines for the RIOT. CS1 must be high and $\overline{CS2}$ must be low for the RIOT to be enabled. A reset input, $\overline{RES}$, pin 34, must be held low as the system is initialized to zero all internal registers and to prevent false data from being transferred out of the system during power up. Once the microprocessor has initialized, the $\overline{RES}$ line should go high and remain high.

The interrupt request line, IRQ, pin 25, is normally high and goes low whenever the RIOT wants to transmit an interrupt to the microprocessor.

System timing is maintained by the $\phi 2$ clock which enters the RIOT at pin 39. All data transfers on the bus take place when $\phi 2$ is high.

One RIOT, U5, uses I/O port PA7 as an edge triggered interrupt for the slam switch input. This gives the slam switch a higher priority than other input functions.

Two ROMs, U2 and U3, each contain 32K bits of memory in a 4K x 8 configuration. This is 'background' memory and does not change from game to game. Addressing is received from the microprocessor and data is read directly onto the data bus. The S2 input, pin 21, is used to select which of the two ROMs is enabled at any given time.

Data which must be retained when the game is turned off is stored in Z5, a P5101 CMOS RAM. The 5101 is a 256 x 4 RAM with low power consumption when the CE2 line, pin 17 is low. Since the 5101 is a 4-bit RAM, it is connected only to the lower four data bus lines, DB0 through DB3. Addressing is provided directly off the address bus from the microprocessor.

The other type of memory used is the programmable ROM (PROM) which is changed from game to game. The PROM is a 4K device with a 512 x 8 configuration. Address and data information is transferred on the microprocessor bus system. Chip Select 4, pin 18, is used as the PROM SELECT to determine which of the two PROMs is enabled at any given time.

The remaining circuitry on the control board is standard TTL and CMOS. It is used primarily to buffer all inputs and outputs from the microprocessor to the external areas of the game. This prevents most external failures in the game from damaging any of the LSI devices.

B. DRIVER BOARD

The driver board provides the necessary output interfacing to the playfield and other controlled devices in the game. It consists of three types of driving circuits; lamps, solenoids, and sound board. Inputs to the board are on connector J1 and outputs are on connectors J2 through J6.

The sound board is driven by four sections of Z13, a 7404 hex inverter. Input signals are simply inverted and routed to the sound board through connector J5.

The solenoid driver section of the driver board receives positive pulses from the control board. These pulses are applied to the base of each driver transistor through a 1N4148 diode. Each pulse causes the transistor to turn on, completing a circuit from the collector to the emitter.

Three high current solenoids are driven by using transistor pairs. The pulse from the control board turns on an MPS-U45 causing the emitter to go high. This turns on the 2N3055, which energizes the solenoid. The 1N4148 diodes protect the control board from damage in the event of transistor failure.

The remainder of the driver board is dedicated to the lamp driver circuits. The 12 integrated circuits are 74175 D-type flip-flops which are used as 4-bit latches. Each of the four lamp data lines, LD1 through LD4, is applied to all 12 integrated circuits through connector J1. There are also 12 data strobe lines, DS1 through DS12, one of which is applied to the clock input of each integrated circuit. Each time a DS line is pulsed high, the data on the LD lines at that instant is latched into that integrated circuit and is transferred to the Q outputs.

On integrated circuit Z12, both the Q and $\overline{Q}$ outputs are used which allows four sets of lamps to be alternated.

C. POWER SUPPLY

The power supply consists of two separate circuits which share a common ground. The high voltage section has a 60VAC input and outputs 60VDC and 42VDC. The low voltage section has a 12VDC input and outputs 5VDC and 8VDC.

Diodes CR1 through CR4 form a bridge rectifier which is supplied 60VAC through connector A2-J1, pins 7 & 8. The negative side of the bridge is grounded and the positive side output is filtered by capacitor C1. This filtered DC is applied to pass transistor Q1. Voltage regulation is provided by zener diode CR5 and resistor R1. Current regulation is provided by R4 and Q2. If too much current is drawn through R4, the voltage across it increases, turning on Q2. Q2 then lowers the voltage on the base of Q1, turning it off and decreasing available current to R4.

The 42VDC is generated from the 60VDC by zener diode CR6 and resistor R5.

A bridge rectifier and filter capacitor on the bottom board supply 12VDC to the low voltage section of the power supply through connector A2-J1, pin 1. LED 1 indicates that the input DC is present on the power supply. The current limiting circuit consists of R8, R9, and R12. Excessive current causes the voltage across R12 to increase which increases the voltage between the current sense and limit pins, 2 & 3, of the regulator. The output of the regulator on pin 10 then decreases. Voltage adjustment is provided by R7, R14, and the potentiometer.

A portion of the reference voltage from regulator pin 6 is returned to the non-inverting input, pin 5, depending on the adjustment of the potentiometer. This establishes the output voltage. Voltage stability is maintained by applying a portion of the output voltage to the regulator inverting input, pin 4. As this voltage falls, the regulator will increase its output to bring the voltage back up.

High frequency input to output oscillations are prevented by capacitor C3.

Overvoltage protection is provided by CR8 and SCR1.

The display offset voltage, 8VDC, is generated by CR7 and R10.

LED 2 indicates an output voltage is present on the 5VDC output circuit.

NOTE: LED 2 is a relative indicator and is not intended to indicate the proper adjustment of the 5VDC output.

D. DISPLAY BOARDS

Two different display boards are used in the game. Six-digit displays are used in the player score positions and a four-digit display is used as a status display. The status display indicates credits and ball-in-play during a game, and credits and a match number in game-over. It is also used in the bookkeeping and self-test modes.

All display boards incorporate a Futaba display module which is an evacuated glass envelope containing the physical display elements: anode segments, grids, and filaments. Before explaining the theory of operation of the two types of display boards, a description of the basic principle of operation of the fluorescent display tube is provided.

When the filament is charged with electricity and heated, electrons are emitted. If positive voltage is applied to the anode and grid under this condition, electrons emitted from the filament are accelerated into the anode after passing through the grid, excite the fluorescent substance and emit light. When anode and grid voltages are made zero or negative, the electrons do not reach the anode and no light is emitted.

The filament, which acts as a direct-heated cathode, works on AC power. This assures uniform brightness across the face of the display. To cut off the flow of electrons into the anode by means of a grid, negative voltage (with reference to the

filament) must be applied to the grid. Since the filament voltage swings negative every half-cycle, simply grounding the grid would not be sufficient to disable the display. However, if a low + DC voltage is applied to the filament in addition to the AC voltage, the filament can be held at a positive potential, and grounding the grid will then serve to disable the display. This is the purpose of the offset voltage, which is applied to the center tap of the filament supply transformer windings.

Elements corresponding to anode segments are connected in common in each display module, and voltage is applied time-sharing-wise to the designated segments. Simultaneously, voltage is applied time-sharing-wise to the grids of each digit in order. Thus only one anode segment decoder driver is required for each display board.

SIX-DIGIT DISPLAY

Each of the six digits has eight segments identified as 'a' through 'h'. Segment information is received from the control board and enters the display board at connector J1, pins 7 through 14. This information is applied to the input of Z1, and any high inputs will generate high outputs to the corresponding segments of each digit in the module. Simultaneously, the grid control information is received from the control board at connector J1, pins 1 through 6. This information is applied to the input of Z2 which functions exactly as Z1. The six grid control lines are enabled sequentially by the microprocessor, which also changes the segment information as each digit is strobed. The multiplexing rate makes it appear as if all the digits are being enabled at once.

A 10K resistor is connected between V_{DP} and a grid discharge point on the display module (GD). This prevents the build-up of a space charge around the grid which would decrease the display brightness.

For the six-digit display, V_{DP} is + 60VDC, the filament voltage is 5VAC, and the offset voltage is + 8VDC.

FOUR-DIGIT DISPLAY

The four-digit display functions exactly as the six-digit display with these exceptions: each digit has only seven segments, 'a' through 'g' and thus additional circuitry is required to enable segments 'b' and 'c' when the number 1 is to be displayed. Z1 achieves this by applying the 'h' segment information from connector J1, pin 9, to the 'b' and 'c' segment inputs of Z2.

The four-digit display does not have a grid discharge connection. V_{DP} is + 42VDC, filament voltage is 3VAC, and the offset voltage is + 5VDC.

E. SOUND BOARD

The sound board requires three supply voltages; +5VDC, +12VDC, and −12VDC. The 5VDC is generated on the power supply and is applied to the sound board through the edge connector, pin 5. The +12VDC is generated on the bottom board and is applied to the sound board through the edge connector, pin 1. The −12VDC is generated on the sound board by diodes CR1 through CR4 and is regulated by the 1N4742A zener diode.

When power is applied, pin 3 of U8 stays high for a period of time determined by R6 and C4. This generates a reset signal for the microprocessor, U1, and the RRIOT, U2. During this time the clock signal stabilizes and the system is ready to run. Once the reset signal goes high program execution begins.

Signals from the control board, which are buffered on the driver board and by U9 on the sound board, are applied to the PB ports of U2. The four lines form a binary counter which allows selection of up to 15 tunes. The PA0 to PA7 ports of U2 are the outputs from the microprocessor. These eight signals are converted to an analog, signal by the DAC, U3. The analog signal, U3, pin 4, is then decoupled by C12 and amplified by U7, an LM380. C13, C14, and C17 provide filtering.

There are two option switches and a self-test switch on the sound board. The option switches are read by PB4 and PB7 of the RRIOT. The self-test switch is the NMI of the system, and is programmed to work only if the option switches are in opposing positions.

F. POP BUMPER DRIVER BOARD

Some non-controlled solenoids on the playfield may be driven by driver boards which are mounted under the playfield. One board is used for each coil, and all of the boards are interchangeable.

When the actuating switch (such as the pop bumper cup switch) closes, it triggers the multivibrator circuit. The timed output of this circuit is inverted and buffered by the 7416 and amplified by the Darlington transistor, which provides a ground for the coil.

The coil 'on time' is controlled by the value of the timing resistor and capacitor in the 74121 circuit.

G. SYSTEM OPERATION

When 5VDC is applied to the control board, the reset signal is held low to permit initialization. This is accomplished by a three transistor delay circuit. A 10 μFd capacitor charges through a 5.6K resistor. When it charges to 2.7VDC, a 2N4400 transistor turns on. This pulls the base of the MPS-A70 low, turning it on. The collector goes high and turns on the other 2N4400 transistor. This acts as a latch to insure that the MPS-A70 stays on. A 1N4148 diode is used to discharge the capacitor so that if power is switched rapidly the circuit will still retrigger.

A power down detection circuit which will reset the system if V_{cc} falls is made up of Q1 and Z1. As V_{cc} decreases, the collector of Q1 goes low. This negative transition causes Z1 to trigger. The Q2 output goes low until Z1 times out, then returns high. This low pulse is gated to the reset circuit by Z4 and causes the microprocessor to reset.

Once V_{cc} and the reset have been established, the system clock should be running and stabilized. A 3.579545 MHz crystal, Y1, is used as a frequency standard. This frequency is divided by 4 in Z2 which gives a system operating frequency of 844.886 KHz. This operating frequency is applied to pin 37 of the microprocessor.

Display control signals (digit strobes and segment information) are output by the microprocessor through RIOT U5. I/O ports PA0 through PA3 output a 4-bit binary count which is converted to a 1 to 16 strobe by Z25. These 16 lines provide the 16 digit strobes. Segment information for the displays is output in three groups, 'A', 'B', and 'C'. Each group consists of eight lines for segments 'a' through 'h'. The number which is to be displayed appears in binary form on the PB0 through PB3 lines. This data is latched by one of three 74175 devices, depending upon which receives a clock pulse. Three clock pulses are output from the RIOT on PA4, PA5, and PA6 and need no further decoding.

Switch closures in the game are recognized by use of a switch matrix. Eight strobe signals are generated by the microprocessor and output by RIOT U4 on the PB0 through PB7 ports. The signals are then buffered and routed to both the playfield and the front door. The strobe signals are low-going pulses which repeat approximately every 10 msec. Strobe pulses return to the microprocessor on eight return lines, R0 through R7. Return signals from the control board option switches

are combined with the switch matrix returns and enter the microprocessor system through the PA0 through PA7 ports of RIOT U4. All switch closures of 10 msec. and longer are recognized and stored. A total of 15 multiple closures for each switch can be stored.

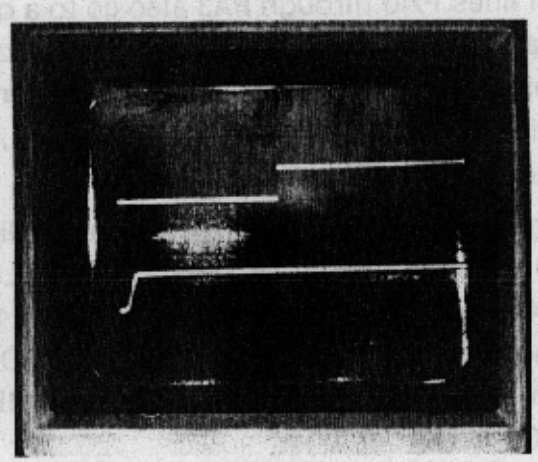
Solenoid and sound board drive signals are output by RIOT U6 on the PA0 through PA7 ports. The PA0 through PA3 outputs are buffered and combined with a sound enable signal, the PA4 output, in Z31. These outputs are then routed to the driver board. Output lines PA0 through PA3 also go to a dual 2 to 4 decoder. The A and B inputs form a two line binary input which is decoded into a 1 of 4 output. Enable signals for each section of the 2 to 4 decoder come from output ports PA5 and PA6. The outhole is driven by a discrete output, PA7, which is buffered by Z30 and routed directly to the driver board.

Lamp control signals are output by RIOT U6. Output lines PB0 through PB3 are buffered by Z32 and become the four lamp data signals, LD1 through LD4. Four additional outputs, PB4 through PB7 are decoded by a 4 to 16 decoder to provide the necessary strobe lines. In addition, DS0, DS1, DS2, and DS3 are used to strobe the control board option switches. Switch enable for the option switches comes from the PB7 output of RIOT U5.

SECTION IV
BOARD SERVICE AND REPAIR

A. CONTROL BOARD CHECKS

1. Power-on checks
   a. Power-up initialization or system reset occurs when +5VDC is applied. Figure 1 shows the Power-on (PO) signal at test connector TC1, pin 17.



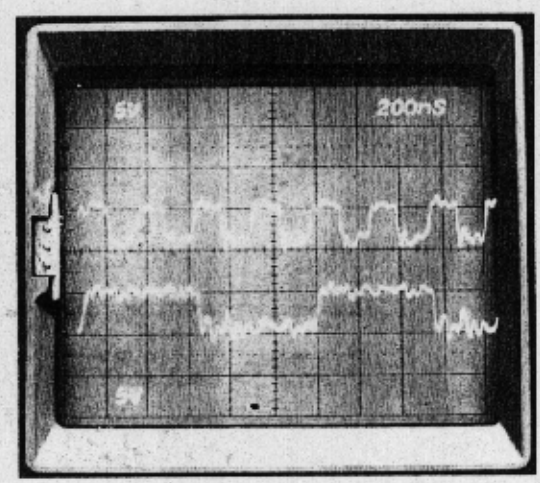
TC1 PIN 17

V = 5 Volts/Div
H = 10 msec/Div

5VDC

RESET SIGNAL
FIGURE 1

   b. Measure +5VDC ±5% at TC1, pin 7.
   c. Measure battery voltage of 3.9 to 4.1VDC at plus side of battery.
   d. Probe Z3, pin 6 and verify a square wave of 5V P-P with a period of 0.28 μ sec. See Figure 2.
   e. Verify the waveforms shown in Figure 3 at TC-1, pin 15 and TC-1, pin 11.



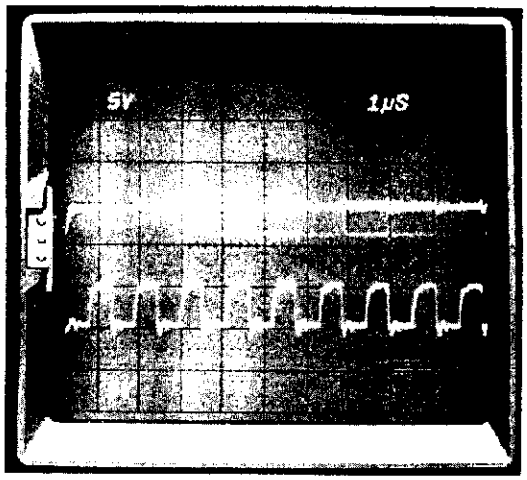
CRYSTAL OUTPUT
Z3, PIN 6

SYSTEM CLOCK
Z2, PIN 9
U1, PIN 37

SYSTEM CLOCK
FIGURE 2

f. Probe Z-1 pin 9 and verify a low going pulse when the +5VDC is turned off. This disables the static RAM during power-down.

g. Verify that the Read/Write signal at Z5 pin 20 is normally at a LOGIC 1 level except when the CPU is writing information into the RAMs or the I/O ports, whereupon the level changes to a LOGIC 0.



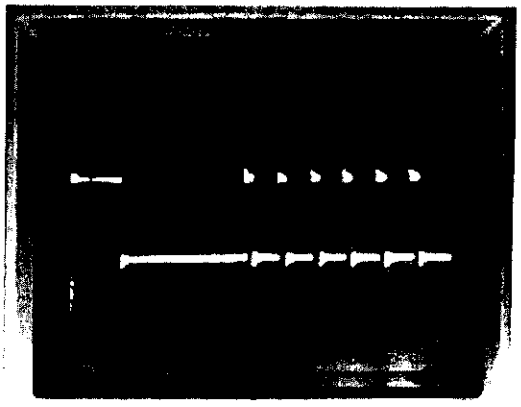
R/W TC1, PIN 11

SYSTEM CLOCK TC1, PIN 15

READ/WRITE SIGNAL

FIGURE 3

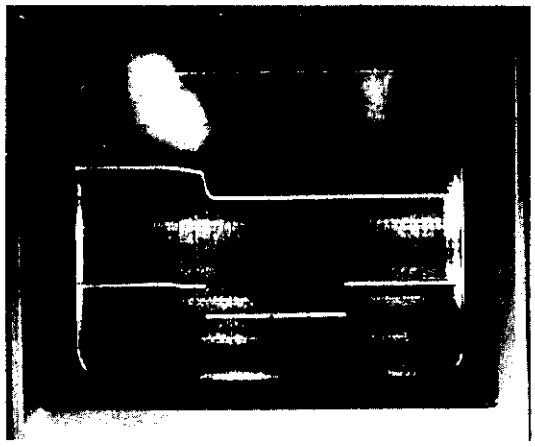
h. Verify that immediately after power is applied the RAM enable signal at Z5 pin 17 is as shown in Figure 4.



V = 2 Volts/Div.
H = 5 μsec/Div.

RAM ENABLE DURING POWER-UP

FIGURE 4



Z1, PIN 11

V = 5 V/DIV.
H = 5 ms/DIV.

Z1, PIN 9

POWER DOWN MEMORY PROTECT
FIGURE 4A

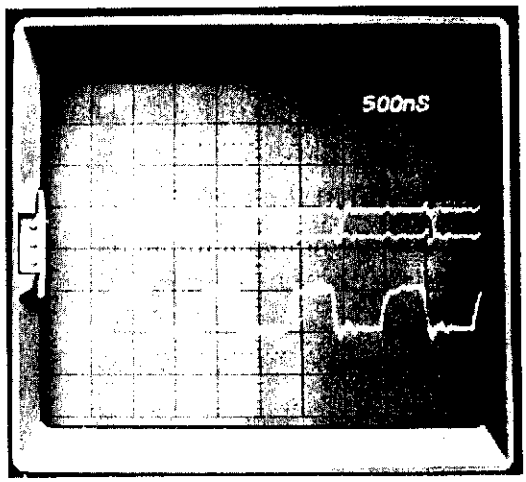
This completes the power-on checks. Turn power off and observe signals in Figure 4A for proper operation. All of the above checks should be performed before making any dynamic signal checks.

2. Dynamic Signal Checks

   a. CPU Bus Signals

      The test points listed below permit examination of the CPU bus signals between the CPU and other MOS/LSI devices. These signals occur while the program is executing in the attract mode. Address bus (AB-0 through AB-15) signals should be compared to Figure 5. Data bus lines DB-0 through DB-7 should be compared to Figure 6.

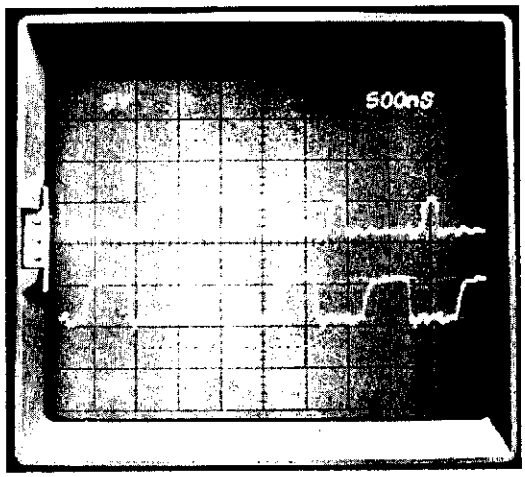
TC1 pin #	Signal
36	AB-0
37	AB-1
38	AB-2
39	AB-3
40	AB-4
31	AB-5
30	AB-6
29	AB-7
28	AB-8
27	AB-9
26	AB-10
25	AB-11
32	AB-12
33	AB-13
34	AB-14
35	AB-15
3	DB-0
4	DB-1
5	DB-2
10	DB-3
9	DB-4
8	DB-5
2	DB-6
1	DB-7
16	$\overline{IRQ}$
12	SYNC



AB-0—AB-15

CLOCK ϕ2
TC1-15

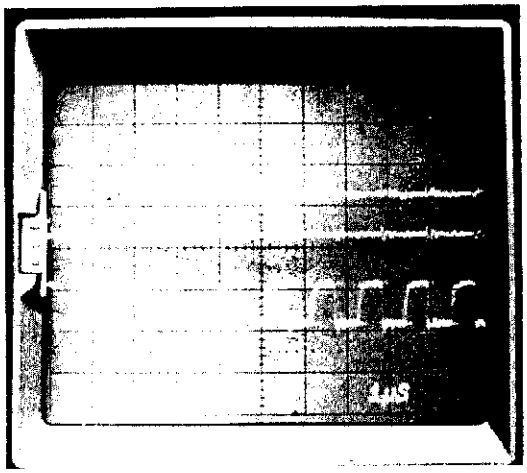
ADDRESS BUS
FIGURE 5



DB-0—DB-7

CLOCK ϕ2
TC1-15

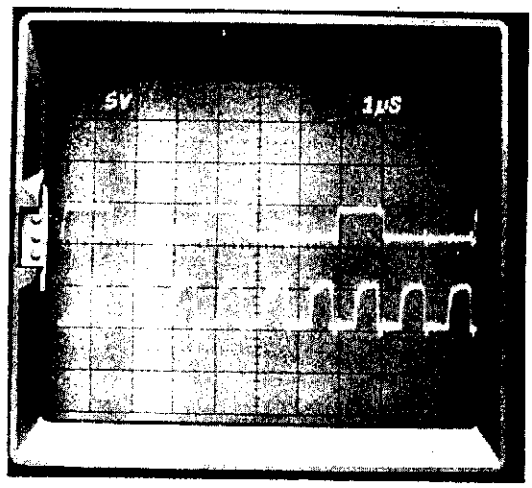
DATA BUS
FIGURE 6



$\overline{IRQ}$ TC1-16

CLOCK ϕ2
TC1-15

INTERRUPT REQUEST SIGNAL
FIGURE 6A



SYNC
TC1-PIN 12

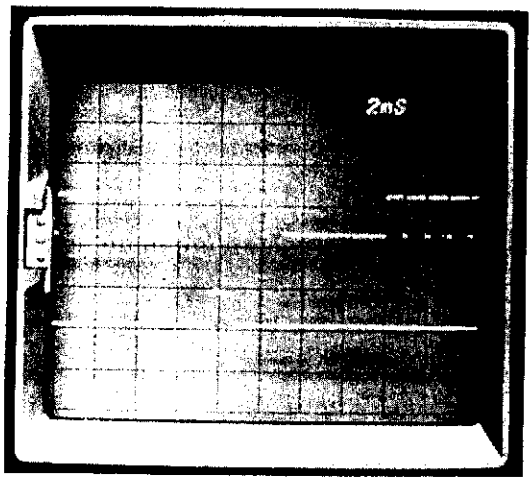
SYSTEM CLOCK $\phi 2$
TC1-PIN 15

FIGURE 6B

This completes all checks of control board dynamic signals.

d. Display Signals

After initialization, the control board will idle in the attract mode. During this time, segments will alternate between "High Game to Date" (if option switches S23 & S24 are not both OFF) and the players last scores, which will be zero for all players. Segments 'a' through 'g' of components Z19, Z21, and Z23 will toggle as shown in Figure 7. Segment 'g' will have little or no information on it.



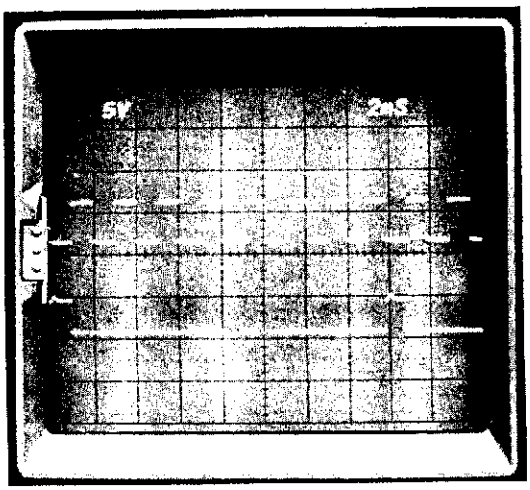
TYPICAL SEGMENT DATA

DIGIT STROBE 1
Z17, PIN 4

FIGURE 7

NOTE: The waveform shown is typical. The number of pulses for any particular section will vary by what information is residing for players scores, number of credits, and match/ball-in-play. If all scores are zero and S28 and S18 are OFF, then data on output segment 'g' will not be present.

The digit strobes will run continuously after five seconds from the time power is applied to the board. Refer to Figure 8.



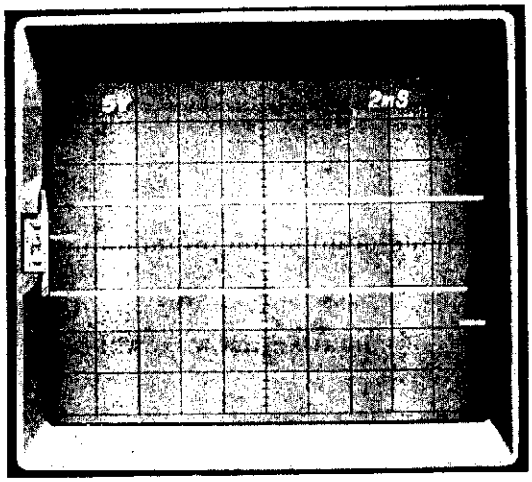
PA0
U5, PIN 8

DIGIT STROBE

DIGIT STROBES (TYPICAL)
FIGURE 8

c. Switch Matrix Signals

While in the attract mode, the switch matrix strobes are present at connector J5 pins 2-7 and pin 9, and connector J6 pins 1-8. Refer to Figure 9.



$\overline{S0}$ Z12, PIN 2

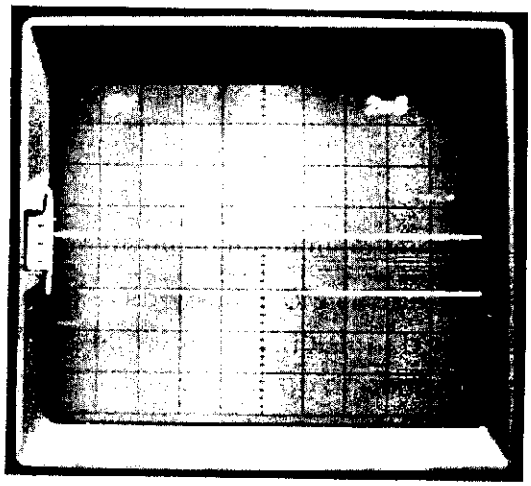
$\overline{S7}$ Z11, PIN 8

SWITCH MATRIX STROBE (TYPICAL)
FIGURE 9

The switch matrix return signals R0-R7 coming into Z13 and Z14 are normally at a LOGIC 1 level. If all playfield switches are open and all option switches are OFF, the outputs of Z13 and Z14 will all be at LOGIC 0 level.

d. Option Switches

There are 32 option switches on the control board used to adjust coin and play features in the game. An ON switch allows one of four data strobes (DS0, DS1, DS2, DS3) to be read by U4 when the power is turned on or the replay button is pressed. Refer to Figure 10.



PA0
U4, PIN 8

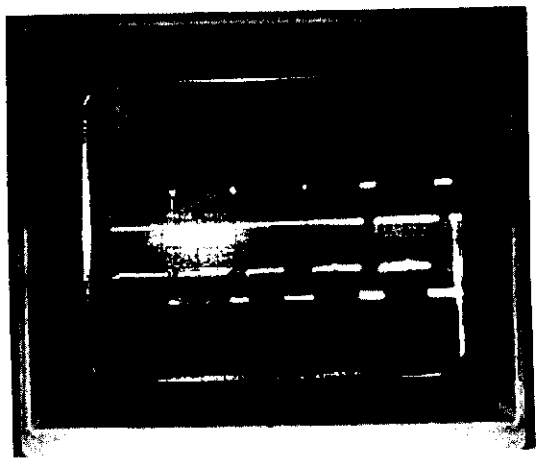
$\overline{S0}$
Z12, PIN 2

NOTE: ALL OPTION SWITCHES ON

FIGURE 10

e. Lamp Control

Lamp control logic consists of data strobes DS1 through DS12 clocking a latch IC on the driver board and load data signals LD1 through LD4 providing data to positions 1 through 4 of each latch IC. All of these signals are outputted from connector J4. A LOGIC 1 on LD1 at the time DS1 strobes high sets Latch 1 ON and will turn on the light connected to that point on the driver board. During SELF-TEST Step 16, each LD line is commanded to go from a LOGIC 0 to a LOGIC 1 to turn on the associated lamps. All data strobes, DS1 through DS12, may be checked at the even numbered pins of Z34 and Z35. Refer to Figure 11.



LD1
Z32, PIN 4

V = 5 Volts/Div.
H = 1 ms/Div.

DS1
Z34, PIN 12

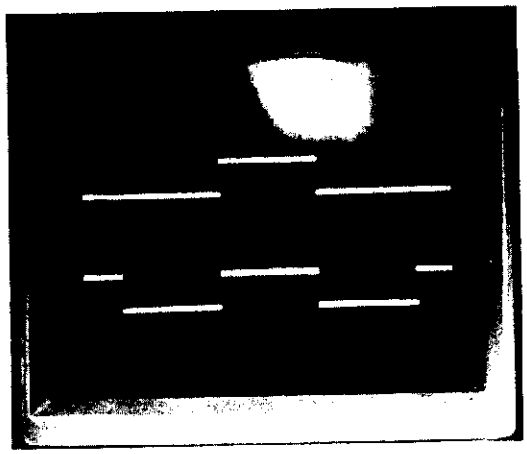
SCOPE TRIGGERED
BY DS LINE

FIGURE 11

f. Solenoid Control

Nine solenoid control lines are used for momentary solenoid operation. The nine lines go to the driver board through connector J4. During SELF-TEST Step 17 each line is commanded to go from a LOGIC 0 to a LOGIC 1 level to turn on the associated solenoid. In the attract mode all of these lines are at a LOGIC 0 level.

NOTE: Solenoids 3, 4, and 7 drive the optional electro-mechanical coin counters. These lines are not pulsed during SELF-TEST.



SOL. 1
Z29, PIN 2

V = 5 v/Div.
H = .15 sec/Div.

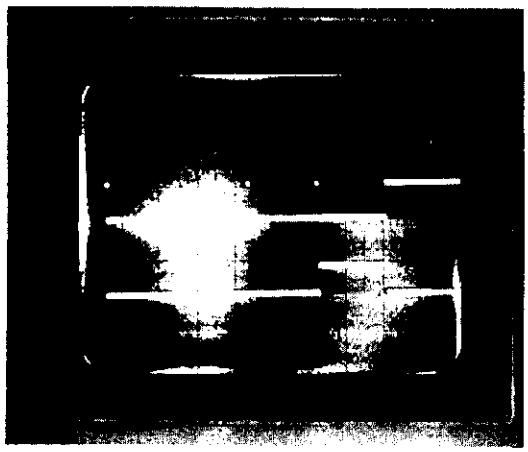
PA0
U6, PIN 8

SOLENOID TRIGGER SIGNAL

FIGURE 12

g. Sound Board Control

Four sound board control lines are used to trigger 1 of 15 sounds from the sound board. These four lines exit the microprocessor on the PA0 through PA3 ports of U6 and are gated with a sound enable signal, PA4, in Z31. The outputs of Z31 are normally low and pulse high.



PA4
U6, PIN 12

V = 5 v/Div.
H = 50 ms/Div.

S1
Z31, PIN 6

SOUND SELECT
FIGURE 13

B. DRIVER BOARD SERVICE

With the aid of the TEST FIXTURE or a known good game, each driver board output may be examined individually. Driver board malfunctions will most commonly be associated with transistor failures, which may cause a continuous output or no output. In these cases, replacement of the defective transistor will correct the malfunction.

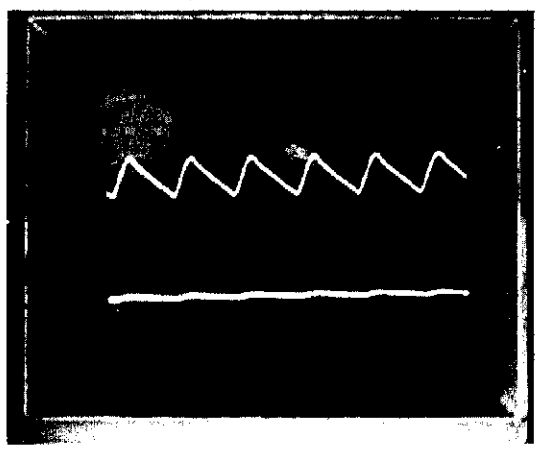
If one of the quad flip-flop devices is suspected, the outputs may be checked under test conditions. A LOGIC 1 on the output of any latch circuit (SN74175) should turn on the corresponding transistor lamp driver.

The 7404 IC on the driver board provides buffering for the sound board trigger signals. The normal input states for these four signals is low, pulsing high when the sound board is triggered.

C. POWER SUPPLY SERVICE

Trouble-shooting the power supply consists of determining which of the output voltages are incorrect, and then determining which components are at fault. The Theory of Operation section will serve as an aid in tracing through the circuits on the power supply. Note that the voltages shown on the power supply schematic are typical values when the power supply is installed in a game and the game is in the attract mode. Test points are provided and labeled to assist in measuring voltages.

Two comments are in order: (1) The two LEDs on the power supply indicate voltage is present, but not necessarily correct. (2) Always check to see that the case of the transistor mounted on the frame (Q1) and the associated mounting hardware is electrically isolated from the frame. No component lead or connector lead should be in electrical contact with the frame.

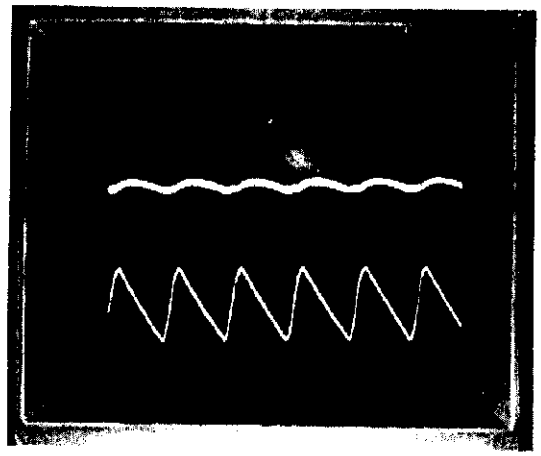


12VDC RIPPLE
V = 2V/DIV (AC COUPLED)

5VDC RIPPLE
V = 5mv/DIV (AC COUPLED)

5VDC VOLTAGE REGULATION

FIGURE 14



60VDC REGULATION

60VDC OUTPUT RIPPLE
V = 50mv/DIV
AC COUPLED

60VDC RIPPLE AT C1
V = 1v/DIV
AC COUPLED

FIGURE 15

D. DISPLAY BOARD SERVICE

A LOGIC 1 input pulse to either driver package on the display board results in a high pulse at the corresponding output to enable a particular digit or a particular segment.

Continuous driver outputs or failure of an input to produce an output indicate a defective driver package.

Incorrect segments turning on with normal driver outputs indicates an internally shorted display module.

Segments which fail to turn on with normal driver outputs indicate a defective display module.

E. SOUND BOARD SERVICE

Sound board problems will generally be of two types, (1) no sound at all, and (2) low volume or distorted sounds.

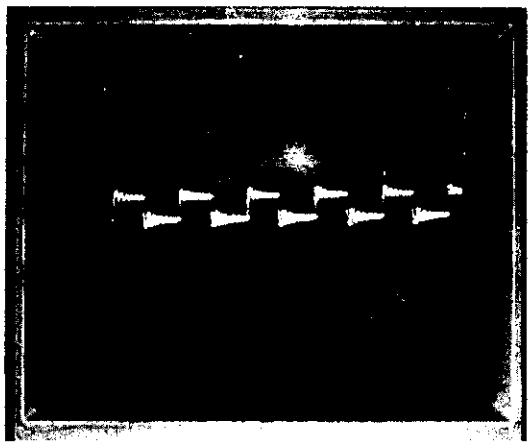
If the board emits no sound at all, check the three supply voltages, +5VDC, +12VDC, and −12VDC, on the board.

Press the self-test switch and observe pin 4 of the DAC. An asynchronous sine wave with harmonics should be present. If not, check the reset signal on U1, pin 1. It should remain low after power is applied, and then go high.

Check the clock signal on U1 pin 28 and U2 pin 39. Check PA0 through PA7 of U2. If these lines are inactive, check the R/W line, data bus, and address bus for signals. NOTE: AB-10 and AB-11 are buffered on the board. Check on both sides of the buffering.

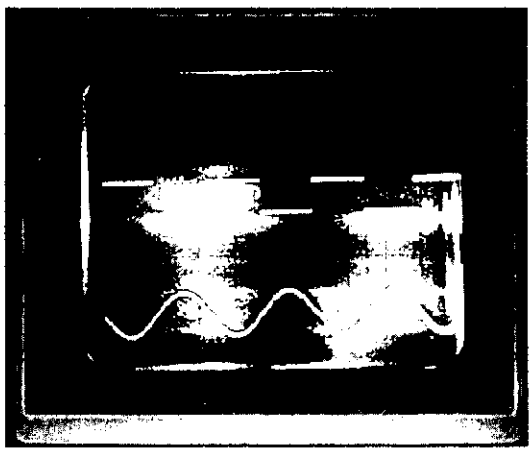
If pin 4 of the DAC is active, the problem is most likely the LM380. Check pin 2 of the LM380 for a 200 mvolt P-P signal. Check pin 8 of the LM380 for a signal changing from +2V to +10V (nominal). This is the output of the sound board.

If the sound board output is incorrect, again check pin 4 of the DAC. If the wave is discontinuous, check PA0 through PA7 and the −12VDC. One of these signals may be missing. Compare the input and output of the LM380. Verify that it amplifies and does not distort the waveform. Replacement of the DAC or the LM380 will usually correct the problem.



U6, PIN 2
V = 5V/DIV.
H = .5 s/DIV.

A6 SOUND BOARD CLOCK
FIGURE 16



U3, PIN 5
V = 5V/DIV.
H = 2ms/DIV.
U3, PIN 4

DIGITAL-TO-ANALOG CONVERTER OPERATION
FIGURE 17

F. POP BUMPER DRIVER BOARD SERVICE

Install the board on a known good playfield. Check for + 5VDC between pins 7 and 14 of Z1. Ground pin 3 of Z1. Pin 1 of Z1 should pulse low for approximately 40 msec. At the same time, pin 12 of Z2 should pulse high. This turns on Q1 which will provide a ground path for the coil.

SECTION V
SCHEMATICS AND PARTS LIST

I SYSTEM 80 POWER DISTRIBUTION

II A1 CONTROL BOARD

III A2 POWER SUPPLY

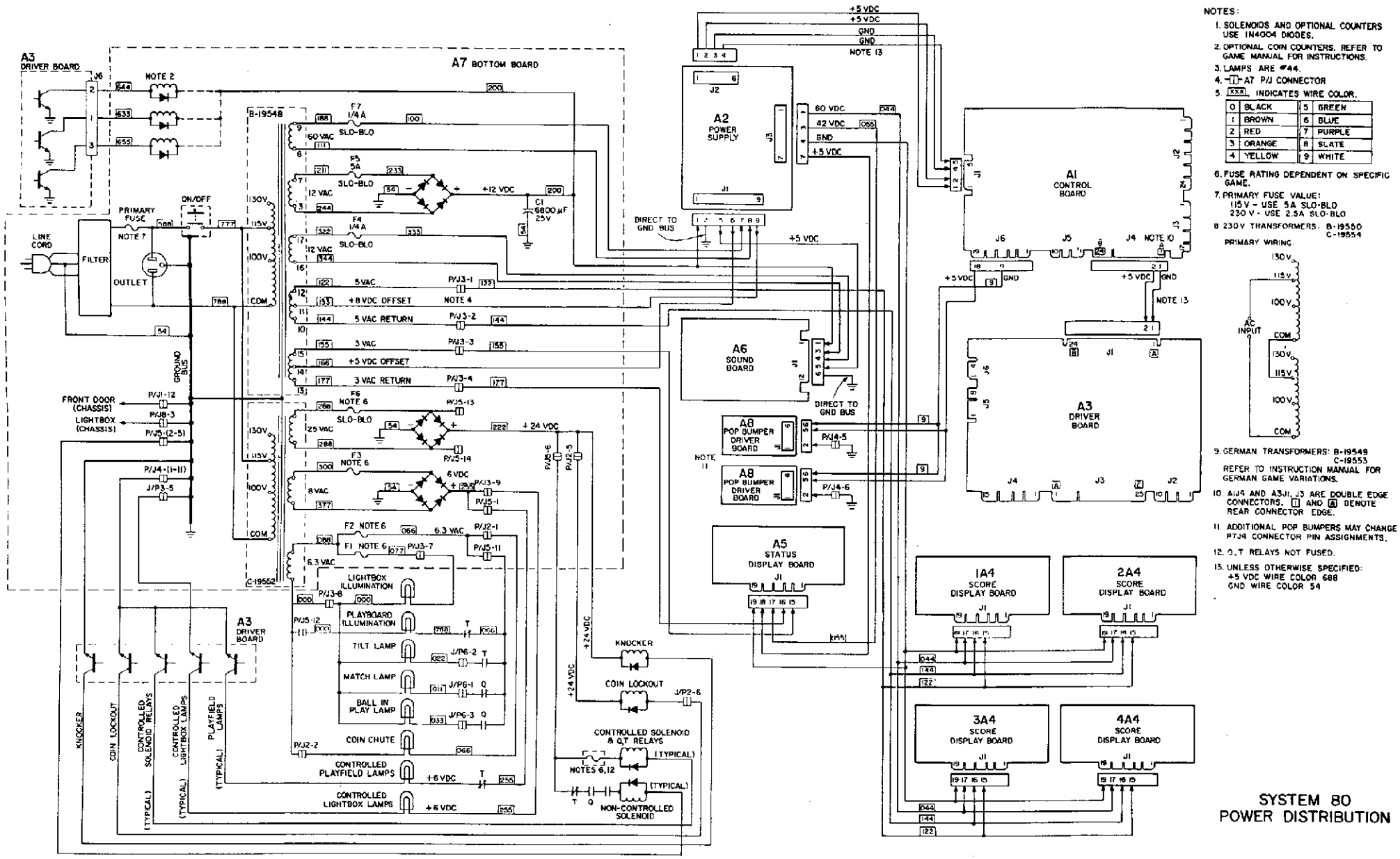
IV A3 DRIVER BOARD

V A4 DISPLAY

VI A5 DISPLAY

VII A6 SOUND BOARD

VIII A8 POP BUMPER DRIVER BOARD



NOTES:

1. SOLENOIDS AND OPTIONAL COUNTERS USE 1N4004 DIODES.
2. OPTIONAL COIN COUNTERS. REFER TO GAME MANUAL FOR INSTRUCTIONS.
3. LAMPS ARE #44.
4. -[1]- A7 P/J CONNECTOR
5. [XXX] INDICATES WIRE COLOR.

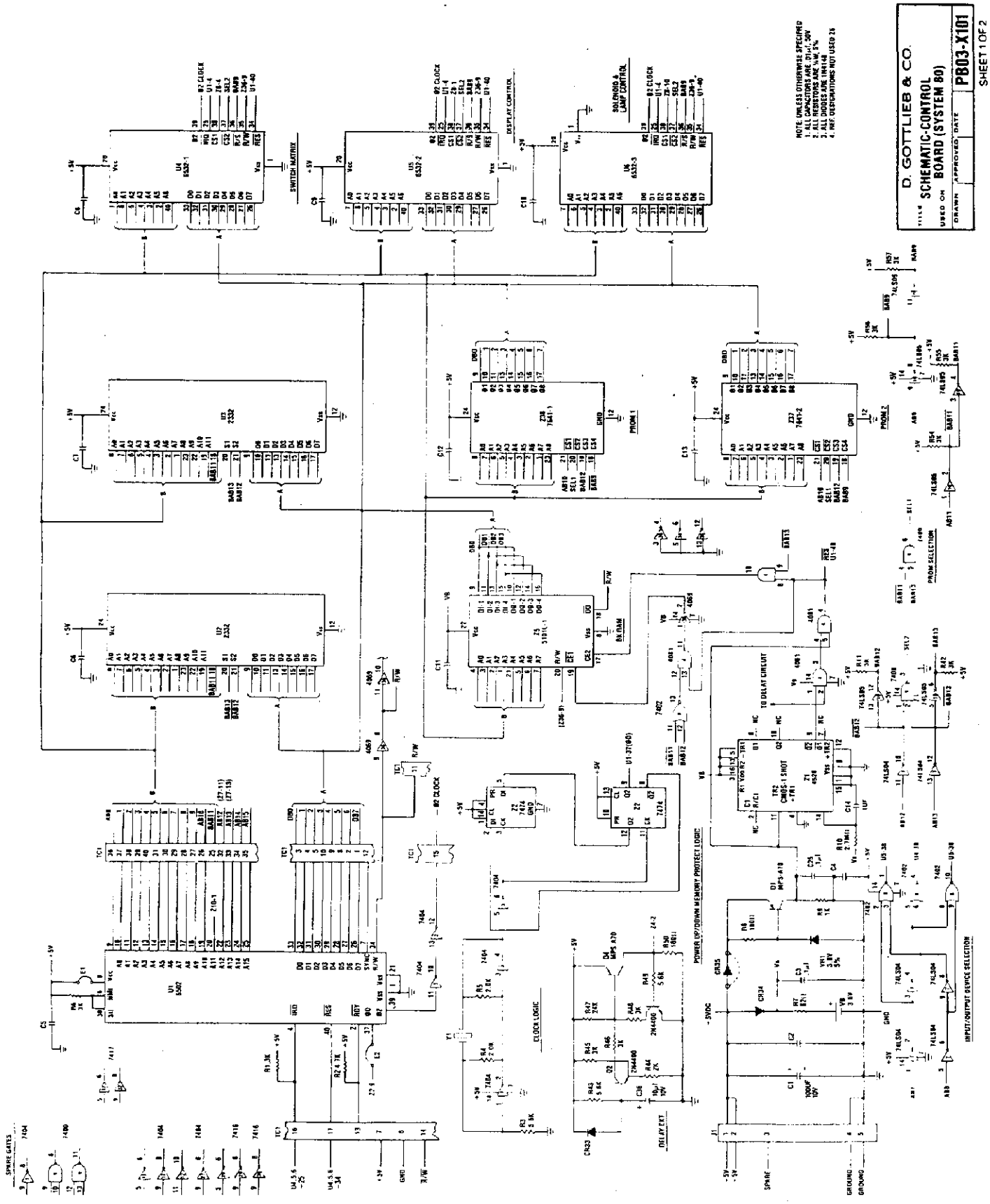
0	BLACK	5	GREEN
1	BROWN	6	BLUE
2	RED	7	PURPLE
3	ORANGE	8	SLATE
4	YELLOW	9	WHITE

6. FUSE RATING DEPENDENT ON SPECIFIC GAME.
7. PRIMARY FUSE VALUE:
   115 V - USE 5A SLO-BLO
   230 V - USE 2.5A SLO-BLO
8. 230 V TRANSFORMERS: B-19550
   C-19554
   PRIMARY WIRING.

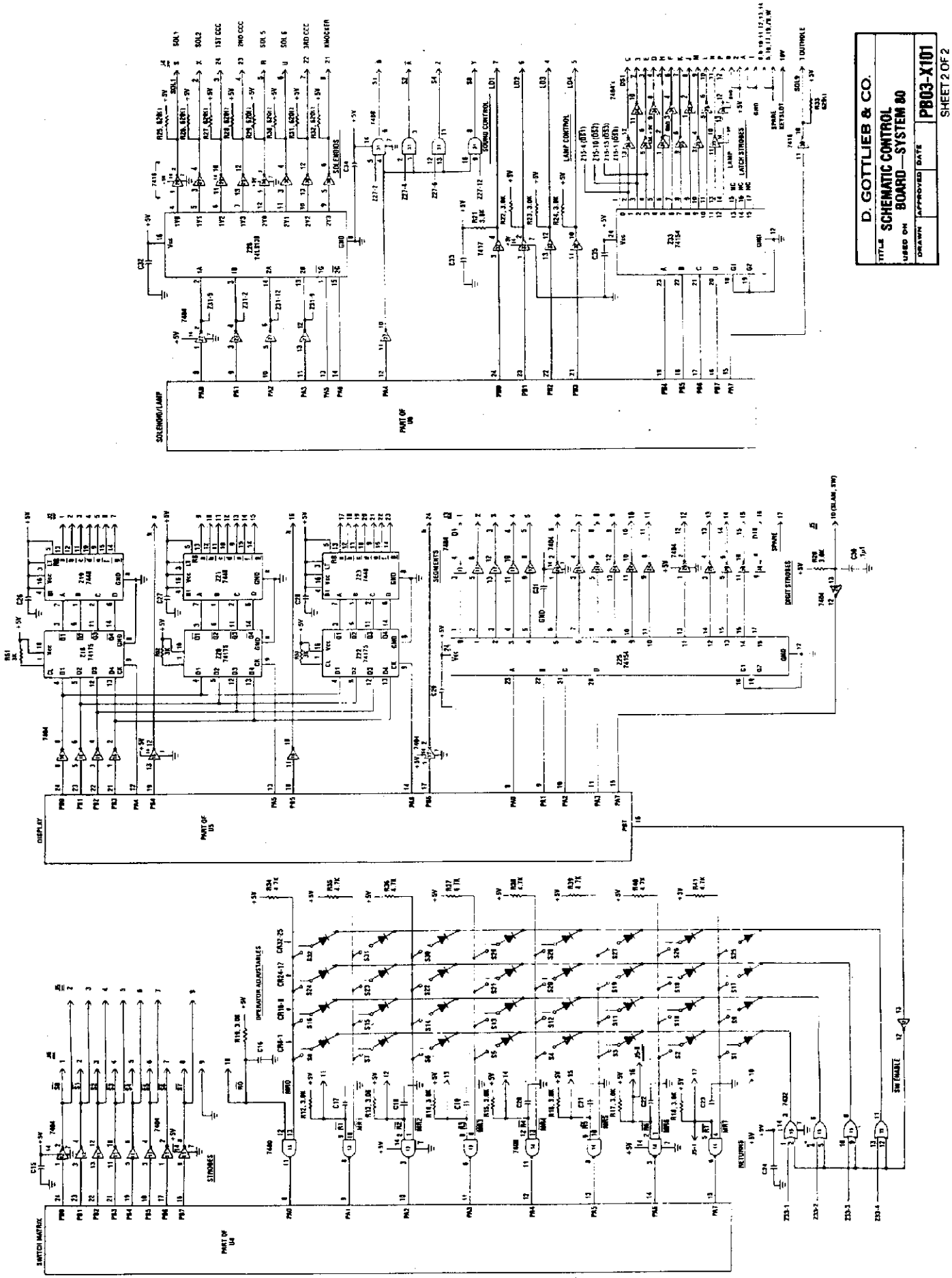
9. GERMAN TRANSFORMERS: B-19549
   C-19553
   REFER TO INSTRUCTION MANUAL FOR GERMAN GAME VARIATIONS.
10. A1J4 AND A3J1, J3 ARE DOUBLE EDGE CONNECTORS. [1] AND [A] DENOTE REAR CONNECTOR EDGE.
11. ADDITIONAL POP BUMPERS MAY CHANGE PTJ4 CONNECTOR PIN ASSIGNMENTS.
12. Q,T RELAYS NOT FUSED.
13. UNLESS OTHERWISE SPECIFIED:
    +5 VDC WIRE COLOR 688
    GND WIRE COLOR 54

SYSTEM 80
POWER DISTRIBUTION

A1 CONTROL BOARD SCHEMATIC (DET. PB03-D102-001)



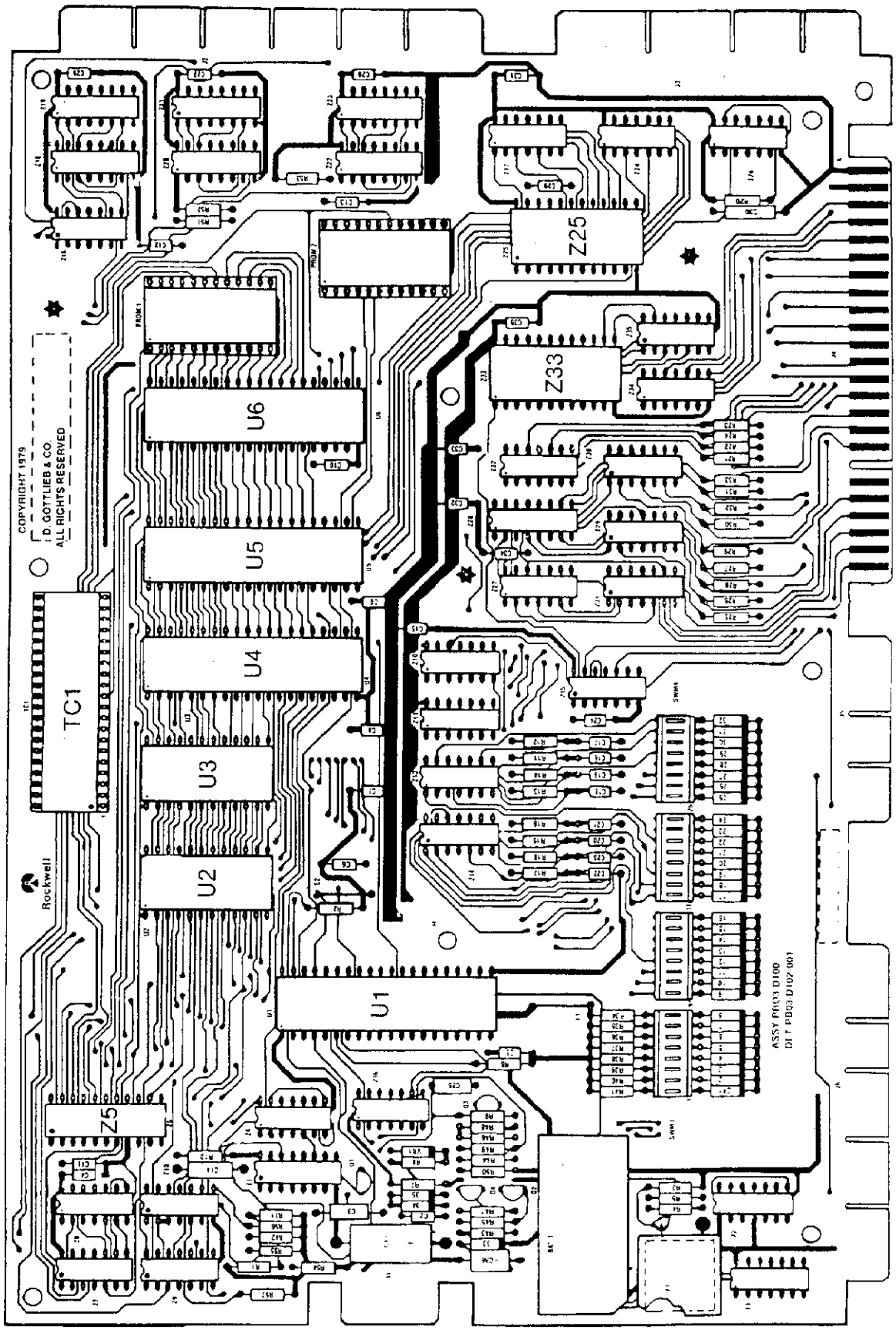
CONTROL BOARD COMPONENT LOCATION (DET. PB03-D102-001)



D. GOTTLIEB & CO.			
TITLE SCHEMATIC CONTROL BOARD—SYSTEM 80			PB03-X101
USED ON			
DRAWN	APPROVED	DATE	

SHEET 2 OF 2

A1 CONTROL BOARD SCHEMATIC (DET. PB03-D102-001)



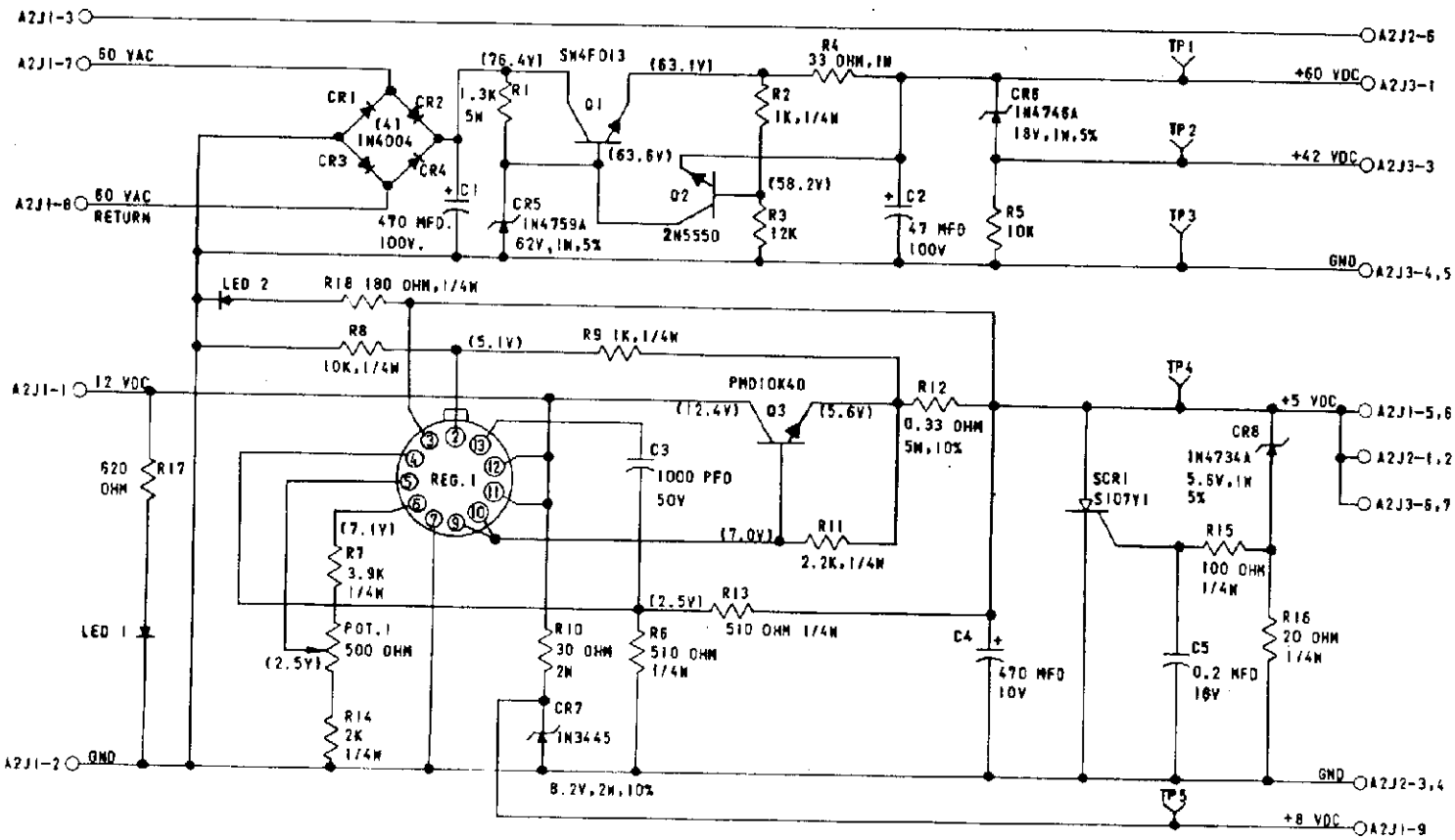
CONTROL BOARD

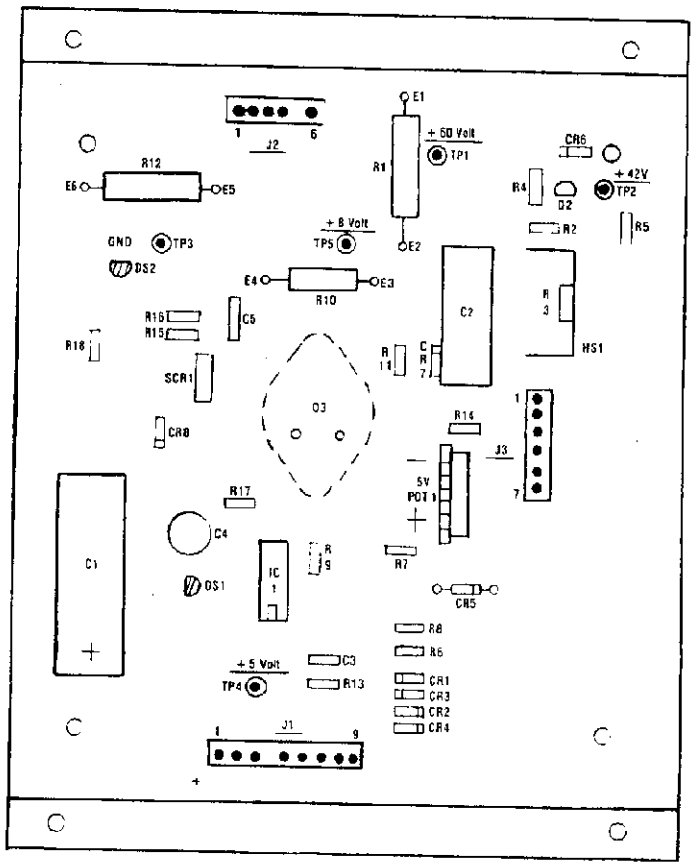
PART NUMBER	DESCRIPTION
R6502-13	CPU—(U1)
R6532-18	RIOT—(U4, U5, U6)
R3273-12	ROM—(U2)
R3272-12	ROM—(U3)
P5101L-1	RAM/CMOS—(Z5)
640361-3	SOCKET—DIL, 24 PIN
SN7402N	IC—2 INPUT—"NOR"—(Z8)
SN7400N	IC—2 INPUT—"NAND"—(Z9, Z13, Z14)
SN7432N	IC—2 INPUT—"OR"—(Z15)
SN7404N	IC—HEX INVERTER—(*)
SN7416N	IC—HEX INVERTER—OC/HV—(Z29, Z30)
SN7417N	IC—HEX BUFFER—OC—(Z32)
SN74LS139N	IC—2 TO 4 DECODER—(Z28)
SN74175N	IC—"D" FLIP FLOP—(Z18, Z20, Z22)
SN7448N	IC—4 TO 7 DECODER—(Z19, Z21, Z23)
SN74154N	IC—4 TO 16 DECODER—(Z25, Z33)
SN7474N	IC—DUAL FLIP FLOP—(Z2)
SCL4528B	CMOS IC—DUAL 1 SHOT—(Z1)
SCL4081B	CMOS IC—QUAD 2 INPUT "AND"—(Z4)
1N4148	DIODE—GP—(CR1-CR35)
1N5225B or 1N5987B	ZENER DIODE—3.0V, 5%—(VR1)
326R10-002	BATTERY—3.6V—(BAT. 1)
333R08-001	CRYSTAL—3.579545 MHZ—(Y1)
131R06-001	SPACER, CORK
MPS A70	TRANSISTOR—PNP—(Q1, Q4)
341R31-005	DIP SWITCH PACK—8 POS.—(SW1-SW4)
2N4400	TRANSISTOR—MOTOROLA—(Q2, Q3)
SN74LS05N	IC—OPEN COLLECTOR INVERTER—(Z10)
SN74LS04N	IC—HEX INVERTER—(Z7)
MM74C04 or SCL 4069B	IC—CMOS—(Z36)
640379-3	SOCKET—40 PIN—(TC1)

*(Z3, Z11, Z12, Z16, Z17, Z24, Z26, Z27, Z34, Z35)

DESCRIPTION (Continued)
RESISTOR—62Ω, ¼W, 5%—(R7)
CAPACITOR—.01 MICROFARAD, 50V—(C2, C4-C13, C15-C24, C26-C29, C31-C35)
CAPACITOR—.1 MICROFARAD, 50V—(C3, C14, C25, C30)
CAPACITOR—100 MICROFARAD, 10V—(C1)
RESISTOR—3.0KΩ, ¼W, 5%—(R1, R6, R11-24, R42, R45, R46, R48, R51-R57)
RESISTOR—2.0KΩ, ¼W, 5%—(R4, R5, R44)
RESISTOR—180Ω, ¼W, 5%—(R8, R50)
RESISTOR—1KΩ, ¼W, 5%—(R9)
RESISTOR—2.7MΩ, ¼W, 5%—(R10)
RESISTOR—620Ω, ¼W, 5%—(R25-R33)
RESISTOR—4.7KΩ, ¼W, 5%—(R2, R34-R41)
RESISTOR—5.6KΩ, ¼W, 5%—(R3, R43, R49)
RESISTOR—24KΩ, ¼W, 5%—(R47)
CAPACITOR—10 MICROFARAD, 10V—(C36)

A2 POWER SUPPLY SCHEMATIC





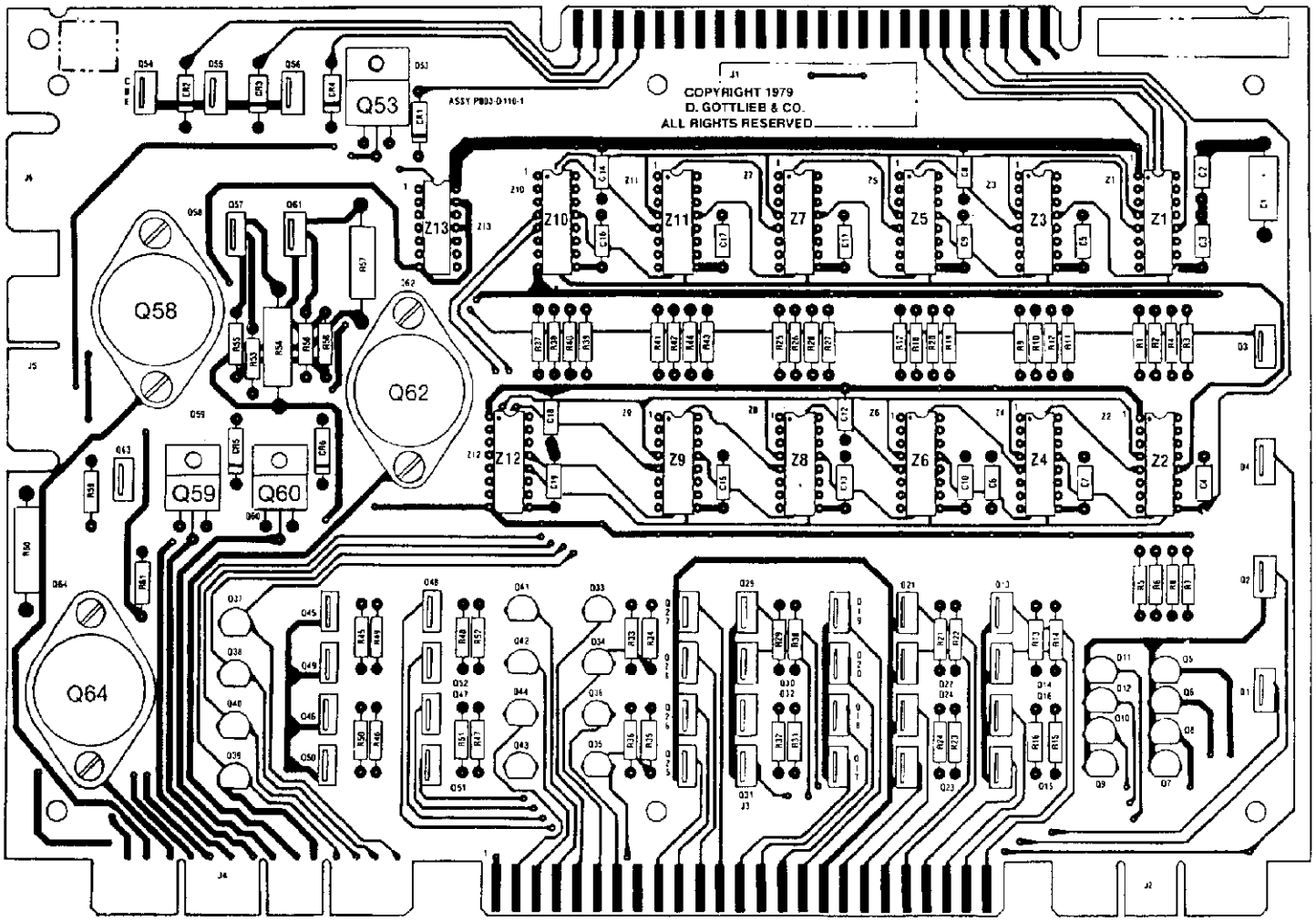
NOTE: UNLESS OTHERWISE SPECIFIED,
1. RESISTORS ARE ½W, 5%
2. VOLTAGES ARE DC WITH RESPECT TO CIRCUIT GROUND
3. ALL VOLTAGES ARE AT NOMINAL LINE VOLTAGE (115VAC)
4. REG. 1 IS TYPE 723 14 PIN DIP
5. LEDS ARE RL4850
6. ASSEMBLY NUMBER PX2600

D. GOTTLIEB & CO.			
TITLE: POWER SUPPLY SCHEMATIC			
USED ON: SYSTEM 80			
DRAWN	APPROVED	DATE	B-19694

A2 POWER SUPPLY

PART NUMBER	DESCRIPTION
	HEATSINK MOUNTING PLATE
	SPACER—6—32 THREAD X 5/32
	SPACER—6—32 THREAD X 1/8
1N4004	DIODE—(CR1-CR4)
1N4759A	ZENER DIODE—62V, 1W, 5%—(CR5)
1N4746A	ZENER DIODE—18V, 1W, 5%—(CR6)
1N3445	ZENER DIODE—8.2V, 2W, 10%—(CR7)
1N4734A	ZENER DIODE—5.6V, 1W, 5%—(CR8)
SW4F013	TRANSISTOR—NPN—NATIONAL—(Q1)
2N5550	TRANSISTOR—NPN—(Q2)
PMD10K40	TRANSISTOR—LAMBDA—(Q3)
S107Y1	SILICON CONTROLLED RECTIFIER—(SCR1)
UA723CN	IC—14 PIN DIP—(IC1)
CM4-22	DIODE—LIGHT EMITTING—(LED1, LED2)
115R501A	POTENTIOMETER—500Ω—CTS—(POT1)
	RESISTOR—1.3KΩ, 5W, 10%—(R1)
	RESISTOR—1KΩ, 1/4W, 5%—(R2, R9)
	RESISTOR—12KΩ, 1/2W, 5%—(R3)
	RESISTOR—33Ω, 1W, 5%—(R4)
	RESISTOR—510Ω, 1/4W, 5%—(R6, R13)
	RESISTOR—3.9KΩ, 1/4W, 5%—(C7)
	RESISTOR—10KΩ, 1/4W, 5%—(R8)
	RESISTOR—30Ω, 2W, 5%—(R10)
	RESISTOR—2.2KΩ, 1/4W, 5%—(R11)
	RESISTOR—.33Ω, 5W, 10%—(WIRE WOUND)—(R12)
	RESISTOR—10KΩ, 1/2W, 5%—(R5)
	RESISTOR—2KΩ, 1/4W, 5%—(R14)
	RESISTOR—100Ω, 1/4W, 5%—(R15)
	RESISTOR—20Ω, 1/4W, 5%—(R16)
	RESISTOR—620Ω, 1/2W, 5%—(R17)
	RESISTOR—180Ω, 1/4W, 5%—(R18)
	CAPACITOR—470 MICROFARAD, 100V—(C1)
	CAPACITOR—47 MICROFARAD, 100V—(C2)
	CAPACITOR—1000 PICOFARAD, 50V—(C3)
	CAPACITOR—470 MICROFARAD, 10V—(C4)
	CAPACITOR— 2 MICROFARAD, 16V, $^{+80\%}_{-20\%}$—(C5)
	TURRET TERMINAL—(E1-E6)
	TURRET TERMINAL—(TP1-TP5, CP5)
1NS-3	INSULATOR
DM111	INSULATOR
GS2-3	EYELET
	CONNECTOR—6 PIN—MOLEX—(J2)
	CONNECTOR—7 PIN—MOLEX—(J3)
	CONNECTOR—9 PIN—MOLEX—(J1)
	HEAT SINK—THERMALLOY

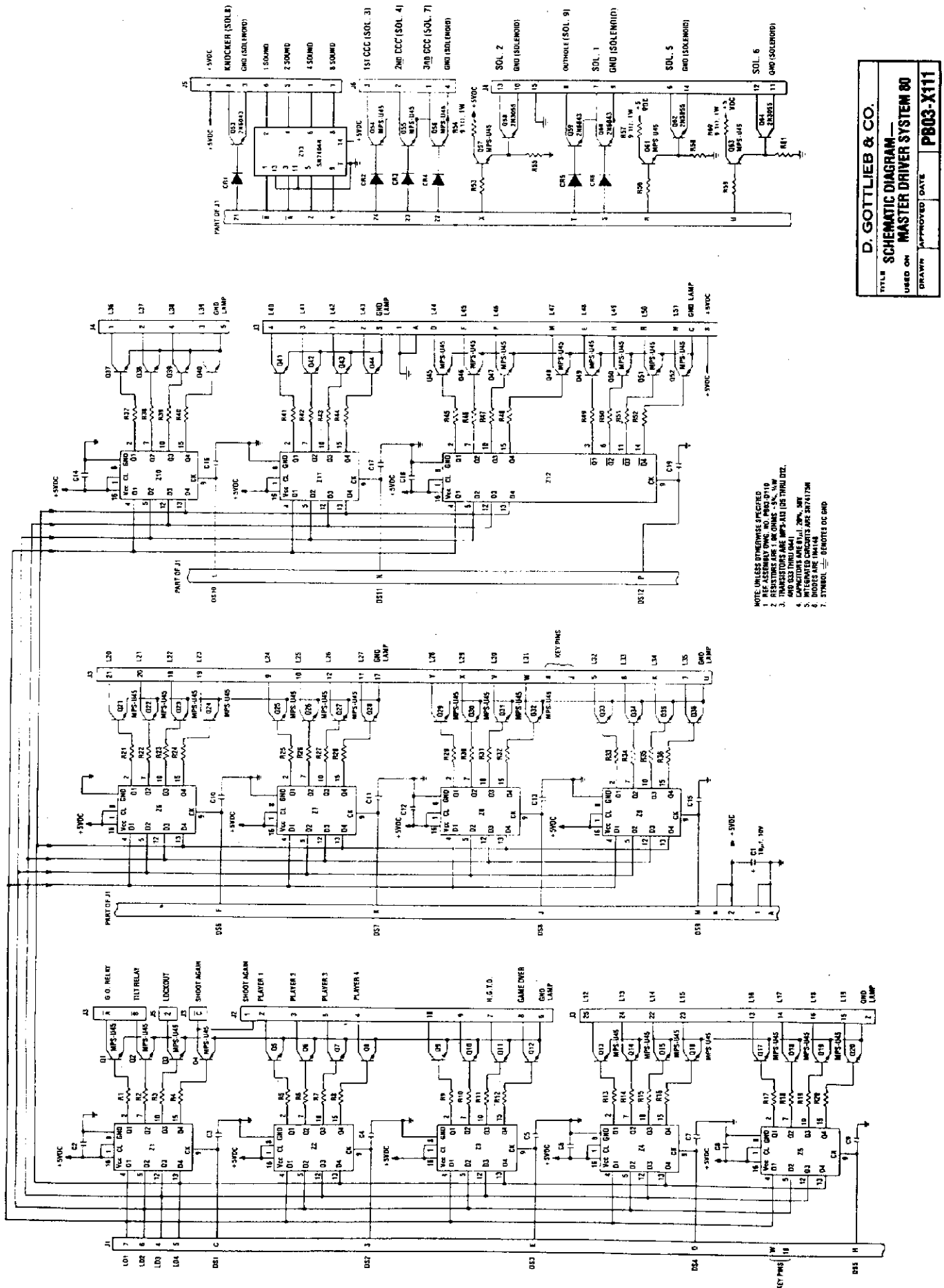
A3 DRIVER BOARD COMPONENT LOCATION



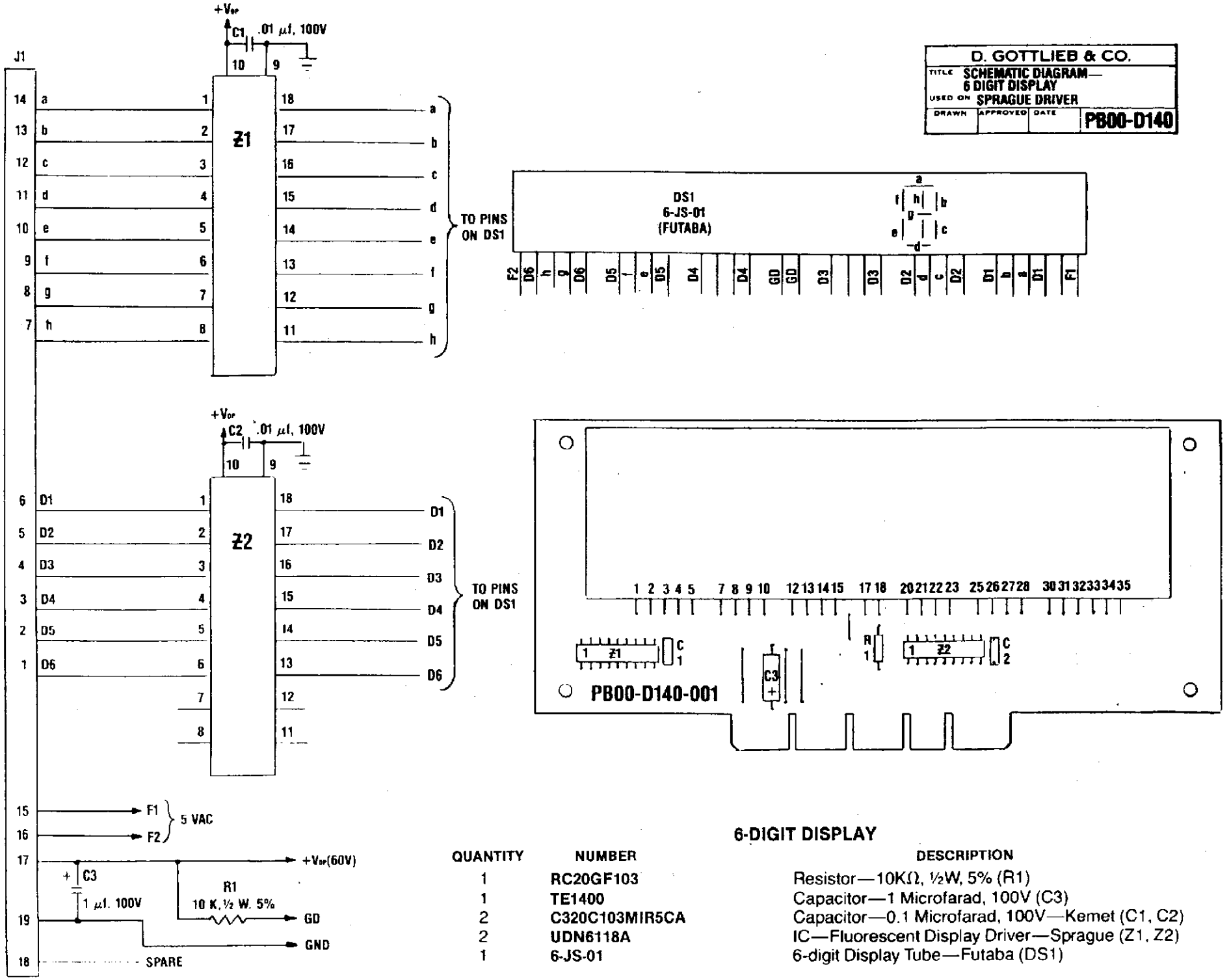
MASTER DRIVER BOARD

PART NUMBER	DESCRIPTION
43-03-4	INSULATOR—THERMALLOY
2N6043	TRANSISTOR—NPN—(Q53, Q59, Q60)
2N3055	TRANSISTOR—NPN—(Q58, Q62, Q64)
MPS-U45	TRANSISTOR—NPN—(Q1-Q4, Q13-Q32, Q45-Q52, Q54-Q57, Q63)
MPS-A13	TRANSISTOR—NPN—(Q5-Q12, Q33-Q44)
SN74175N	IC—QUAD "D" FLIP-FLOP—(Z1-Z12)
SN7404N	IC—HEX INVERTER—(Z13)
1N4148	DIODE—SILICON—(CR1-CR6)
	CAPACITOR—.01 MICROFARAD, 50V—(C2-C19)
	CAPACITOR—10 MICROFARAD, 10V—TANTALUM—(C1)
	RESISTOR—1000Ω, ¼W, 5%—(R1-R53, R61, R55, R56, R58, R59)
	RESISTOR—9.1Ω, 1W, 5%—(R54, R57, R60)

A3 DRIVER BOARD SCHEMATIC



D. GOTTLIEB & CO.			
TITLE: SCHEMATIC DIAGRAM—			
USED ON: MASTER DRIVER SYSTEM 80			PB03-X111
DRAWN	APPROVED	DATE	

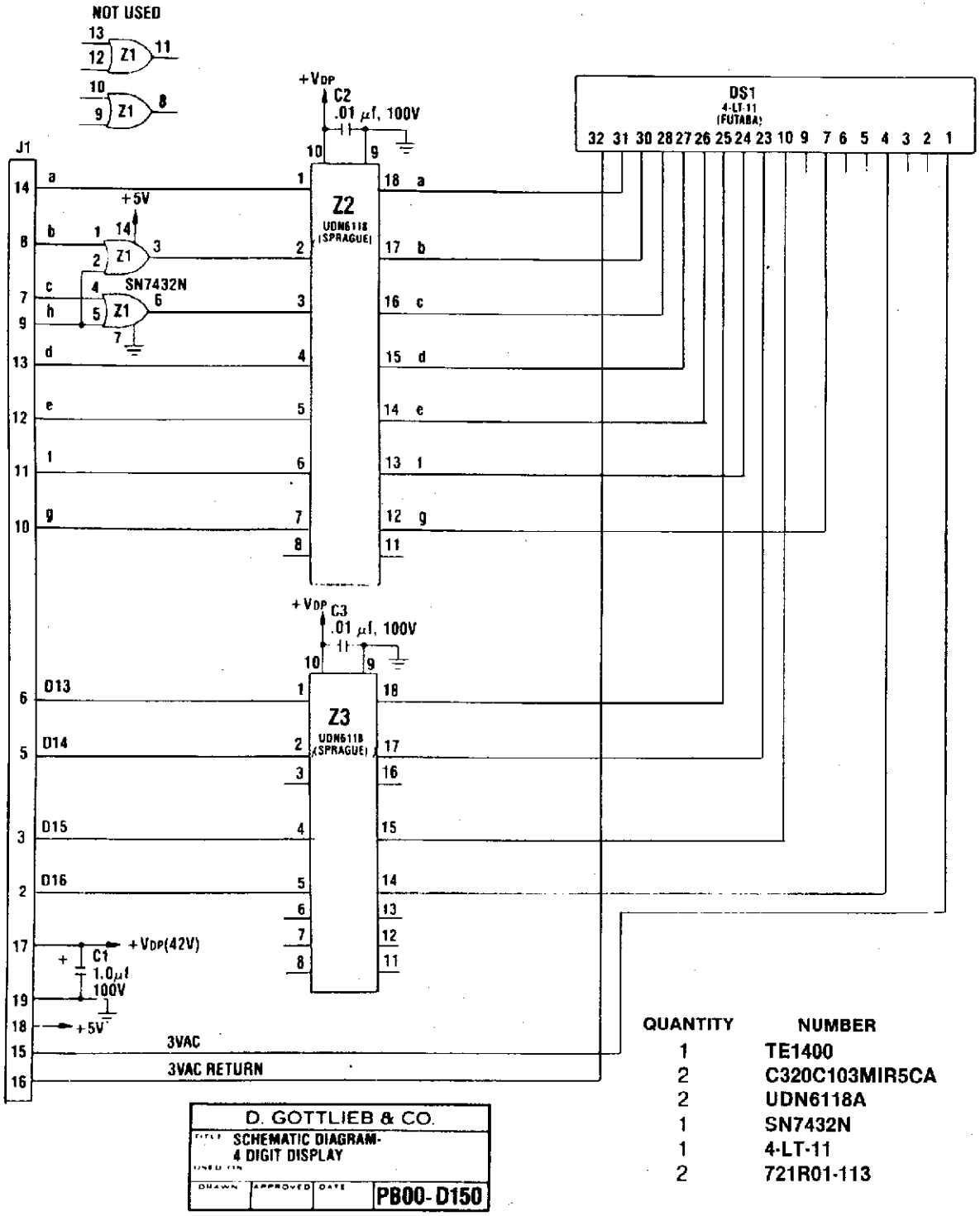


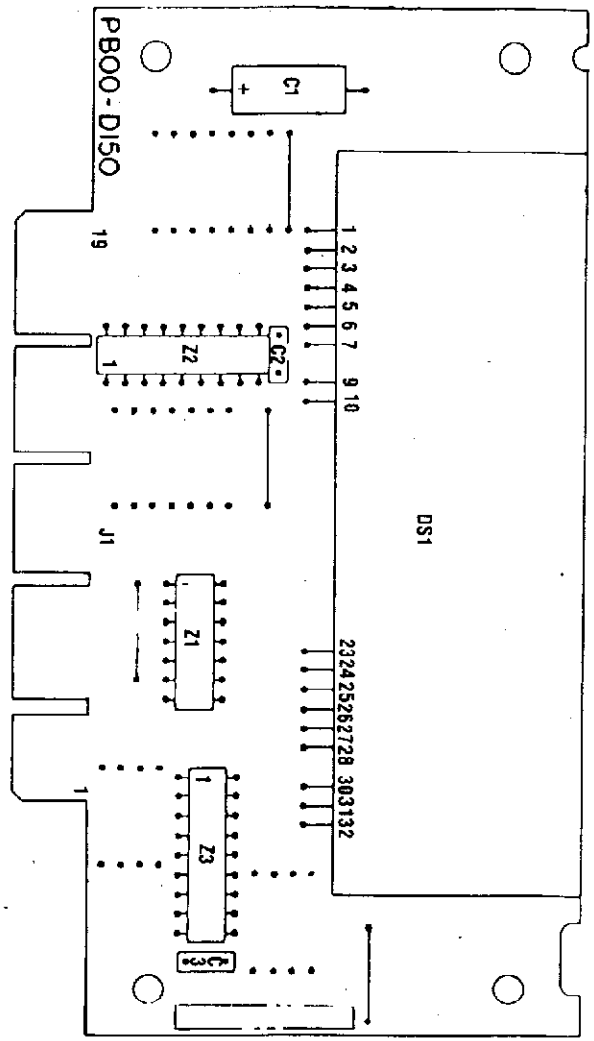
D. GOTTLIEB & CO.			
TITLE SCHEMATIC DIAGRAM— 6 DIGIT DISPLAY			
USED ON SPRAGUE DRIVER			
DRAWN	APPROVED	DATE	PB00-D140

A4 6 DIGIT DISPLAY

6-DIGIT DISPLAY

QUANTITY	NUMBER	DESCRIPTION
1	RC20GF103	Resistor—10KΩ, ½W, 5% (R1)
1	TE1400	Capacitor—1 Microfarad, 100V (C3)
2	C320C103MIR5CA	Capacitor—0.1 Microfarad, 100V—Kemet (C1, C2)
2	UDN6118A	IC—Fluorescent Display Driver—Sprague (Z1, Z2)
1	6-JS-01	6-digit Display Tube—Futaba (DS1)





A5 4 DIGIT DISPLAY

D. GOTTLIEB & CO.			
SCHEMATIC DIAGRAM- 4 DIGIT DISPLAY			
DRAWN	APPROVED	DATE	PB00-D150

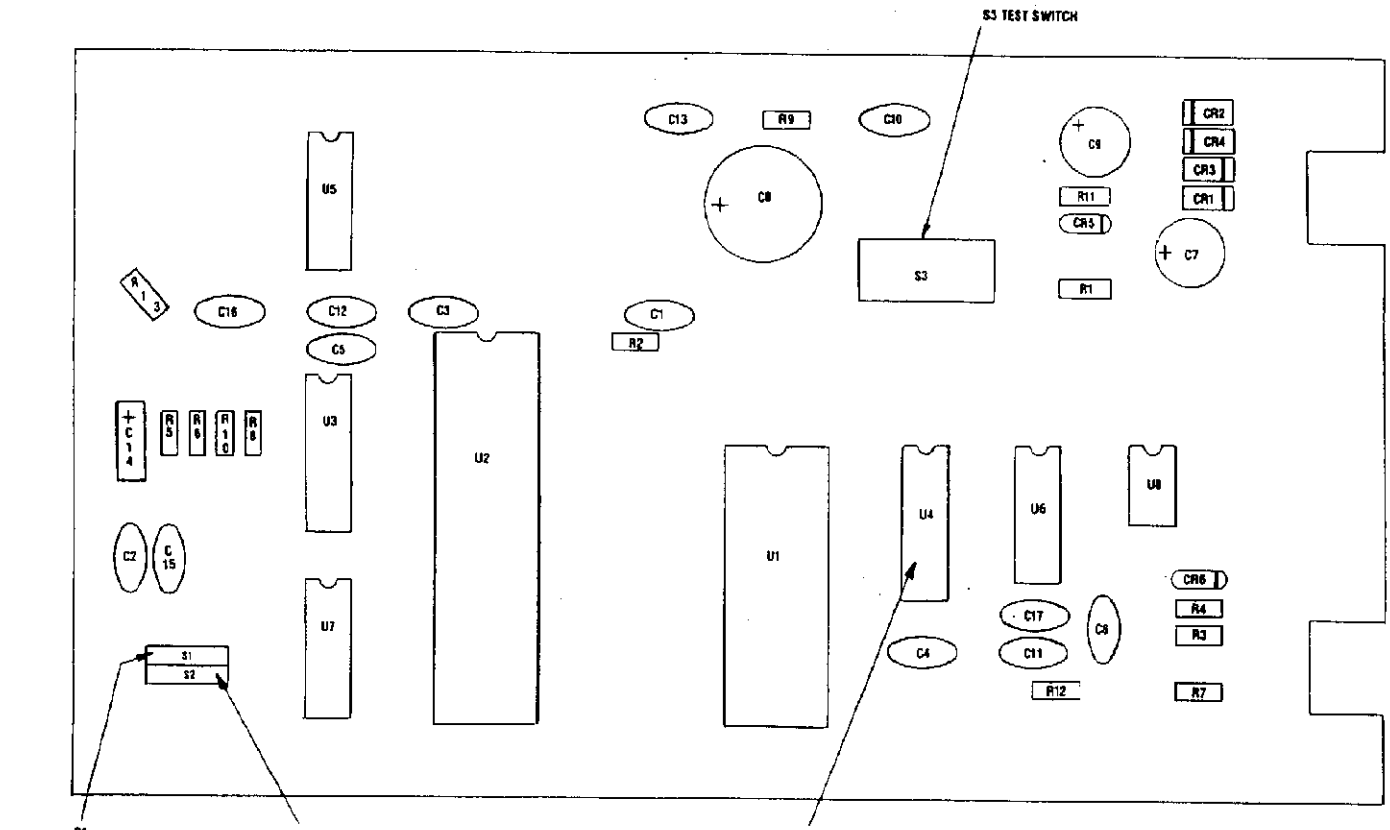
QUANTITY	NUMBER
1	TE1400
2	C320C103MIR5CA
2	UDN6118A
1	SN7432N
1	4-LT-11
2	721R01-113

4-DIGIT DISPLAY

DESCRIPTION

Capacitor—1 Microfarad, 100V—Sprague (C-1)
Capacitor—0.01 Microfarad, 100V—Kemet (C2, C3)
IC—Fluorescent Display Driver—Sprague (Z2, Z3)
IC—Quad OR Gate—T.I. (Z1)
4-digit Display Tube—Futaba (DS1)

A6 SOUND BOARD COMPONENT LOCATION



S1
OFF = CONTINUOUS SOUND
ON = SCORING SOUNDS ONLY

S2
OFF = NO ATTRACT TUNE
ON = ATTRACT TUNE EVERY 6 MINUTES

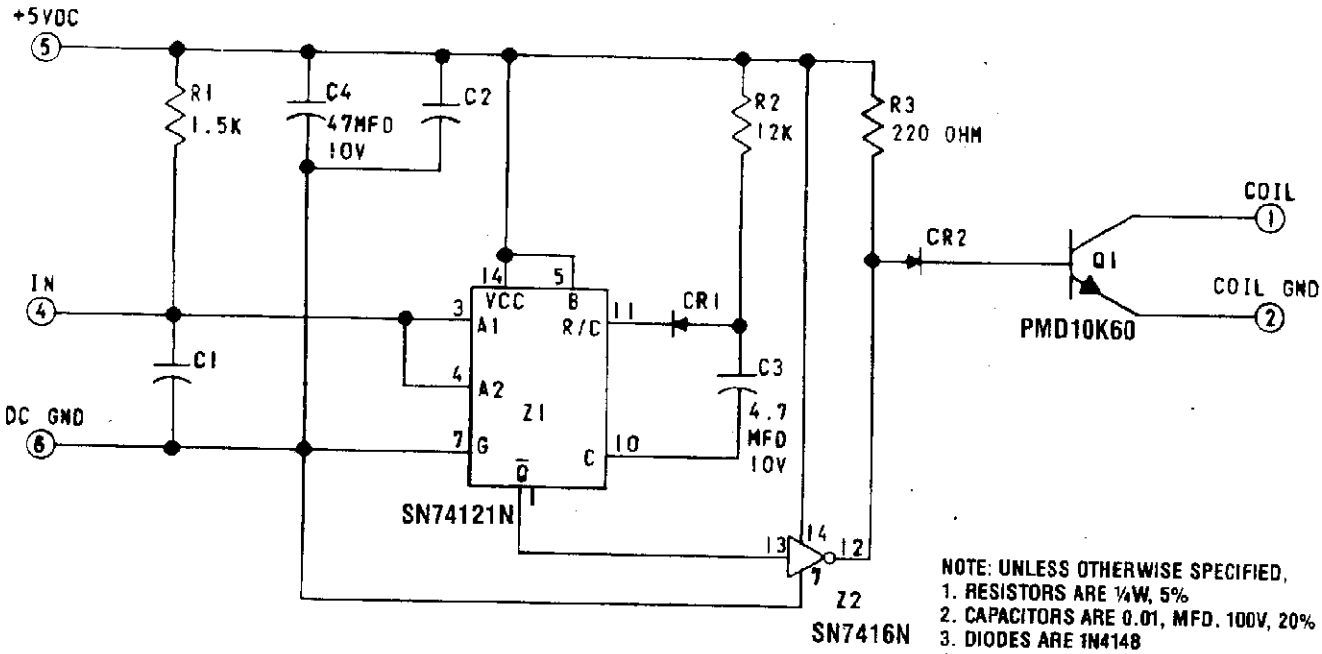
NOTE: SOUND BOARD PROM IS INSERTED WITH INDENT NOTCH UP. PROM IS MARKED WITH GAME NUMBER.

D. GOTTLIEB & CO.	
TITLE	SOUND BOARD COMPONENT LOCATION—SYSTEM 80
USED ON	
DRAWN / APPROVED / DATE	C-19829

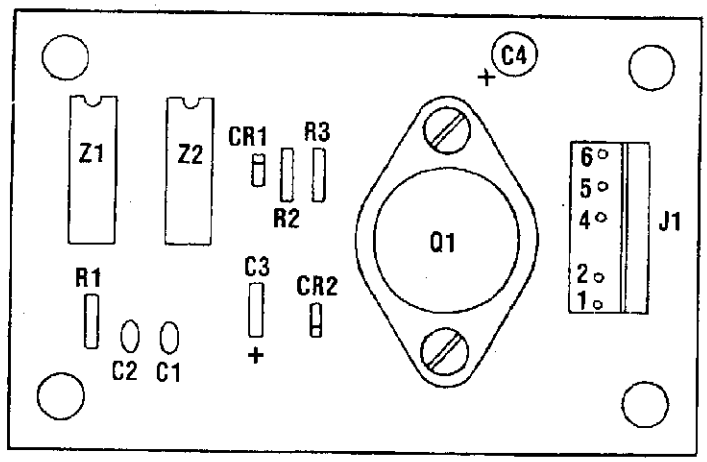
SOUND BOARD

PART NUMBER	DESCRIPTION
	RESISTOR—2.7KΩ, ¼W, 5%—(R1, R2, R7)
	RESISTOR—2.7Ω, ¼W, 5%—(R9)
	RESISTOR—6.8KΩ, ¼W, 5%—(R10)
	RESISTOR—430Ω, ½W, 5%—(R11)
	RESISTOR—2.7MΩ, ¼W, 5%—(R3)
	RESISTOR—1.8MΩ, ¼W, 5%—(R4)
	RESISTOR—22.1KΩ, ¼W, 1%—(R12)
	RESISTOR—10KΩ, ¼W, 5%—(R6)
	RESISTOR—5.6KΩ, ¼W, 5%—(R8)
	RESISTOR—270KΩ, ¼W, 5%—(R5)
	RESISTOR—47KΩ, ¼W, 5%—(R13)
	CAPACITOR—0.01 MICROFARAD, 100V, 20%—KEMET—(C1-C5)
	CAPACITOR—47 MICROFARAD, 25V—(C7, C9)
	CAPACITOR—470 MICROFARAD, 25V—(C8)
	CAPACITOR—0.1 MICROFARAD, 100V, 20%—KEMET—(C6, C10, C13, C17)
	CAPACITOR—10 PICOFARAD, 1000V, 5%—(C11)
	CAPACITOR—100 PICOFARAD, 250V, 20%—(C12)
	CAPACITOR—0.047 MICROFARAD, 25V, 20%—(C15)
	CAPACITOR—0.0033 MICROFARAD, 50V, 20%—(C16)
	CAPACITOR—10 MICROFARAD, 25V—(C14)
R6503	IC—CPU—(U1)
R6530C:R3016-11	IC—ROM/RAM/I/O—(U2)
SSS1408-6P	IC—DAC—(U3)
HM7643-5	IC—PROM—(U4)
NE555P	IC—TIMER—(U8)
SN7404N	IC—INVERTER—(U6, U7)
LM380N	IC—AMPLIFIER—(U5)
1N4004	DIODE—(CR1-CR4)
1N4742A	ZENER DIODE—12V, 1W, 5%—(CR5)
1N270	DIODE—(CR6)
76SB02	2 POSITION DIP SWITCH—(S1, S2)
EVQ-PAR-11K	PUSH BUTTON SWITCH—(S3)
640359-1	SOCKET, 18 PIN (PROM SOCKET)

A8 POP BUMPER DRIVER BOARD SCHEMATIC



NOTE: UNLESS OTHERWISE SPECIFIED,
1. RESISTORS ARE ¼W, 5%
2. CAPACITORS ARE 0.01, MFD. 100V, 20%
3. DIODES ARE 1N4148
4. ASSEMBLY NUMBER A-19741



POP BUMPER DRIVER BOARD

PART NUMBER	DESCRIPTION
	CAPACITOR—47 MICROFARAD, 10V—(C4)
	CAPACITOR—0.01 MICROFARAD, 100V, 20%—(C1, C2)
	CAPACITOR—4.7 MICROFARAD, 10V, 10%—(C3)
	RESISTOR—1.5KΩ, ¼W, 5%—(R1)
	RESISTOR—12KΩ, ¼W, 5%—(R2)
	RESISTOR—220Ω, ¼W, 5%—(R3)
1N4148	DIODE—(CR1, CR2)
SN74121N	IC—(Z1)
SN7416N	IC—(Z2)
PMD10K60	TRANSISTOR—LAMBDA—(Q1)
09-65-1061	CONNECTOR—(J1)

APPENDICES

A. CABLE CONNECTOR WIRE ASSINGMENTS

B. SYSTEM 80 LSI DEVICES
   - 6502 MICRO PROCESSOR
   - 2332 ROM MEMORY
   - 7641 PROM MEMORY
   - 5101 RAM MEMORY
   - 6532 RAM—INPUT-OUTPUT—TIMER (RIOT)

APPENDIX A CABLE CONNECTOR WIRE ASSIGNMENTS

A1-J1

PIN	WIRE COLOR	FUNCTION
1	*688	+5VDC
2	*688	+5VDC
3	—	SPARE
4	*54	GROUND
5	*54	GROUND

A1-J2

PIN	WIRE COLOR	FUNCTION
1	300	aA
2	311	bA
3	322	cA
4	333	dA
5	344	eA
6	355	fA
7	366	gA
8	377	hA
9	600	aB
10	611	bB
11	622	cB
12	633	dB
13	644	eB
14	655	fB
15	666	gB
16	677	hB
17	800	aC
18	811	bC
19	822	cC
20	833	dC
21	844	eC
22	855	fC
23	866	gC
24	877	hC

A1-J3

PIN	WIRE COLOR	FUNCTION
1	400	D1
2	411	D2
3	422	D3
4	433	D4
5	444	D5
6	455	D6
7	466	D7
8	477	D8
9	700	D9
10	711	D10
11	722	D11
12	733	D12
13	744	D13
14	755	D14
15	766	D15
16	777	D16
17	—	SPARE

A1-J4

PIN	WIRE COLOR	FUNCTION
1	*54	GROUND
2	*688	+5VDC
3	9	DS2
4	9	LD3
5	9	LD4
6	9	LD2
7	9	LD1
8	—	SPARE
9	—	SPARE
10	—	SPARE
11	—	SPARE
12	—	SPARE
13	—	SPARE
14	—	SPARE
15	—	SPARE
16	—	SPARE
17	—	SPARE
18	—	KEY
19	—	SPARE
20	—	SPARE
21	9	KNOCKER
22	9	3RD COUNTER
23	9	2ND COUNTER
24	9	1ST COUNTER
A	*54	GROUND (SPARE)
B	*688	+5VDC (SPARE)
C	9	DS1
D	9	DS4
E	9	DS3
F	9	DS6
H	9	DS5
J	9	DS8
K	9	DS7
L	9	DS10
M	9	DS9
N	9	DS11
P	9	DS12
R	9	SOLENOID 5
S	9	SOLENOID 1
T	9	OUTHOLE
U	9	SOLENOID 6
V	—	(KEY)
W	—	SPARE
X	9	SOLENOID 2
Y	9	SOUND 8
Z	9	SOUND 4
A	9	SOUND 2
B	9	SOUND 1

ALL WIRES #22 GAUGE UNLESS SPECIFIED* (18 GA.)

A1-J5

PIN	WIRE COLOR	FUNCTION
1	677	RETURN 7
2	400	STROBE 0
3	411	STROBE 1
4	422	STROBE 2
5	433	STROBE 3
6	*444	STROBE 4
7	455	STROBE 5
8	666	RETURN 6
9	477	STROBE 7
10	700	SLAM SW.

A1-J6

PIN	WIRE COLOR	FUNCTION
1	400	STROBE 0
2	411	STROBE 1
3	422	STROBE 2
4	433	STROBE 3
5	444	STROBE 4
6	455	STROBE 5
7	466	STROBE 6
8	477	STROBE 7
9	9	GROUND
10	600	RETURN 0
11	611	RETURN 1
12	622	RETURN 2
13	633	RETURN 3
14	644	RETURN 4
15	655	RETURN 5
16	666	RETURN 6
17	677	RETURN 7
18	688	+5VDC
19	—	SPARE

A2-J1

PIN	WIRE COLOR	FUNCTION
1	(#16GA) 200	12VDC
2	(#16GA) 54	GROUND
3	—	SPARE
4	—	(KEY)
5	688	+5VDC
6	166	+5VDC offset
7	100	60V
8	111	60V RETURN
9	133	+8VDC offset

A2-J2

PIN	WIRE COLOR	FUNCTION
1	*688	+5VDC
2	*688	+5VDC
3	*54	GROUND
4	*54	GROUND
5	—	(KEY)
6	—	SPARE

A2-J3

PIN	WIRE COLOR	FUNCTION
1	044	+60VDC
2	—	(KEY)
3	055	+42VDC
4	54	GROUND
5	54	GROUND
6	688	+5VDC (SPARE)
7	688	+5VDC

A3-J1

PIN	WIRE COLOR	FUNCTION
1	*54	GROUND
2	*688	+5VDC
3	9	DS2
4	9	LD3
5	9	LD4
6	9	LD2
7	9	LD1
8	—	SPARE
9	—	SPARE
10	—	SPARE
11	—	SPARE
12	—	SPARE
13	—	SPARE
14	—	SPARE
15	—	SPARE
16	—	SPARE
17	—	SPARE
18	—	SPARE
19	—	(KEY)
20	—	SPARE
21	9	KNOCKER
22	9	3RD COUNTER
23	9	2ND COUNTER
24	9	1ST COUNTER
A	*54	GROUND (SPARE)
B	*688	+5VDC (SPARE)
C	9	DS1
D	9	DS4
E	9	DS3
F	9	DS6
H	9	DS5
J	9	DS8
K	9	DS7
L	9	DS10
M	9	DS9
N	9	DS11
P	9	DS12
R	9	SOLENOID 5
S	9	SOLENOID 1
T	9	OUTHOLE
U	9	SOLENOID 6
V	—	SPARE
W	—	(KEY)
X	9	SOLENOID 2
Y	9	SOUND 8
Z	9	SOUND 4
A	9	SOUND 2
B	9	SOUND 1

ALL WIRES #22 GAUGE UNLESS SPECIFIED* (18 GA.)

A3-J2

PIN	WIRE COLOR	FUNCTION
1	588	SHOOT AGAIN LAMP
2	500	PLAYER 1 LAMP
3	511	PLAYER 2 LAMP
4	533	PLAYER 4 LAMP
5	522	PLAYER 3 LAMP
6	*54	GROUND
7	577	HIGH GAME TO DATE LAMP
8	566	GAME OVER LAMP
9	—	SPARE
10	—	SPARE

A3-J3

PIN	WIRE COLOR	FUNCTION
1	*54	SPARE GROUND
2	777	L43
3	755	L41
4	744	L40
5	544	L32
6	555	L33
7	577	L35
8	—	KEY
9	344	L24
10	355	L25
11	377	L27
12	366	L26
13	144	L16
14	155	L17
15	177	L19
16	166	L18
17	(16GA) 54	GROUND (L20-L27)
18	322	L22
19	333	L23
20	311	L21
21	300	L20
22	122	L14
23	133	L15
24	111	L13
25	100	L12
A	*54	SPARE GROUND
B	*688	+5VDC (SPARE)
C	*54	GROUND (L44-L51)
D	800	L44
E	844	L48
F	811	L45
H	855	L49
J	—	KEY
K	566	L34
L	—	SPARE
M	833	L47
N	877	L51
P	822	L46
R	866	L50

continued

A3-J3 continued

PIN	WIRE COLOR	FUNCTION
S	*54	GROUND (L40-L43)
T	766	L42
U	(16GA) 54	GROUND (L28-L35)
V	522	L30
W	533	L31
X	511	L29
Y	500	L28
Z	(16GA) 54	GROUND (L12-L19)
Ā	288	GAME OVER RELAY
B̄	277	TILT RELAY
C̄	588	SHOOT AGAIN LAMP

A3-J4

PIN	WIRE COLOR	FUNCTION
1	700	L36
2	711	L37
3	733	L39
4	722	L38
5	*54	GROUND (L36-L39)
6	*211	SOLENOID 5
7	*266	SOLENOID 1
8	*244	OUTHOLE (SOL. 9)
9	*54	GROUND (SOL. 1, 9)
10	*54	GROUND (SOL. 2)
11	*54	GROUND (SOL. 6)
12	*233	SOLENOID 6
13	*200	SOLENOID 2
14	*54	GROUND (SOL. 5)
15	*54	SPARE GROUND

A3-J5

PIN	WIRE COLOR	FUNCTION
1	733	SOUND 4
2	877	COIN LOCKOUT COIL
3	54	GROUND (KNOCKER)
4	688	+5VDC (SPARE)
5	722	SOUND 2
6	711	SOUND 1
7	744	SOUND 8
8	888	KNOCKER

A3-J6

PIN	WIRE COLOR	FUNCTION
1	633	2ND COUNTER
2	644	3RD COUNTER
3	655	1ST COUNTER
4	54	GROUND

ALL WIRES #22 GAUGE UNLESS SPECIFIED* (18 GA.)

1A4-J1

PIN	WIRE COLOR	FUNCTION
1	455	D6
2	444	D5
3	433	D4
4	422	D3
5	411	D2
6	400	D1
7	377	hA
8	366	gA
9	355	fA
10	344	eA
11	333	dA
12	322	cA
13	311	bA
14	300	aA
15	122	5VAC
16	144	5VAC RETURN
17	044	+60VDC
18	—	SPARE
19	54	GROUND

2A4-J1

PIN	WIRE COLOR	FUNCTION
1	733	D12
2	722	D11
3	711	D10
4	700	D9
5	477	D8
6	466	D7
7	377	hA
8	366	gA
9	355	fA
10	344	eA
11	333	dA
12	322	cA
13	311	bA
14	300	aA
15	122	5VAC
16	144	5VAC RETURN
17	044	+60VDC
18	—	SPARE
19	54	GROUND

3A4-J1

PIN	WIRE COLOR	FUNCTION
1	455	D6
2	444	D5
3	433	D4
4	422	D3
5	411	D2
6	400	D1
7	677	hB
8	666	gB
9	655	fB
10	644	eB
11	633	dB
12	622	cB
13	611	bB
14	600	aB
15	122	5VAC
16	144	5VAC RETURN
17	044	+60VDC
18	—	SPARE
19	54	GROUND

4A4-J1

PIN	WIRE COLOR	FUNCTION
1	733	D12
2	722	D11
3	711	D10
4	700	D9
5	477	D8
6	466	D7
7	677	hB
8	666	gB
9	655	fB
10	644	eB
11	633	dB
12	622	cB
13	611	bB
14	600	aB
15	122	5VAC
16	144	5VAC RETURN
17	044	+60VDC
18	—	SPARE
19	54	GROUND

ALL WIRES #22 GAUGE UNLESS SPECIFIED* (18 GA.)

A5-J1

PIN	WIRE COLOR	FUNCTION
1	—	SPARE
2	777	D16
3	766	D15
4	—	SPARE
5	755	D14
6	744	D13
7	822	cC
8	811	bC
9	877	hC
10	866	gC
11	855	fC
12	844	eC
13	833	dC
14	800	aC
15	155	3vAC
16	177	3vAC RETURN
17	055	+42vDC
18	688	+5vDC
19	54	GROUND

A6-J1

PIN	WIRE COLOR	FUNCTION
1	200	+12vDC
2	—	SPARE
3	333	AC
4	344	AC RETURN
5	688	+5vDC
6	54	GROUND
7	011	SPEAKER OUTPUT
8	711	SOUND 1
9	722	SOUND 2
10	—	SPARE
11	733	SOUND 4
12	744	SOUND 8

A7-J1/P1

PIN	WIRE COLOR	FUNCTION
1	677	RETURN 7
2	500	STROBE 0
3	511	STROBE 1
4	533	STROBE 3
5	522	STROBE 2
6	544	STROBE 4
7	555	STROBE 5
8	—	SPARE
9	—	SPARE
10	700	ANTI-CHEAT SW.
11	9	ANTI-CHEAT SW. (GND)
12	*54	EARTH GROUND

A7-J2/P2

PIN	WIRE COLOR	FUNCTION
1	*066	COIN CHUTE LIGHTS
2	*000	COIN CHUTE LIGHTS RETURN
3	*055	LEFT FLIPPER SWITCH
4	*388	FLIPPER SWITCH RETURN
5	222	+24vDC
6	877	COIN LOCKOUT

A7-J3/P3

PIN	WIRE COLOR	FUNCTION
1	*122	5VAC
2	*144	5VAC RETURN
3	155	3VAC
4	177	3VAC RETURN
5	*54	LAMP GROUND
6		SPARE
7	(16GA) 077	6.3 VAC
8	(16GA) 000	6.3 VAC RETURN
9	*255	+6vDC

A7-J4/P4

PIN	WIRE COLOR	FUNCTION
1	*54	GROUND
2	*54	GROUND
3	*54	GROUND
4	*54	GROUND
5	*54	GROUND
6	*54	GROUND
7	*54	GROUND
8	*54	GROUND
9	*54	GROUND
10	*54	GROUND
11	*54	GROUND
12	—	SPARE

A7-J5/P5

PIN	WIRE COLOR	FUNCTION
1	(16GA) 255	+6 VDC
2	(16GA) 54	GROUND
3	(16GA) 54	GROUND
4	(16GA) 54	GROUND
5	(16GA) 54	GROUND
6	(16GA) 222	+24VDC
7	*388	FLIPPER SW. RETURN
8	*388	FLIPPER SW. RETURN
9	*055	LEFT FLIPPER SWITCH
10	*044	RIGHT FLIPPER SWITCH
11	(16GA) 066	6.3VAC
12	(16GA) 000	6.3VAC RETURN
13	*277	25VAC
14	*288	25VAC RETURN
15	—	SPARE

ALL WIRES #22 GAUGE UNLESS SPECIFIED* (18 GA.)

A7-J6/P6

PIN	WIRE COLOR	FUNCTION
1	011	MATCH LIGHT
2	022	TILT LIGHT
3	033	BALL IN PLAY LIGHT
4	—	SPARE

A7-J7/P7

PIN	WIRE COLOR	FUNCTION
1	400	STROBE 0
2	433	STROBE 3
3	477	STROBE 7
4	666	RETURN 6
5	677	RETURN 7
6	(#16GA) 54	GROUND
7	—	SPARE
8	777	AC INPUT
9	788	AC INPUT

A7-J8/P8

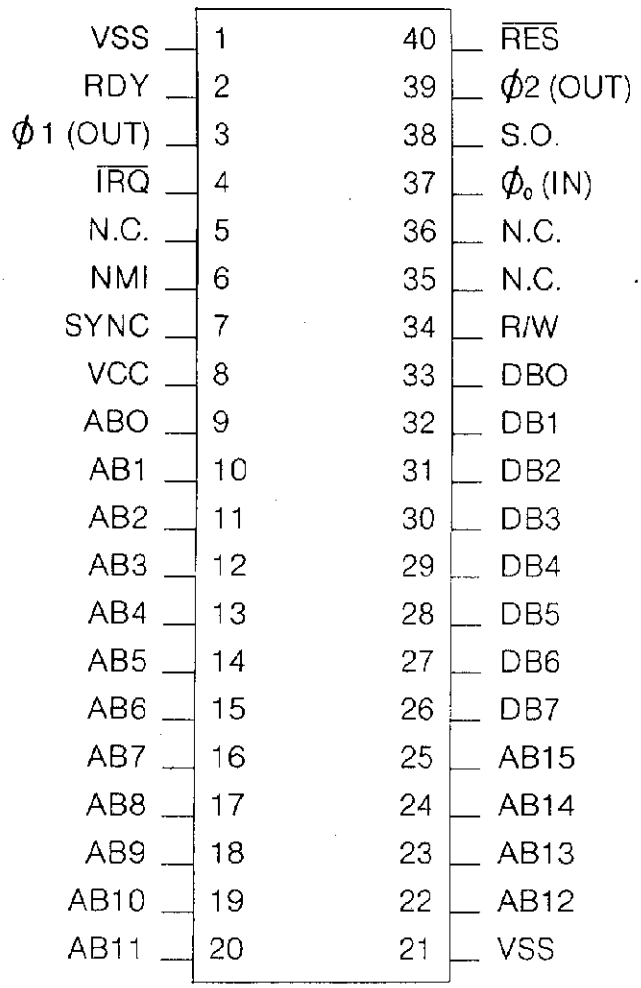
PIN	WIRE COLOR	FUNCTION
1	022	SPEAKER
2	*54	GROUND
3	*54	EARTH GROUND
4	—	SPARE

1A8-J1

Number of Pop Bumper Driver Boards vary from game to game. See Game Instruction Manual for Pop Bumper Driver Board Wire Designations.

ALL WIRES #22 GAUGE UNLESS SPECIFIED* (18 GA.)

APPENDIX B SYSTEM 80 LSI DEVICES
6502 MICRO PROCESSOR



A0 TO A15 — 16 address lines, designated in hexadecimal notation in 4 groups of 4 lines.

D0 TO D7 — 8 data lines—bi-directional—designated in hex in 2 groups of 4 lines.

RESET — Low to reset system, high to run.

IRQ — Interrupt request—high for normal program sequence—low when one of the RIOT's requests an interrupt.

NMI — Non maskable interrupt—low to interrupt—not used in this system.

READY — An input to the processor, which, when taken low, will stop the system on the next read cycle.

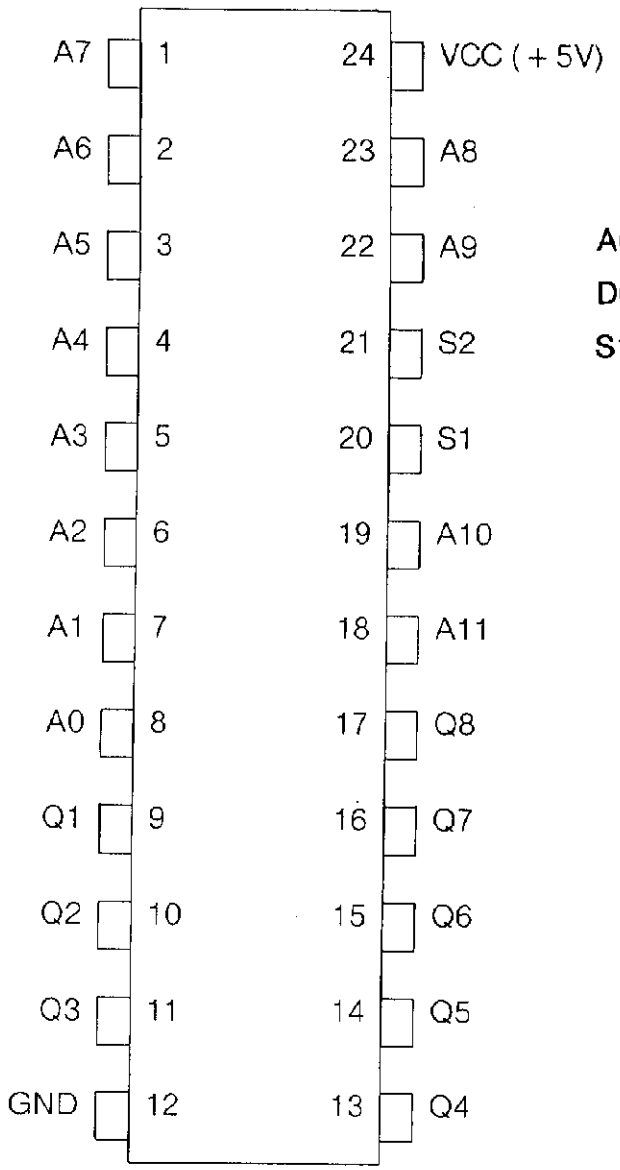
R/W — Read write line. High to read, low to write. Instructs RAM and RIOT's whether data on the bus is being written or being read.

SYNC — An output which goes high each time the μP starts an OP code.

φ0-φ2 — Clock circuit. O0 is input from the crystal. φ2 is output to RIOTs.

2332 ROM MEMORY

4K X 8 ORGANIZATION



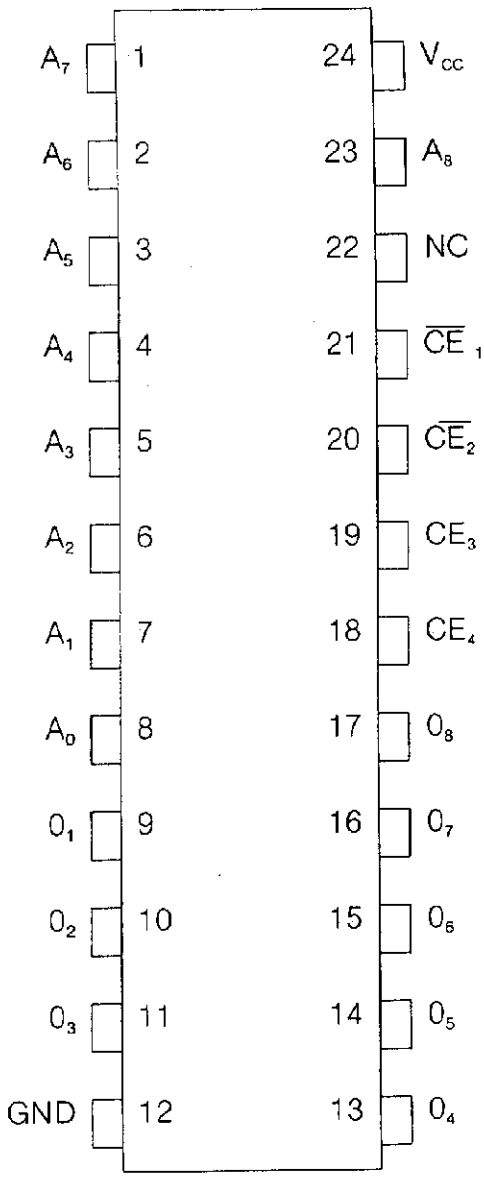
A0-A11 — 12 address lines.

D0-D7 — 8 data lines.

S1-S2 — Chip select lines—both high to enable chip.

7641 PROM MEMORY

CONFIGURATION 512 X 8



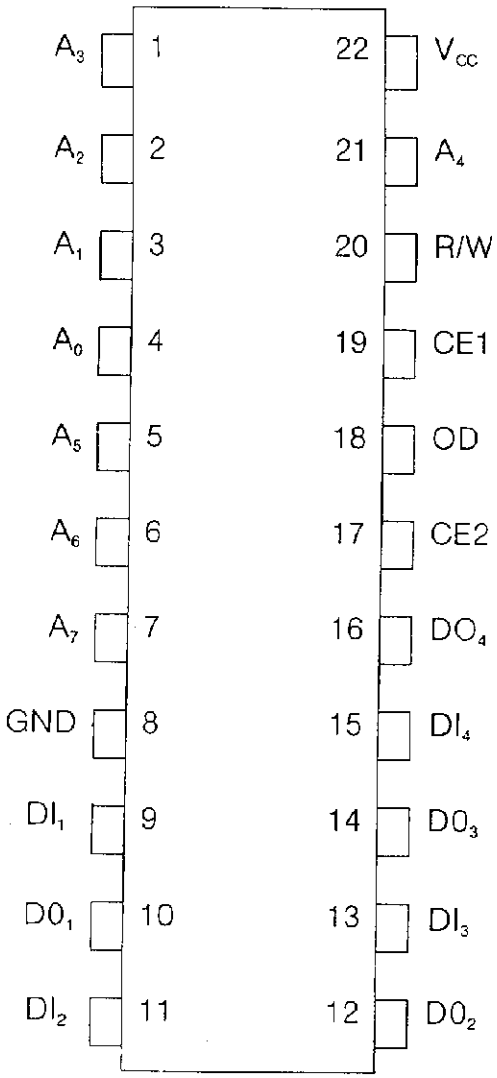
$\overline{CS1}$ - $\overline{CS2}$ — 4 chip select lines. 1 and 2 low and
CS3 - CS4 3 and 4 high to select.

A0-A8 — Address bus.

D0-D7 — Data bus.

5101 RAM MEMORY

256 X 4 CONFIGURATION



$\overline{CE1}$ — Chip enable—low to enable RAM—does not disable input and output buffers.

CE2 — Chip enable—low to disable RAM and place it in low power standby.

OD — Output disable—places outputs in 3 state configuration "OFF"—high to disable.

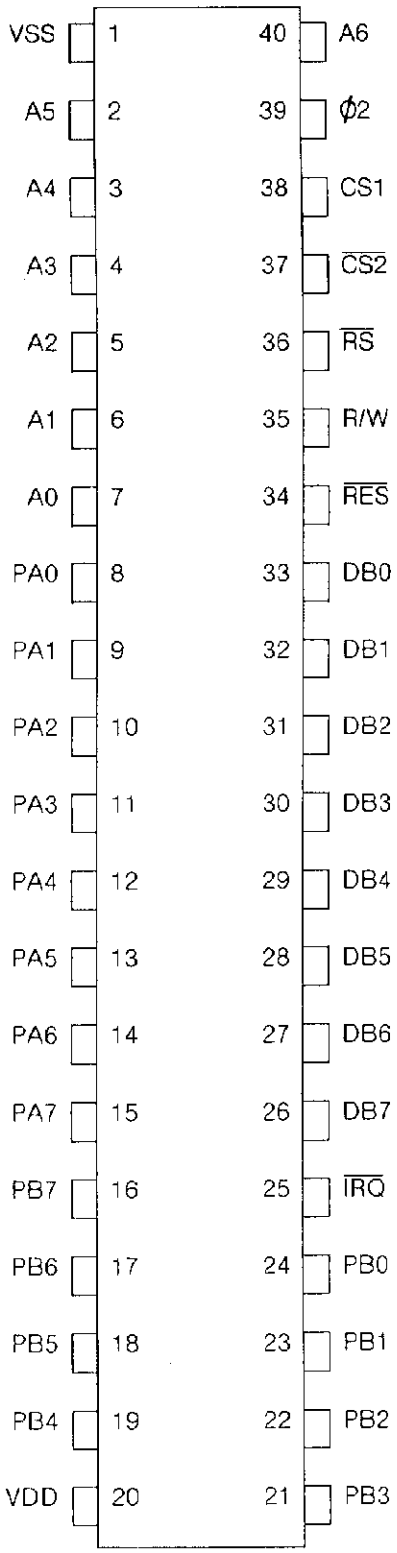
R/W — Read/Write control. High to read RAM—low to write into RAM.

DI-1-DI-4 — Data in lines 1 thru 4.

D0-1-D0-4 — Data out lines 1 thru 4.
The data in and data out lines are tied together in this system and the R/W and OD lines are used to control data direction flow.

A0-A7 — Address bus.

6532 RAM—INPUT-OUTPUT—TIMER



CS1- $\overline{\text{CS2}}$ — Chip select lines. CS1 high to select, CS2 low to select.

$\overline{\text{RS}}$ — RAM select—low to select the RAM section of the RIOT.

PB0-PB7 — A group of 8 lines which may be used as inputs or outputs from the system. PB ports are capable of direct drive of Darlington Transistors.

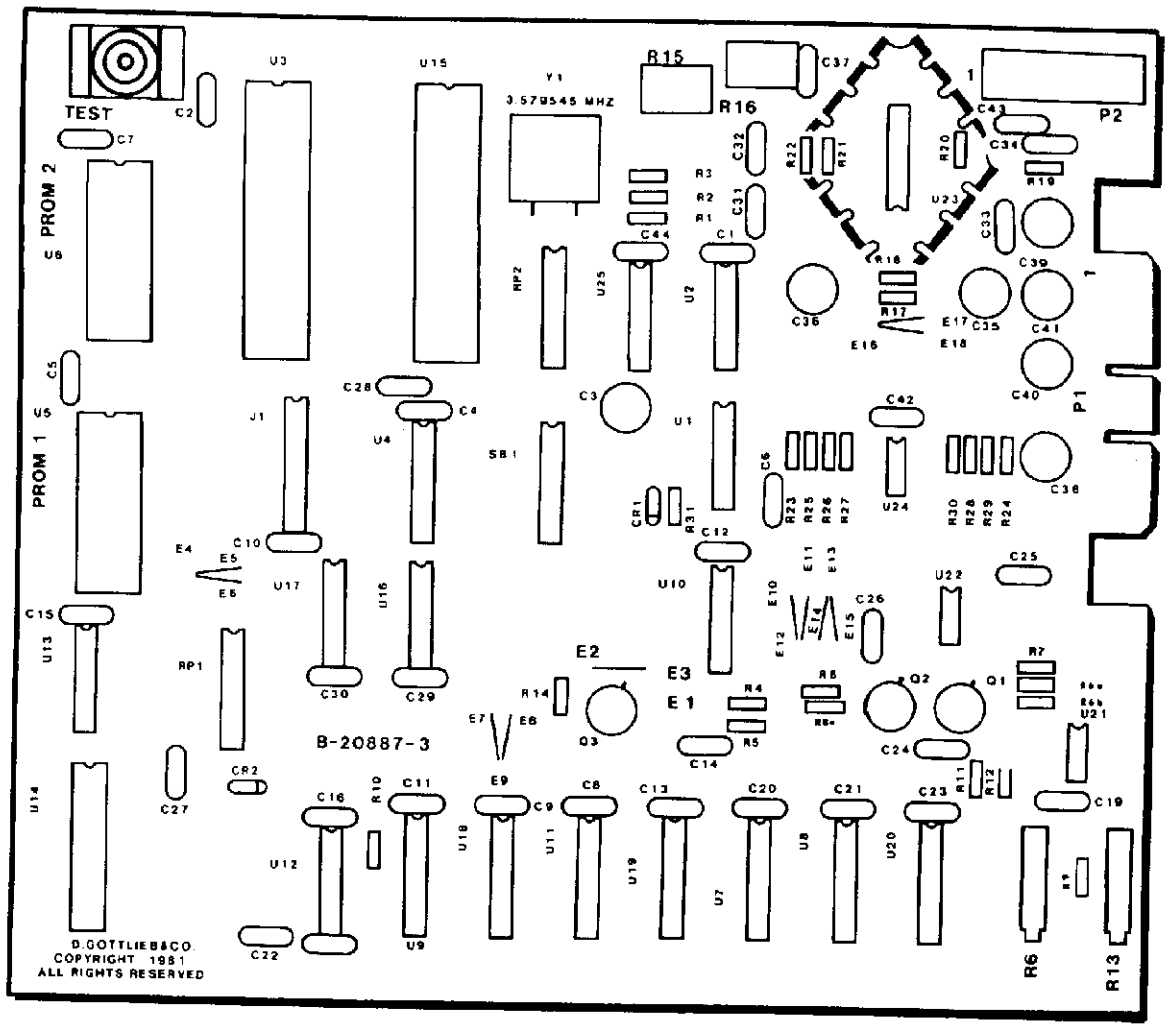
PA0-PA7 — A second group of 8 lines for input/output uses. PA7 can be used as an edge detecting input that generates an interrupt.

A0-A6 — Address bus.

D0-D7 — Data bus.

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

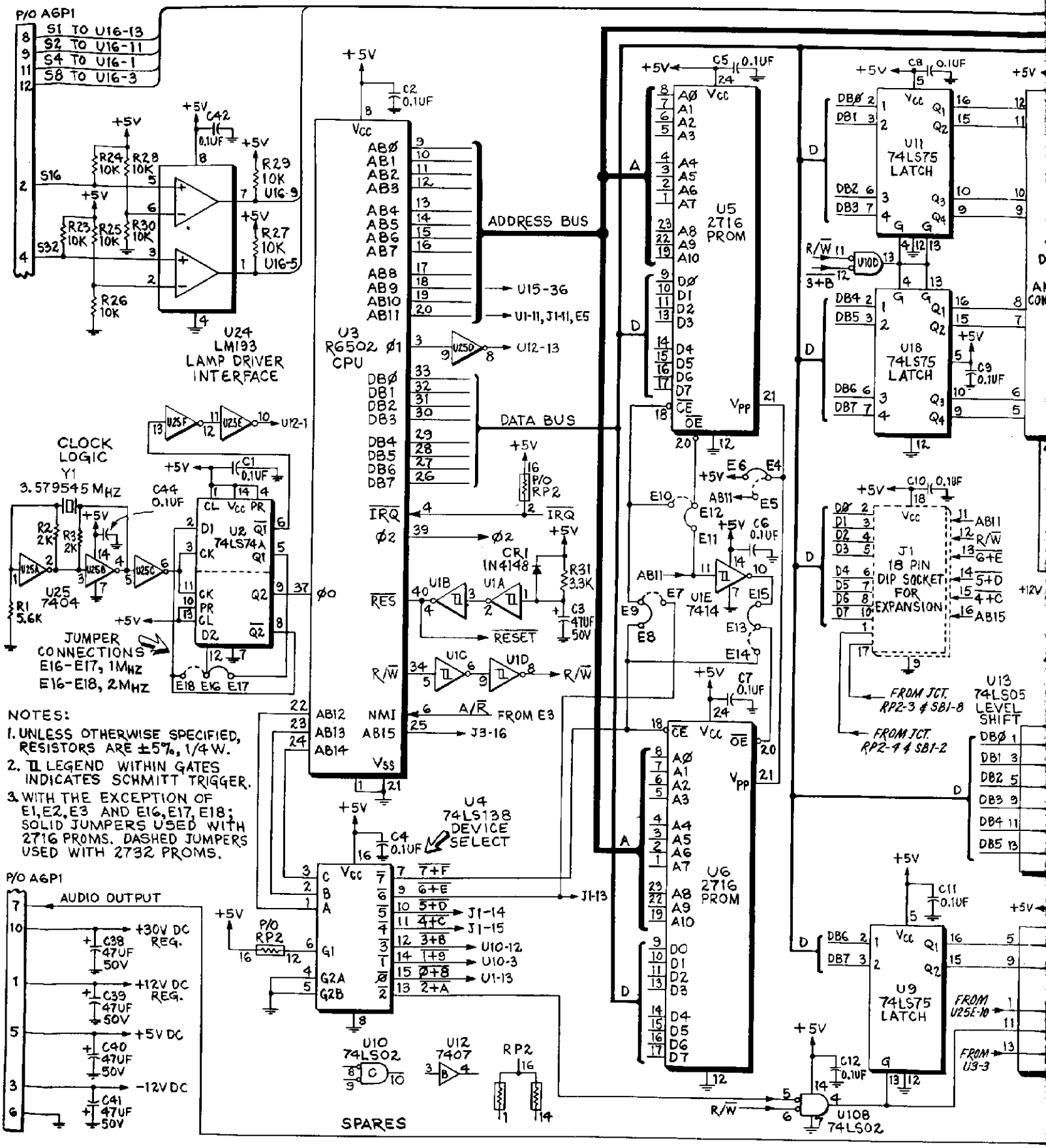
SOUND/SPEECH BOARD (A6) COMPONENT LOCATION

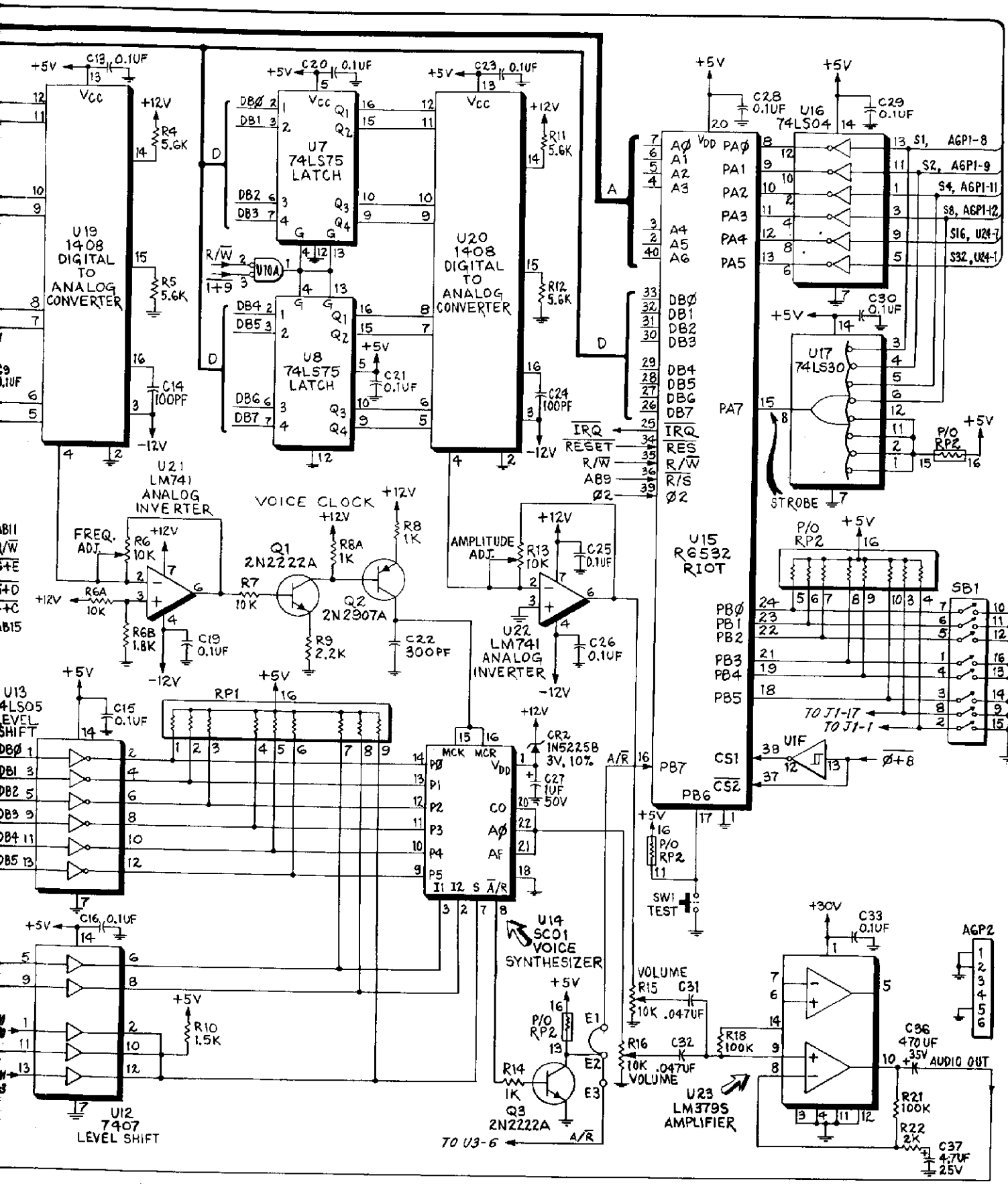


SOUND/SPEECH BOARD (A6) PARTS LIST

REFERENCE	DESCRIPTION	PART NUMBER
C1, C2	Capacitor, .1 UF 25V, CMD	
C4-C13, C15, C16, C19, C20, C21, C23 C25, C26, C28-30 C33		
C31-C32 C42, C44	Capacitor, 0.05 MF, 25V, CMD	
C37	Capacitor, 4.7 MF, 25V Tantalum	
C3, C38-C41	Capacitor, 47 MF, 50V	
C14, C24	Capacitor, 100 PF, 250V, 20%	
C22	Capacitor, 300 PF, CMD	
C27	Capacitor, 1 UF, 50V, TNT	
C36	Capacitor, 470 MF, 35V	
CR1	Diode	1N4148
CR2	Diode, Zener	1N5225B
Q1, Q3	Transistor, NPN	2N2222A
Q2	Transistor, PNP	2N2907A
R1, R4, R5, R11, R12	Resistor, 5.6K ohm, 1/4W	
R2, R3	Resistor, 2K ohm, 1/4W, 5%	
R6, R13	Potentiometer, 10K, Bourns	3006-103
R7	Resistor, 10K ohm, 1/4W, 5%	
R8, R8A, R14	Resistor, 1K ohm, 1/4W, 5%	
R6A, R6B	Resistor, 1.8K ohm, 5%, 1/4 watt	
R9	2.2K ohm, 5%, 1/4W	
R10	Resistor, 1.5K ohm, 1/4W, 5%	
R15, R16	Potentiometer, 10K, CTS	X201R

REFERENCE	DESCRIPTION	PART NUMBER
R18, R21	Resistor, 100K ohm, 1/4W	
R22	Resistor, 2K ohm, 1/4W, 5%	
R23-R30	Resistor, 10K ohm, 1/4W	
R31	Resistor, 3.3K ohm, 1/4W, 5%	
RP1, RP2	Resistor, Dip	4116R-002-222
SB1	Dip Switch	1008-692
SW1	Moment Pushbutton Switch	
U1	IC, Trigger	7414
U2	IC	SN74LS74N
U3	CPU	R6502-13
U4	IC	SN74LS138N
U5, U6	E Prom	2716
U7-U9, U11, U18	IC	SN74L75
U10	IC	SN74LS02N
U12	IC	SN7407N
U13	IC, Inverter	SN74LS05N
U14 not used	Voice Chip	SC01
U15	RRIOT	R6532-18
U16	IC	SN74LS04N
U17	IC	SN74LS30N
U19, U20	Converter, PMI	1408A-6P
U21, U22	IC	LM741CP
U23	IC	LM379S
U24	IC, Dual Comparitor	LM193
U25	Inverter	7404
Y1	Crystal, 3.579545 MHZ	
	Socket 22 Pin Dip	
	Socket 24 Pin (2)	640361-3
	Socket 40 Pin (2)	640379-3


P/O A6P1
S1 TO U16-13
S2 TO U16-11
S4 TO U16-1
S8 TO U16-3
U24 LM193 LAMP DRIVER INTERFACE
U3 R6502 CPU
ADDRESS BUS
DATA BUS
U15-36
U1-11, J1-11, E5
U12-13
U12-1
CLOCK LOGIC
Y1 3.579545 MHZ
U25 7404
U2 74LS74A
JUMPER CONNECTIONS
E16-E17, 1MHZ
E16-E18, 2MHZ
U4 74LS138 DEVICE SELECT
U5 2716 PROM
U6 2716 PROM
U11 74LS75 LATCH
U18 74LS75 LATCH
U9 74LS75 LATCH
J1 18 PIN DIP SOCKET FOR EXPANSION
U13 74LS05 LEVEL SHIFT
FROM JCT. RP2-3 & SB1-8
FROM JCT. RP2-4 & SB1-2
FROM U25E-10
FROM U3-3
U10 74LS02
U12 7407
RP2
SPARES
U108 74LS02
NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE ±5%, 1/4 W.
2. LEGEND WITHIN GATES INDICATES SCHMITT TRIGGER.
3. WITH THE EXCEPTION OF E1, E2, E3 AND E16, E17, E18; SOLID JUMPERS USED WITH 2716 PROMS. DASHED JUMPERS USED WITH 2732 PROMS.
P/O A6P1
AUDIO OUTPUT
+30V DC REG.
+12V DC REG.
+5V DC
-12V DC



D. GOTTLIEB & CO.	
TITLE	SOUND/SPEECH BOARD A6
USED ON	
DRAWN	APPROVED 4-23-81 E-21337