

## TROUBLESHOOTING Q\*BERT

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Foreground on the Gottlieb GG-III Video System is generated on a 16x16 pixel format. Foreground characters can be moved to any point on the CRT with each having its own priority scheme in relationship to the other foreground characters. The foreground characters consist of: The word "Q\*Bert" on the instruction frame, all moving characters, the large letters for highest score on the high score table, Q\*Bert's balloon that appears when he collides with an enemy and the level number that is displayed between levels.

Background is generated on an 8x8 pixel format and is behind all foreground with the exception of a priority switch (when Q\*Bert falls off behind the pyramid).

<b><u>SYMPTOMS</u></b> <b><u>FOREGROUND</u></b>	<b><u>POSSIBLE CAUSES</u></b>
No Foreground Characters On Screen	D2, E1-E, E2-3, E4, G8, J10, J12, K11
Foreground Characters Divided Horiz. and Stacked On Top of Each Other	G17, H10, L12
Two Separate Characters Appear Stacked Vertically	E1-2, E2-3, E4
The Word " Q*Bert" Is Separated Into Sections	SIP 71
The Word " Q*Bert" Appears As Hex Numbers	J1, J2, K5
Incorrect Characters Appear (i.e., Slick In Place of Q*Bert)	E1-2, E2-3, E4, G4, J1, K1-K3
Foreground Characters Are Blurry (Distorted)	F5
Horizontal Lines Through Foreground Characters	K10, L7-8
Uneven Movement of Characters	SIP 72, SIP 73, H3, H4
Right Half of Character Appears On The Left Side of The Same Character	F5
Vertical Line Above Q*Bert That Blanks Everything Above Q*Bert	H3
Foreground Divided Vertically (Mirror Image of Self)	G17
Foreground Frozen (No Movement)	E1-2
Incorrect Foreground Colors	G13, G14, G15, H12, K5, K10, Q82-Q87
Characters Appear As Colored Squares	K1-K6, K7-8, L4-5, L5-6, L6-7, L7-8
<b><u>BACKGROUND</u></b>	<b><u>POSSIBLE CAUSES</u></b>
No Background Characters on Screen	D5, D10, E8, E10-11, E11-12, E13, G6, J7, J8, J12
Incorrect Letters Generated on the Screen	E10-11
Purple Square Appears At Bottom of Letters	L10
Distorted Letters On Top Half of the Screen	D9
Random Letters Flashing Randomly On Screen	D11, E7, E8, E9-10, J8
Background Characters Are Blurry (Distorted)	E10-11, E11-12, E13
Jumbled Background	E10-11, E11-12, E13
Pyramid Divided Into Several Vert. Sections	E10-11, E16
Horiz. Lines Divide Characters	G11
Green Background When Q*Bert is Smashed	G15
Incorrect Background Colors	G13, G14, G15, Q82-Q87

It is no secret that solid state hardware does sometimes become defective. It is for this reason that the accompanying table of symptom/possible causes can be helpful when troubleshooting the Gottlieb GG-III Logic Board. A note to remember - this list has been compiled to assist the technician in troubleshooting the Logic Board. The list of possible faults is not always definitive.

The Intel 8088 microprocessor is a third generation microprocessor with an 8-bit data bus to memory and to I/O (Input/Output). The chip is a standard 40-pin dual inline package and operates from a single +5VDC power source. The 8088 is extremely flexible in its application and is well suited for use in the GG-III System.

The processor has dual operating modes (minimum and maximum) which is allowed by dual function pins selected by a strapping pin. The GG-III System utilizes the minimum mode of operation. In this mode, these dual function pins transfer control signals directly to memory and I/O devices.

The high efficiency of the 8088 is conducive to combining a 16-bit internal bus with a pipeline architecture allowing instructions to be prefetched during spare bus cycles. Microprocessors execute a program by repeating the simplified cycle shown below:

1. Fetch the next instruction from memory.
2. Read the operand (if required by the instruction).
3. Execute the instruction.
4. Write the results (if required by the instruction).

These steps are usually performed serially by most microprocessors. The architecture of the 8088 however, allocates these steps to two separate processing units within the CPU. The execution unit executes instructions while the bus interface unit fetches instructions, reads operands and writes results. Both units work independently of each other and are able to overlap instruction fetch with execution. This means that the time required to fetch an instruction, during normal program sequence, disappears because the execution unit executes instructions that have already been fetched by the bus interface unit.

Below are listed several of the functions allowed by the minimum mode of the Intel 8088 microprocessor as applied to the GG-III System: The NMI (Non-Maskable Interrupt), pin 17, will receive pulses 61 times a second. The pulse is generated when the CRT's vertical blanking time begins. During this blanking time the background register (E7) transfers data to the background buffer (E10-11) through DMA (Direct Memory Access) for the next frame. The DT/R (Data Transmit/Receive), pin 27, controls the direction of data flow via the Data Transceivers (C4) DIR (Direction Control Input) pin. This allows data to flow from the A bus to the B bus or from the B bus to the A bus. The DEN (Data Enable), pin 26, allows or disables data flow by placing a voltage level on the G (Enable Input), pin 19, on the Data Transceiver (C4) so that the bus is effectively isolated. The RD (Read Control), pin 32, manages the OE (Output Enable) of the program ROM's as well as enabling the output of the Background Character Register (E7) and the Input Port Select (B10). The IO/M (IO/Memory Control), pin 28, is utilized to differentiate between either program memory or I/O on the processors bus. The WR

(Write Control), pin 29, controls the read/write function of the system RAM as well as clocking the Output Port Flip Flops (A8, A9, A10).

This is a general pin function description that can be utilized when troubleshooting the GG-III System. The other pins on the microprocessor are all self explanatory.

## **FOREGROUND**

Foreground generation on the GG-III System is initiated with three foreground registers (E1-2, E2-3, E4) all addressed via the microprocessor through program control. These registers are the Foreground Horizontal Position Register (E1-2), the Foreground Object Select Register (E2-3) and the Foreground Vertical Position Register (E4).

When the appearance of an object is required on a scan line, as detected by the Vertical Position Detector, the address generated by the Foreground Horizontal Position Register is copied into the Line Object Position RAM (H1-H4) and the address generated by the Foreground Object Select Register is copied into the Line Object Select RAM (J1-J6). The Line Object Position RAM contains the horizontal position of the object for the next scan line while the Line Object Select RAM contains the address for the Object ROM to address the desired object.

Since the foreground object size is 16 pixels by 16 lines, the Vertical Position Detector must generate enable pulses for 16 successive lines. The high order 4 bits of the Foreground Vertical Position Register and the Vertical Counter are summed (E5) and feed the Line RAM Enable Pulse Generator (E6, J8). When the sum values of E5 are all high, the write enable is generated. This pulse enables the transfer of data from the Foreground Horizontal Position Register to the Line Object Position RAM as well as the transfer of data from the Foreground Object Select Register to the Line Object Select RAM via the read/write (WR NOT) signal (FBA4) and the chip select (CS NOT) signal (S2) from the multiplexer (G9). For each pulse generated, information for the next scan line is loaded into the Line RAM. When the Line RAM Enable Pulse Generator generates a pulse, it increments the 5-bit Line RAM Address Counter. This counter produces the addresses for the Line Object Position RAM's.

When the Line Object Position RAM is being read, the 8-bit Line Buffer Address Counter (H5, H6) is loaded (every 1.6 usec). Before any new horizontal information can be loaded into the Line RAM, the counter must increment 16 times in order to address the 16 pixels that the foreground object will occupy that frame time.

The low order 4-bits of the Foreground Vertical Position Register and the Vertical Counter are summed (F5) and address the object information to the Foreground Object ROM (K4, K5, K6, K7-8) via the multiplexer (G5) and the Object ROM Address Latches (K1-K3).

The Foreground Object ROM's receive their addressing from three sources: (1) The high order 8-bits from the Foreground Object Select Register, (2) 4-bits from the Vertical Position Detector and (3) The least significant bit (RA0) comes from the 800ns counter (L12). This counter will output every 4 clock cycles. The information out of the Object ROM's is loaded into four

parallel to serial shift registers (L4-5, L5-6, L6-7, L7-8). Every clock cycle the outputs of the four shift registers are checked for data. If any output data, a write enable pulse (K12, K13, K9) is generated allowing data to transfer to the Line Object Buffers.

## BACKGROUND

The Background Character Registers (E7) data is copied into the Background Buffer RAM (E10-11) during the first half of the vertical blanking time through DMA transfer (E9-10). Once the data is read by the Buffer RAM, the Character Register is ready to be loaded with new information. The data in the Buffer RAM is an 8-bit object number. This object number addresses the Background Character ROM (E11-12, E13) which contains pixel definition for the background character. The Character ROM will output 8-bits of information for two pixels for the 8 pixel by 8 line character. The horizontal counter, H1 and H2, and the vertical counter, V0, V1 and V2 are used so that the background object is displayed at the correct vertical and horizontal positions on the screen for each frame.

<b>SYMPTOMS</b>	<b>POSSIBLE CAUSES</b>
Picture Rolls Vertically	D17, E16, E17, F16, J14, J17
Glitching	D3, E5, G7, G9, J6, J16, J17, L13
Missing Colors on Characters	G10, G13-G15, K11-K13, L7-8
Characters Vertically Separated	D15, D16, E4-E6, E15, J2, J5, J6, SIP 71
Incorrect Vertical Position of Characters	E4, F5
Vertical Lines on Screen	J10, J11, K9, K11
Incorrect Horizontal Position of Characters	E1-2, G1-G2, H1-H6, H8, SIP 72
Characters Horizontally Separated	H3, L11, L12
Missing Characters	D3, E2-3, L12
Blank Screen (Black or Blue)	F15-F17, J16-J17
Blurry Characters	E15, E16, G5, J5, J6