

## High Score Memory Circuitry

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5, and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to -29V. When the signal is 0V, CR5 is cutoff and CR4 is forward-biased which causes C84 to develop a charge. C84 charges to approximately -28V. This is the potential required for EAROM C0 to operate.

The MPU addresses the EAROM (AB0-AB5) when a low EAADDR gates WRITE2 at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low EACONTROL gates WRITE2 at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when EAREAD on pin 1 of buffer H4 goes low.

