DRAGONS LAIR TROUBLESHOOTING MANUAL

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CHAPTER 1
THEORY OF OPERATION
FOR THE SYSTEM CONTROLLER

A. Z80

The microprocessor used in this system is a 4 MHz Z80. All of the Z80's address, data, and control outputs are buffered by bus drivers: U2, U9, U15, and U23. These buffers are always enabled.

B. DATA BUS DIRECTION CONTROL

A high Read signal RD- at U15-1 allows the Z80 to write into the RAMs and other external devices. A low RD- sighal allows the transfer of data from the RAMS, ROMS, and other external devices to the Z80.

The Z80 generates sixteen address lines. After buffering, these lines are referred to as AO through A15. AO is the least significant bit, A15 the most significant.

Similarly, after buffering by data bus driver U15, the eight data bus lines are referred to as D0 through D7.

U23 buffers the following four control signals generated by the Z80:

SIGNAL		OCCURRENCE
M1-	MACHINE CYCLE 1	During instruction fetches.
MREQ-	MEMORY REQUEST	When the Z80 reads or writes data from or to memory-mapped devices.
RD-	READ	When the Z80 reads data.
WT-	WRITE	When the Z80 writes data.

NOTE: Bus Acknowledge signal BUSAK- may be wired on some boards but it is never used.

C. Z80 CONTROL LOGIC

This section describes the generation of three control inputs to the Z80: CLOCK+, RESET-, and WAIT-. The control input Bus Request (BUSRQ-) may be wired on some boards, but it is never used.

1. CLOCK CIRCUIT

The Clock Circuit provides the Z80 Controller Board with a stable source of timing, thus insuring, among other things, that all audio sounds remain in tune. Composed of U24, U29, Yl, and other discrete parts, the Clock Circuit consists of an oscillator and several dividers and drivers.

The oscillator is composed of U24, pins 1 through 6, Yl, R45, R46, C54, and C63. The output of the oscillator circuit is 16.000 MHz clock at U24-6. This signal is fed into divider U29-3.

The dividers reduce the oscillator frequency by a factor of four, yielding a frequency of 4.00 Mhz at U29-9. After the frequency undergoes an additional division by two, the dividers generate the clock for the GI sound chip by supplying 2.00 Mhz at U26-5: the 4.00 Mhz output of divider U29-9 is fed to the Z80 at Ul~6 after being redriven by U23, pins 7 and 13.

2. RESET CIRCUIT

The Reset Circuit forces the processor and other registers on the Z80 Board into their proper initial states and prevents the generation of unwanted sounds. The Reset Circuit is activated automatically at power up and manually by pressing the RESET button on the Z80 Controller Board.

The Power-up Reset Circuit is composed of CR1, CR2, R43, R44, C62, Ql, U23, pins 11 and 9, U22, pins 1 through 3.

At power up, the positive side of C62 is very close to 0 volts. This causes Ql to be turned on and the output of the circuit, U23-9, to be high. C62 now begins to charge; i.e., the voltage on its positive side goes from ground to +5V. When the positive side of C62 reaches a potential of approximately 1.4 volts, Ql turns on, forcing U23-9 low. To provide a clean output pulse at U23-9, the pulse width at U23-9 should be in excess of 50 milliseconds.

A Schmidt-Trigger device, U23 has built-in hysteresis. U22, pins 1 through 3 provide an active low RESET at U22-3.

When the RESET button is depressed, C62 de-charges, initiating the RESET Circuit activity described above.

3. WAIT LOGIC

When reading or writing to the GI Sound Chip U19, the Z80 must wait for one Time State, or T-State. For circuit simplicity, a signal generated by U25-6 determines when these states need to be inserted. Sometimes active for other reasons, this signal is always active low whenever the GI Sound Chip is addressed.

The Wait Circuit for the GI Sound Chip is composed of U28 and U2S, pins 1 through 6. A T-State is generated as follows:

The signal at U25-6 is fed to U28-2. U28 is configured as a 2-Bit shift register. Normally, U25-6 remains high, causing U28, pins 5 and 9 to be held high and the WAIT signal at U25-3 to be high/inactive. When the GI Sound Chip is addressed, U25-6 drops low, causing U28-6 to go high, while U28-9 remains high. The WAIT signal then drops low for 250 ns or one T-State.

D. Z80 ADDRESS DECODING

Address decoding is performed by U4, Ull, and U10. U4 decodes address lines 13, 14, and 15. The outputs of U4 select five different banks of ROM, one bank of RAM, and two banks of memory-mapped I/0 devices. Each of these banks is 4K long. Address decoding at U4 is enabled when Memory Request signal MREQ+ is active high at U25-10. It is disabled during Refresh Cycles (RFSH-) by a low at U25~9.

U10 decodes address lines 3, 4, and 5. Its outputs are used to generate Write Strobes to memory-mapped I/0 devices. Also used to decode address lines 3, 4, and 5, Ull generates Read Strobes for memory-mapped I/0 devices.

E. PROM MEMORY

Located on the Personality Board, PROM Memory Ul through U5 contain the program for the game.

F. RAM MEMORY

RAM Memory U3 stores the variables for the Z80 Controller Board. U3 = one 2K block of memory.

G. REAL TIME CLOCK

Interrupts occuring at a rate of approximately 33 milliseconds are required to keep the Z80 in sync with the video disc player. The signal RTC+ (REAL TIME CLOCK) at U26-11 is a square wave with a 33 millisecond period. In early models, this signal is generated by the 68705, U7-12. In later models, U6 and U13 are cascaded to form a 16-Bit binary counter. The output of this counter circuit, U6-6 is a 33 millisecond square wave.

In either case, U26-8 is forced low every 33 milliseconds, thereby generating an interrupt signal to the Z80. When the Z80 recognizes the interrupt signal, it forces both Ml- and the IORQ- signals low simultaneously, causing CLR INT- (CLEAR INTERRUPT) to go low at U25-11, thus removing the interrupt generated at U26-8.

H. GI SOUND CHIP

GI Sound Chip Ul9 generates the boops and beeps for the coin drop and joystick feedback.

Both address words and data words are written by the Z80 to the GI Sound Chip. However, only data words are read from the Sound Chip. Two control inputs on the Sound Chip control all reading and writing between the Z80 and the Sound Chip. When an address word is written into U19, the Write Address signal generated at U10-13 falls low at U22, pins 4 and 10, forcing both control inputs, pins 18 and 20 on U19 high. In a similar fashion, the Write Data signal at U22-5, and the Read Data signal at U22-9 are encoded at U22 to control data transactions between the Z80 and U19.

The GI Sound Chip's input/output ports A and B are always programmed as inputs and are used to read option switches SW1 and SW2.

I. AUDIO AMPLIFIERS

There are two audio channels on the disc player. Channel 1 contains all of the talking: Dirk and Daphne's words and the voice of the attract mode narrator. Channel 2 contains all of the general game sounds: Dirk's grunts, screams, the creatures' noises, and all other background sounds.

U29 amplifies the sounds on Channel 1, U30 the sounds on Channel 2 and the sounds generated by GI Sound Chip U19.

J. COLOR MONITOR

The monitor used in this system is ELECTROHOME model 19MON/NTSC. 115V from the power supply's Isolation Transformer reach the monitor through a 2-pin flying lead. Video signals travel through a COAX cable from the video disc player to P103 of the monitor's NTSC decoder board.

See Chapter 5 for additional information on the monitor and the NTSC Decoder.

K. POWER SUPPLY

There are three versions of the power supply. All of the versions have outputs of +SV DC regulated and +25V unregulated power. The +25V is regulated down to +14V by the Z80 Controller for usage with audio amplifiers U29 and U30. All versions also output of 6.3V AC to the coin door lamps. Some versions have -25V and other outputs that'are not used.

The three versions of the power supply differ also in the number of. fuses, circuit breakers, and capacitors:

Version I: 1 five amp MDL fuse
2 circuit breakers

Version II: 1 five amp MDL fuse
1 circuit breaker
2 capacitors

Version III: 1 five amp MDL fuse
1 two amp AGC fuse for the +25V output
1 two amp AGC fuse for the 6.3V AC output
2 capacitors

NOTE: The first fuse on all versions (F1) should be a five amp MDL,, even if the white silkscreen markings on the PC board say otherwise. If a game appears to lose power, make sure that Fl is a five amp MDL fuse.

L. AUDIO AMPLIFIER POWER SUPPLY

Composed of VR1, Q3, and other discrete components, the Audio Amplifier Power Supply circuit supplies approximately 14 volts to Audio Amplifiers U29 and U30. A 3-terminal voltage regulator chip, VR1 is used to drive the base of Q3 with +15V. Q3 is configured as an emitter-follower. The output of the circuit is the emitter Q3. The voltage at the emitter of Q3 is normally 14.3V.

M. PLAYER INTERFACE

All player controls and the coin switches are read by the Z80 via input registers U8 and U14. All player control inputs are furnished with pull-up resistors and RC de-coupling networks.

N. DISC PLAYER INTERFACE

The disc player interface is composed of U20, U21, and U16. In games with Pioneer 7820 disc players, U16 feeds both the ENTER+ and the INT/EXT signals to the disc player. The signal OUT DISC DATA+ at U16-5 is fed to the output enable pin at U21-1. U21 is used to send control words to the disc player. U20 is not required when communicating with the Pioneer player. Jumper Wl should be installed with the Pioneer player.

In games with the Pioneer LDV-1000 player, the only signal sent to the player from the Z80 is the INT/EXT signal generated at U16-9. The ENTER+ signal is returned from the disc player and is fed to U14-6. U16-5, the output disc data signal, goes high, disabling U21, when the Z80 wishes to read data words from the disc player via U20. Jumper Wl should be removed when using the LDV-1000 player.

0. COIN COUNTER

The mechanical coin counter is controlled by U16-2. When U16-2 is high or disabled, no base current is drawn thru Q2. (Q2 is the coin counter driver transistor). This keeps the coin counter de-energized. When the Z80 wishes to register a coin count, it will drop U16-2 low, thereby drawing base current through Q2, turning Q2 on, and bringing the collector of Q2 to approximately 4.7 volts. After a delay of at least 50 milliseconds, the Z80 will force U16-2 high.

To prevent false coin counts on power-up, U16-1 is connected to RESET+. This connection disables U16 until the program can start running, forcing U16-2 high and de-energizing the coin counter.

P. LED DISPLAY BOARD

The LED Display Board is composed of two identical circuits. Each circuit has eight common anode displays and one multiplexer chip. The following is a description of one of these identical circuits.

The multiplexer chip has a memory of eight words, with four bits to each word. The Z80 writes into any location of this memory by setting appropriate highs and lows on address lines AO through A2. The Z80 selects the character to be written into the memory by placing data on DO through D3, thereby supplying a WRITE pulse to pin 8 of the multiplexer chip. Address lines AO through A2 and data lines DO through D3 are connected to the Z80's address and data bus by a 16~ribbon cable attached to the two boards. Display enable signals DEN1 and DEN2 are generated by address decoder U10, pins 7 and 9 on the Z80 Board.

CHAPTER 2
ON-BOARD DIAGNOSTICS

The on-board diagnostics are a series of tests performed on the system's hardware to verify whether or not the hardware is fully functional. Resident in the Z80A game program EPROM, the diagnostic software routines are initiated by having A7 on Dip Switch 2 in the OFF position when the game is powered up.

Once initiated, the diagnostic program cycles through the following tests. The results of these tests flash consecutively on the monitor display. If further troubleshooting proves to be necessary, see the Service Diagnostic and Signature Analysis Tests in Chapter 4.

A. RAM TEST

Each RAM cell is loaded with 55H and read to insure that all of the cells retained the data. The RAM is then reloaded with OAAH, which causes every bit in every cell to be inverted. The RAM is then read again to verify data retention. If all cells are operating properly, the diagnostics proceed to the EPROM Test.

If a bad cell is found, the system displays "RAM test failed' on the monitor and halts until it receives a reset.

B. EPROM TEST

There are five 8K-byte EPROMs within the system. The Diagnostic program calculates each EPROM's checksum and compares it to pre-stored correct checksum values. If all of the checksums match, the program continues with the security device test. If an EPROM fails, the monitor displays the words "ROM Test Failed" and the address location of the bad EPROM. The correct address locations are listed in the following table:

Checksum no.	Address Location	EPROM Address
1	OFFF6H	OOOOH-1FFFH
2	OFFF8E	2000H-3FFFE
3	OFFFAH	4000H-5FFFH
4	OFFFCH	6000H-7FFFH
5	OFFFEH	8000H-9FFFH

C. SECURITY DEVICE TEST

Disregard this test.

D. SOUND TEST

The program outputs a tone scale to each of the three channels of the GI Sound Chip. Check the volume control while these sounds are playing. If no sound is heard, check the AY-3-8910 Sound Chip.

E. DISPLAY TEST

The seven segment Player 1 and Player 2 displays now cycle through all of their available digits: each display should progress through the numbers 0 through 9. No rating of PASS or FAIL appears on the monitor. Simply watch the displays themselves to ensure that they are operating properly.

F. KEYBOARD TEST

This test checks the operation of the player controls. During the fifteen second period of the test, push all of the player control buttons and operate the joystick. One seven segment display corresponds to each of the controls and to each direction of the joystick. Each time a control is operated, a zero should appear in its corresponding display. The monitor displays the diagram shown below, a table indicating which display corresponds to each control.

PLAYER 1 SCORE

	ACTION	RIGHT	LEFT	DOWN	UP	

PLAYER 2 SCORE

P1	P2	COIN1	COIN2			

G. COLOR TEST

The program now displays the image of a dead Dirk. Adjust the video monitor till the colors in this image are satisfactory. This image stays on the monitor until the A7 on Dipswitch 2 is turned to the ON position.

CHAPTER 3

SERVICE DIAGNOSTICS AND SIGNATURE ANALYSIS FOR THE Z80 CONTROLLER BOARD

The following troubleshooting procedures assume a relatively advanced level of technical expertise.

The first eight tests utilize Diagnostic PROMs and/or a test harness not included in the game package. The Diagnostic PROMs may be purchased from Cinematronics' Customer Service Department. The test harness may be constructed quickly and easily using the guideline below. The last three tests require an Hewlett-Packard 5004A Signature Analyzer.

Diagnostic PROMS:
- LAIR 3
- LAMPCYC2
- MEMB3
- INT TEST 5
- DISC INT 5
- GITF
- GI SCOPE

TEST HARNESS

Use any available wire to assemble a harness with the cable connections listed on the following page. Plug Pl into the Z80 Controller Board, and P2 into the Power Supply.

P1 = Molex 03-09-1364
P2 = Molex 03-09-1122

P1 to --->	P2 to --->	J1 CPU Disc Interface
1		4
2		11
3	9	
4	10	
5		3
6		17
7		
8		
9		2
10		
11		
12		
13		1
14		
15		
16		
17		16
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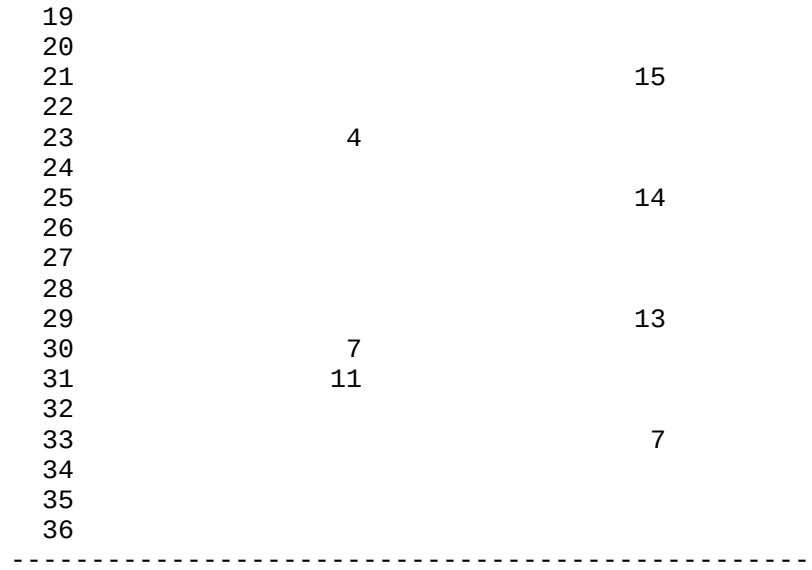

The following pages describe the Diagnostic and Signature Analysis tests. The write-up for each individual test includes:

a.) Reason(s) for running the test.
b.) Instructions for setting up and conducting the test.
c.) Description/explanation of the test itself.

The first test, the "LAIR" GO/NO GO Test, surveys the entire Z80 Controller Board, indentifying general problem areas. The seven "Stand-Alone" Diagnostic tests that follow isolate and troubleshoot the individual problem areas.

All of the Diagnostic tests utilize the game's Credit Display Board in different ways. See Figure 4-1 for a reference illustration of the Credit Display Board.

The two Signature Analysis Procedures that conclude this chapter of the manual serve to locate and correct especially hard-to-find problems in the board, tracing the problems to specific lines, PROMs or circuits.

"LAIR"

GO/NO GO TEST

To prepare for testing, connect the Disc Control Output Cable (24 DIP ribbon) from Jl of the Z80 Controller Board to Jl of the test harness. Remove Ul from the PROM board, and insert the LAIR 3 PROM in the Ul socket. Leave Game PROMs U2-U5 in the board. Power up the boards.

The program in the LAIR 3 PROM automatically cycles through the following series of Go/No Go tests, thus isolating specific problem areas of the Z80 Controller Board for futher testing.

DISPLAY DATA TEST: .

Each display progresses through the same sequence of characters at the same time: the numbers 0 through 9, a dash, the letters E, H, L, P, and a blank. All displays should register identical characters at any given time. Note that a blank is considered to be a character.

If this test fails, the problem may be traced to either the Z80 Microprocessor, the ROM Board, or the displays themselves. Use the Z80 Controller Board Signature Analysis Procedures to find and correct the problem.

DISPLAY ADDRESS TEST:

The numbers 0 through 9, a dash, the letters E, H, L, P, and a blank should appear, in this consecutive order, in displays DS1 through DS16. 0 appears in DS1, 1 in DS2, etc..

Maintaining this order, the entire sequence of characters should then rotate, with a pause between each rotation, until each character has appeared in every display.

If this test fails, the problem may be traced to either the Z80 Microprocessor, the PROM Board, or the displays themselves. Use the Z80 Controller Board Signature Analysis Procedures to find and correct the problem.

After the DISPLAY ADDRESS TEST, the test program automatically runs through the tests coded 00-50. The general areas examined by each of these tests are named in TABLE 1.

While a specific test is running, the two digit code for that test appears in three locations: on DS1 and DS2, on DS9 and DS10, and on DS15 and DS16.

When a specific test passes, a "P" appears on both DS7 and DS8. The remaining eight displays (DS3-DS6 and DS11-DS14) show dashes.

When a test fails, a two digit error code replaces the test code number on DSI and DS2, on DS9 and DS10, and on DS15 and DS16. The message "HELP" is displayed on DS3-DS6 and on DS11-DS14. And, DS7 and DS8 show dashes.

The type of errors represented by the error codes are outlined in TABLE 2. The solutions to these errors are listed in TABLE 3. Note that TABLE 2 breaks down some of the general problem areas listed in TABLE 1. This breakdown occurs automatically within the program to help isolate any problems in the board. If further breakdown, and/or exploration, of a specific area is necessary,

TABLE 3 suggests the running of the 'Stand-Alone", or individual, tests of those areas. The Stand-Alone tests require programs other than that stored in the LAIR 3 PROM.

TESTS 00 through 50:

TABLE 1: TEST NAMES

TEST CODE	TEST
00	Processor Tests
10	ROM Check Sum Test
20	RAM Tests, Data and Address
30	Interrupt Test
40	Disc Interface Test
50	GI Sound Chip Test

TABLE 2: TEST ERROR CODES

TEST NAME	ERROR CODE	TYPE OF FAILURE
Processor Test 1	02	Processor or ROM
Processor Test 2	04	Processor, ROM, or RAM
ROM Check Sum Test of Ul	10	Processor or ROM
ROM Cheek Sum Test of U2	11.	U2 on ROM Board
ROM Check Sum Test of U3	12	U3 on ROM Board
ROM Check Sum Test of U4	13@	U4 on ROM Board
ROM Check Sum Test of U5.	14	US on ROM Board
RAM Test	20	Data Lines
RAM Test	22	Address Lines
Interrupt Test	30	Interrupt too late or nonexistent
Interrupt Test	32	Interrupt too soon
Disc Interface Test	40	Output Enable Error
Disc Interface Test	42	Disc Local Error
Disc Interface Test	44	Disc External Control

			Error.
Disc Interface	Test	46	Disc External Data Error
GI Sound Test		so	GI Sound Chip Data Error

TABLE 3: SOLUTIONS

ERROR CODE	SOLUTION
02	Replace the Z8O. If problem still exists, conduct Z80 Controller Board Signature Analysis Procedures.
04	Replace the Z80. If problem still exists, first conduct Z80 Controller Board Signature Analysis Procedures, then run RAM Test.
10	Same as for 02.
11	Check U2 on ROM Board and U4 on Z80 Controller Board.
12	Check U3 on ROM Board and U4 on Z80 Controller Board.
13	Check U4 on ROM Board and U4 on Z80 Controller Board.
14	Check US on ROM Board and US on Z80 Controller Board.
20 and 22	Replace RAM. If problem still exists, run Stand-Alone RAM test.
30 and 32	Run Stand-Alone Interrupt Test.
40, 42, 44, 46	Run Stand-Alone Disc Interface Test.
50	Run Stand-Alone GI Sound Test, and, if necessary, the GI SCOPE Program.

If the program fails to run any tests at all, either the processor is incapable of running the diagnostics, or the display board itself is bad. Perform board substitution to isolate the problem.

TEST 60: DIPSWITCH TEST

Immediately following Test 50, the program runs Test 60. First set to OFF all of the bits on Dipswitches 1 and 2, causing a dash to appear on both Dipswith displays. The dashes indicate that no

bits are grounded.
NOTE: Grounded = Closed = low

Dipswitch 1 = B = DS4
Dipswitch 2 = A = DS5

Now ground one bit at a time, starting with those on Dipswitch 1. The bit number for each successively grounded bit should appear in its respective Dipswitch display:

For Dipswitch 1:		For Dipswitch 2:	
BIT	BIT NUMBER on DS4	BIT	BIT NUMBER on DS5
0	BO	0	AO
1	Bl	1	Al
2	B2	2	A2
3	B3	3	A3
4	B4	4	A4
5	B5	5	A5
6	B6	6	A6
7	B7	7	A7

If an 'E' appears on a display, more than one bit is grounded on the Dipswitch under test. There may be a short on that Dipswitch. If an "L" appears, all bits are grounded.

After testing ALL of the bits on both Dipswitches, use the above process to make sure that all of the test points on the test fixture are operating correctly. First turn all of these switches to OFF. Then ground each of them, one at a time to produce the following displays on DS6:

BIT	DISPLAY on DS6
0	
1	-----
2	Coin 1
3	Coin 2
4	Aux 4
5	Aux 5
6	Fan
7	-----

A display of "E" indicates that two bits are grounded at the same time. Test 60 is the last test of the LAIR 3 PROM. Press the RESET button if it is necessary to repeat the test cycle.

LAMP TEST

If the Lamp Test portion of the LAIR Test fails, or if the displays fail to operate correctly in any other tests, conduct this Lamp Test.

Begin by connecting a 16-pin ribbon cable from J3 of the Z80 Controller Board to Jl of the game's display board. Insert the LAMPCYC2 PROM into Ul of the PROM board, and power up the boards. It does not matter how/if Jl is hooked up.

This test is composed of two parts. The first is a Display Data Test, the second a Display Address Test.

Note that the LAMPCYC2 program does not automatically halt on errors. Error detection is the job of the technician. Any variance frem the expected output should be corrected.

DISPLAY DATA TEST

This test begins as soon as one of the control panel inputs is grounded. Each display progresses through the same sequence of characters at the same time: the numbers 0 through 9, a dash, the letters E, H, L, P, and a blank. All displays should register identical characters at any given time. Note that a blank is considered to be a character.

DISPLAY ADDRESS TEST

The numbers 0 through 9, a dash, the letters E, H, L, P, and a blank should appear, in this consecutive order, in displays DS1 through DS16. 0 appears in DS1, 1 in DS2, etc..

Maintaining this order, the entire sequence of characters should then rotate, with a pause between each rotation, until each character has appeared in every display.

If the tests fail to function at all, one of the following is true:

1. The Z80 is incapable of running any of the diagnostics.
2. The display board is malfunctioning.
3. The PROM board is defective.

Perform board substitution to isolate the problem.

If, however, the tests indicate a problem on the Z80 Controller Board, check the: data lines, address lines, control lines, address decoding, power, reset, and clock. After locating and solving all problems, repeat the LAIR Test.

RAM TEST

When the LAIR Test indicates a RAM failure, conduct the following RAM test. Begin by connecting a 16-pin ribbon cable from J3 of the Z80 Controller board to an operating game display panel. Insert the MEMB3 PROM into Ul of the PROM card, and attach the card to the Z80 Controller board. The test harness is not used in this test. Power up the board.

In this test, DS9-DS11 in Display 1 monitor the output data sent by the Z80 to the RAM. Assuming that the Z80 is functioning properly, this data should be "good" data. DS12-DS14 in Display 0 monitor the data being returned from the RAM to the Z80--the data transfer under test, the potentially 'bad' or malfunctioning data. DS7 and DS8 are not used in this test.

The RAM Test passes if, after power up, all twelve working displays change rapidly and continuously. The data displayed in Display 1 and Display 0 should be the same at all times. The RAM Test fails when all of the displays stop changing.

The MEMB3 PROM runs through the RAM test continuously, stopping only to indicate a failure. The 'pass count'--the number of times the test is completed successfully--is registered in Displays 3 and 2, DS1 through DS6.

Each RAM Test may be broken down into two parts: a test of the data lines from the RAM to the Z80, and a test of the address lines from the RAM to the Z80. The data lines are always tested first, the address lines second. Consequently, a successfully completed RAM test always registers an even number on the pass count. For example, as the MEMB3 program runs, the pass count counts "1" for the first data line test passed, "2" for the first address line test passed and for the first entire RAM test passed. "3" indicates a second successful data line test, and "4" a second successful address line test/second successful RAM test.

The source of a failure can thus be narrowed down by the pass count. If the pass count fails to begin, remaining at 00, the board has failed the data line half of the RAM test. If the pass count halts at 01, there is a faulty address line. Always allow the pass count to reach at least 3 to ensure that no problems are missed.

After correcting any problems, repeat the RAM Test by pressing the RESET button on the Z80 Controller board or by turning the power off, then on again. After repeating the RAM Test, repeat the LAIR Test to make sure all problems have been eliminated.

INTERRUPT TEST

When the Interrupt portion of the LAIR Test fails, conduct the following Interrupt Test. Begin by connecting the Z80 Controller board to the test harness. Plug the INT TEST 5 PROM into the Ul socket of a working PROM board. Connect the PROM board and a working display panel to the Z80 Controller Board. And connect Jl of the Z80 Controller Board to il of the test harness.

NOTE: In order to function properly, this test must have good RAM.

This test monitors the length of time between the interrupts generated by the 68705 at U7. The time between interrupts should be 33 milliseconds. The test may be conducted in either of the following modes:

1. HALT ON ERROR: Here, the test halts when it detects an error. DS8 displays a '5' if the time between interrupts is too short, a '1' if the time between interrupts is too long. To conduct the test in this mode, simply follow the directions above. An "H" in DS7 indicates that the HALT ON ERROR mode is in use.

2. LOOP ON ERROR: 'Here, the test program runs continuously, counting and classifying any errors as it progresses. DS8 displays a "5" if the time between interrupts is too short, a "1" if the time is too long. Displays DS9 through DS11 record the number of times the intervals between interrupts are too short. Displays DS12 through DS14 record the number of times the intervals are too long.

   To conduct the test in this mode, ground any one of the control panel inputs at the test fixture, and press the RESET button on the Z80 Controller Board. An 'L" in DS7 indicates that the LOOP ON ERROR mode is in use.

For both modes, the number of times the test passes the "pass count" is recorded in DS1 through DS6. Note that a verdict of too-long intervals may indicate that no interrupts are being generated at all.

DISC INTERFACE TEST

Begin by connecting Jl of the Z80 Controller Board to Jl of the test harness. Connect the 16-pin ribbon cable from J3 of the Z80 Controller board to Jl of the display panel. Insert the DISC INT 5 PROM into the Ul socket of the PROM board.

ON-BOARD LOGIC

Part I: Output Enable

The test program writes a series of zeros to output latch U21. This write and a high on U21-1 should disable the output enable of U21, causing a series of ones to be read back by video disc input latch U20.

If the test fails, an 'e' for 'error' appears in DS7, and a zero appears in DS8, indicating that an on-board problem is hindering or preventing the disablement of interface between the Z80 Controller Board and the video disc.

Part II: Logic

Here, the test program writes data to video disc output latch U21. This data is read back into video disc input latch U20. The input data should match.the output data. If the test passes, a 'P' appears in DS8, and a dash appears in DS7.

If the test fails, an 'L' appears in DS8 to indicate a local error, and an 'E' appears in DS7.

EXTERNAL CABLE CONNECTIONS

Now the test program writes to video disc output latch U21, to the INT/EXT control line, to the coin counter output of miscellaneous output register U16, and, in games with serial numbers 1-4999, to the ENTER output. From these locations, the data is then routed through the test fixture to Control Panel A's and Control Panel B's input registers U8 and U14. If the inputs at U8 and U14 match the original outputs, a 'P' appears in DS8.

If the inputs fail to match the outputs, an "E" appears in DS7 and in DS8. Ones signify high signals, zeros low, for the 'good' output signals in D51 through DS3. The same is true for the bad input signals in DS9 through DS11.

The problem causing the discrepancy between the output and input signals may be traced down to a single signal line. Output and input signals from DO through D7 are recorded in octal in displays DS4-DS6 and DS12-DS14. Base eight makes it possible for more than one signal line to be monitored in a single display. This is best understood through an example:

Note that DS4 monitors the signal outputs at D7 and D6. The output signals are both registered or recorded in one octal display number. Now suppose, for example, a 3 appears in DS4. 3 in base eight broken down into binary notation = 2 to the zero power + 2 to the first power = 1 + 2. 2 to the zero power, or 1, is the output signal at D7. And 2 to the first power, or 2, is the output signal at D6. For an illustration of this example, see the display chart for this test.

The same method is used to record the input signals to D7 and D6 in DS12. The outputs in DS4 should match the inputs in DS12. A problem may, by this method, be traced to the output or input of a single line. The rest of the signal lines/displays work the same way.

Once the malfunctioning line is identified, turn to the tables below. Here, the external connections for various output and input signals are listed. Use an oscilloscope probe at these connections to further narrow down the problem. The results for each signal should be the same at both connections.

NOTE: Output bit 6, ENTER, is not used in games with serial numbers 5000 and above.

OUTPUTS FROM MISCELLANEOUS CONTROL REGISTER

OUTPUT SIGNAL NAME	Z80 BIT POSITION	CONNECTOR
INT/EXT	7	Jl-17
ENTER	6	Jl-2
	5	--OUTPUT ENABLE FOR VIDEO DISC LATCH--
COIN COUNTER	4	J4-33
	3-0	NOT USED

INPUTS TO CONTROL PANEL B REGISTER

CONNECTOR	INPUT SIGNAL NAME	Z80 BIT POSITION
J4-6	P2	1
J4-2	Pi	0
Jl-6,7	READY	7

OUTPUTS FROM DISC CONTROL REGISTER U21

OUTPUT SIGNAL NAME	Z80 BIT POSITION	CONNECTOR	
D7	7	Jl-16	
D6	6	J1-15	
D5	5	Jl-14	---->
D4	4	Jl-13	
D3	3	J1-9	
D2	2	J1-10	
Dl	1	J1-11	
DO	0	J1-12	

INPUTS TO CONTROL PANEL A REGISTER

CONNECTOR	INPUT SIGNAL NAME	Z80 BIT POSITION
J4-17	AUX 3	7
J4-21	AUX 2	6
J4-25	AUX 1	5
J4-29	ACTION	4
J4-1	RIGHT	3
J4-5	LEFT	2
J4-9	DOWN	1
J4-13	UP	0

When all the tests pass, a 'P' appears in DS8, the pass count begins to increment in DS15 and DS16, and the program starts over. To reset the pass count; press the RESET button or turn the power off, then on again.

GI SOUND TEST

When the GI Sound portion of the LAIR Test fails, conduct the following test. Begin by connecting a 16-pin ribbon cable from J3 of the Z80 controller board to an operating display panel. Insert the GITF (GI Test Rev F) PROM into the Ul socket of an operating PROM board. It does not matter how/if the test harness is hooked up. Make sure, however, that the RAM on the Z80 board are functioning properly. Hook up the test harness to the speakers.

Power up the board. Display 1, DS9 through DS11, monitor the "good" data, the data sent from GI Sound Chip Ul9 to the Z80. Display 0, DS12 through,DS14, monitor the data tranfer under test, the data transfer from the Z80 back to Ul9. Displays 3 and 2 show the pass count.

At power up, all of the data displays, DS9 through DS14, should be changing rapidly. All data displays, however, should show the same characters at any given time. If the displays halt, the test fails, indicating a problem with the Z80's reads from and writes to the GI Sound Chip.

As the displays change, three musical tones should be heard. Each of these tones come from a different GI Sound output. If any of the tones are missing, either the GI Sound Chip's sound outputs or the audio amplifier circuits are malfunctioning.

To repeat this test, press the RESET button on the Z80 Controller board or turn the power off, then on again. After correcting any problems, rerun the LAIR Test.

GI SCOPE TEST PROGRAM

Problems with the GI sound may be traced to the signal level with the aid of this test program and an oscilloscope. Carefully follow the guidelines for troubleshooting outlined below.

This troubleshooting procedure is dependent upon several assumptions:

l.) The LAIR Test runs all tests up to, but not including, Test 50: GI Sound Test.

2.) The GI Sound Test has failed, leaving the specific problem undiscovered and unsolved.

3.) The original GI Sound Chip has been replaced by a GI Sound Chip that is known to be in correct working order. The replacement failed to rectify the problem.

If all of these assumptions are true for the board presently under test, install the GI SCOPE PROM in the Ul socket of a known-working PROM board. Connect J4 to the main wiring harness. Then attach a 16-pin ribbon cable from J3 of the Z80 Controller Board under test to Jl of a properly functioning Display Board. And, use a 40-pin ribbon cable to connect J2 of the PROM board to J2 of the Z80 Controller Board. Jl of the Z80 Controller Board does not need to be connected.

Now power up the boards, and conduct the following preliminary tests:

l.) Check for grounds at Ul9, pins 1 and 24.

2.) Check for +SV at Ul9, pins 40, 28, and 25.

3.) Check for clock signal at Ul9-22. The signal should be a square wave and have a period of 50Ons.

4.) Check for a reset pulse at Ulg-23. This line is normally high, but should drop low when the reset button is depressed.

Do not continue until the above four conditions are met. When all is satisfactory, make sure that the Display Board reads as follows:

Display 0: 125
Display 2: 252

If the displays are incorrect, or if there are no displays at all, find the problem and correct it before continuing. Either the PROM is defective, the display itself is defective, or the Z80 Controller Board is malfunctioning.

INTRODUCTION TO THE TEST PROGRAM:

The program first sends a low-going sync pulse to U16-2. This pulse serves as an external trigger to the oscilloscope. The program then writes an address of 04 octal to the GI Sound Chip.

Next, the program sends a data byte of 125 octal to the GI Sound Chip. This test data is displayed in Display 0. The program also reads data from the GI Sound Chip. This data is displayed in Display 1. If all is functioning correctly, Display 1 should read 125.

Now the progrant writes first an address of 13 octal, then a data word of 252 octal, to the GI Sound Chip. The latter is displayed in Display 2.

Lastly, the program reads data from the GI Sound Chip and displays it in Display 3. If all is functioning correctly, Display 3 should read 252.

TROUBLESHOOTING PROCEDURE

STEP I:

Use an oscilloscope to compare the pulses occurring at U10, pins 13 and 15, and Ull-15 to the corresponding pulses pictured in the GI Control Signal Timing Chart. If any pulses are missing, there is a problem in the address decoding section of the Z80 Board. In this case, check the inputs to U10 and Ull and both the inputs and outputs of U4.

If all of the pulses occurring at U10, pins 13 and 15, and Ull-15 are shorter than those pictured in the timing chart, the Wait circuit is defective. In this case, connect the external trigger of the oscilloscope to U16-2. Sync the scope to the rising edge of the pulse. Then place Channel 1 of the scope on U10-13. Use Channel 2 to compare the wave forms produced with those in the timing chart. Correct any problems before continuing.

STEP II:

If STEP I fails to locate the problem, proceed as follows. Connect the external trigger of the scope to U16-2, and sync the scope on the rising edge of the pulse. Connect Channel 1 to U10-13. Use Channel 2 to compare the following signals to the corresponding signals illustrated in the signal timing chart:

U10-13
U10-15
Ull-15
U19-27
U19-29

If there are any problems, check U22.

STEP III:

Set up and synchronize the scope as it is in STEP II. Then connect Channel 1 to U10-15, so that two pulses are observed. Use Channel 2 to check pins 30-37 on Ul9, the data lines to the GI Sound Chip. Compare the signals on the scope to those illustrated in the timing chart. It is essential that these lines are in their correct states when U10-15 is low. (When U10-15 is high, the behavior of these lines is irrelevant).

If the lines are in their correct states, the GI Sound Chip is properly connected to the Data Bus.

STEP IV:

Set up and synchronize the scope as it is in STEPS II and III. Then connect Channel 1 to Read Data Pulse Ull-15. Use Channel 2 to compare the signals at U19, pins 30-37 to those illustrated in the timing chart. It is essential that these lines are in their correct states when Ull-15 makes a low-to-high transition. The behavior of these lines is irrelevant at all other times.

If the correct data still fails to appear, an unwanted device is competing with the GI Sound Chip to drive the bus. In this case, use Channel 2 to insure that pins 7 and 9-14 on Ull do not go low simultaneously with Ull-15. If this happens, either Ull is defective, or there is a short on the board. Similarly, pins 7 and 10-15 on U4 should not go low simultaneously with Ull-15. If this happens, either U4 is defective, or there is a short on the board.

SWITCH TEST

If either the Disc Interface portion or the Switch Test portion of the LAIR Test fails, troubleshoot the option and control inputs in the following manner.

First make sure that the Z80, the PROM board, and the Display Panel are functioning properly. The states of the RAM, interrupts, audio amplifiers, and the GI sound have no effect, either positive or negative, on the outcome of this test. Now connect Jl of the Z80 Controller Board to Jl of the test harness.

There are four sets of Switch inputs:

Dip Switch 1
Dip Switch 2.
Control Panel Byte A
Control Panel Byte B

The test program reads these inputs, then echoes them to the Display Panel.

Take the Dip Switches first. Cycle each Dip Switch individually. The inputs for Dip Switch 1 are echoed in octal notation in Display 3, DS1-DS3, the inputs for Dip Switch 2 in Display 2, DS4-DS6. When all bits on a single Dip Switch are open/high, the display for that Dip Switch should read 377 octal. The following table lists the display numbers for a Dipswitch with one pin closed/grounded:

BIT HELD LOW	OCTAL DISPLAY NUMBER
7	177
6	277
5	337
4	357
3	367
2	373
1	375
0	376

Now take the control panel inputs. The input bits at Control Panel Byte A are linked to the outputs at Miscellaneous Output Register U16. The inputs bits at Control Panel Byte B are linked to the inputs at Disc Output Register U21. The connection points for these inputs and outputs are listed be below. Toggle the input bits one at a time by grounding them at the test harness. At the same time, watch the corresponding outputs with a scope. High inputs should be linked to high outputs, low inputs to low outputs. The inputs for Control Panel Byte B are monitored in octal in Display 1, DS9~DS11, the inputs for Control Panel Byte A in Display 0, DS12-DS14.

NOTE: Coin Counter Driver Transistor Q3 acts as an inverter. The signal appearing at U16-2 is therefore the inverse of the Coin Counter Drive signal appearing at J4-33.

CONTROL PANEL INPUT BYTE A

BIT	NAME	J4, PIN	U8, PIN	
D0	Up	13	11	
Dl	Down	9	13	
D2	Left	5	15	---- >
D3	Right	1	17	
D4	Action	29	8	
D5	Aux 1	25	6	---- >
D6	Aux 2	21	4	
D7	Aux 3	17	2	

MISCELLANEOUS OUTPUT

BIT	NAME	J no. PIN	U16, PIN
D0	BO	Not used	----
Dl	Bl	Not used	-------
D2	B2	Not used	--------
D3	B3	Not used	-------
D4	Coin Counter Drive	4 33	2
D5	Disc O.E.		5
D6	Enter	1 2	6
D7	Int/Ext	1 17	9

NOTE: ENABLE DISC OUTPUT BY GROUNDING D5 OF CONTROL PANEL A.

CONTROL PANEL INPUT BYTE B					DISC OUTPUT		
BIT	NAME	J no.	PIN	U14, PIN	BIT	Jl, PIN	U21, PIN
DO	P1	4	2	17	DO	12	2
Dl	P2	4	6	15	Dl	11	19
D2	Coin 1	4	10	13 ---->	D2	10	5
D3	Coin 2	4	14	11	D3	9	16
D4	Aux 4	4	26	2	D4	13	6
D5	Aux 5	4	22	4 ---->	D5	14	15
D6	Fan	4	18	6	D6	15	9
D7	Ready	1	6,7	8	D7	16	12

SIGNATURE ANALYSIS: DATA AND ADDRESS LINES

FOR THE Z80 CONTROLLER BOARD

Use the following procedure to debug boards that do not run test programs properly even after the original Z80 Microprocessor has been replaced by a Z80 that is known to be in correct working order.

STEP I: PRELIMINARY TESTS:

Positive results to each of the following tests are essential to the production of valid signatures in the Signature Analysis Tests of the Data and Address lines. Solve each problem as it arises. Do not move on until each test has been completed satisfactorily.

To begin, connect J4 of the Z80 Controller Board to the main DC wiring harness. Use a 40-pin ribbon cable to connect J2 of the Z80 Board to a PROM board that has been loaded with a game program.

A. DC VOLTAGE SUPPLY: Check the +5V DC supply at Ul-11. There should always be between 4.8 and 5.2 volts.

B. CONTROL LINES: Remove the Z80, and install a modified NO-OP jumper in the Z80 socket at Ul. Now use an oscilloscope to check all of.the following Z80 Control lines:

l.) CLOCK: Ul-6. The CLOCK should have a period of 25Ons. The high level should be 4.4V or above, the low level 0.45V or below.

2.) RESET-: Ul-26. Normally high, this line should drop low when the RESET button is depressed.

3.) BUSRQ-: Ul-25. This line should be high.

4.) WAIT-: Ul-24. This line may be either high or toggling. If it is tied low, the Wait Circuit is defective. Check U28 and associated circuitry.

5.) INT-: Ul-16. This line should be low. If it is not low, check the signals arriving at U26, pins 11 and 13. U26-11 should be a square wave wave with a period of 33 milli-seconds, and U26-13 should be high.

6.) NMI-: Ul-17. This line should be high.

C. ADDRESS DECODING: Connect Channel 1 of the scope to U4-15. Sync the scope until the wave obtained is the same as that shown in Figure 1. Now use Channel 2 to compare the wave forms obtained at U4, pins 7 and 9-14 to the corresponding waves pictured in Figure 1. Note that the pulse bursts at U4, pins 7 and 9 are slightly longer than those at U4, pins 10-14. This difference is due to the action of the Wait Circuit.

If all of the correct wave forms appear, the address decoding system and address lines 13-15 are functioning properly. If some of the waves do not match their counterparts in Figure 1, check U4. If only some of U4's outputs are functioning correctly, the problem can be traced to address lines 13-15. If none of U4's outputs are working, make sure pins 8-10 on U4 are toggling.

D. Ul-19.(MEMORY REQUEST) and Ul-27: Make sure both lines are toggling.

DO NOT proceed until all of the above tests have been completed.

STEP II: SIGNATURE ANALYSIS

Set up the Signature Analyzer in the following manner:

START lead to U4-15: falling edge
STOP lead to U4-10: falling edge
CLOCK lead to CLOCK TEST POINT on NO-OP rising edge
GROUND lead to U4-8

Now power up the CPU Board, and probe for the following Data Line signatures:

TABLE 1

Location: Ul of Z80 Controller Board at base of No-OP jumper.

PIN	NAME	SIGNATURE
14	DO	4A61
15	Dl	9C50
12	D2	C6P5
8	D3	U113
7	D4	0043
9	D5	2837
10	D6	CHSO
13	D7	H4P8

If all of the signatures are correct, the Z80 can successfully read PROM memory. The game boards, therefore, should be able to run the LAMP CYC 2 and SW TST 1 test programs.

If all of the signatures are correct, but the boards are still incapable of running the above two test programs, there may be a problem in the I/0 Address Decoding. In this case, refer to SIGNATURE ANALYSIS: I/0 ADDRESS DECODING.

If any or all of the signatures are incorrect., compare the signatures for DO-D7 on Ul of the PROM card to those listed in TABLE 2 below. If all of these signatures match, then:

a. There is an open data line.
b. U15 is defective.
c. U15-1 is lacking an active-low READ signal.

If any or all of the signatures are incorrect, then:

a. There are shorted address lines.
b. The address lines are defective.
c. Pins 11-15, the outputs of U4, are not properly connected to pin 20 on Ul through U5 of the PROM card.

To locate the problem, compare the signatures for AO-A12 on Ul of the PROM card to the corresponding signatures in TABLE 2. If all of the signatures are correct, the address lines are functioning properly.

If all of the address lines are functioning correctly, test for continuity between pins 11-15 on U4 and pin 20 on Ul through U5 of PROM card.

If any or all signatures are incorrect, check U2, U5, U9, and U12, and check for opens and shorts.

TABLE 2

Location: Ul of the PROM card:

SIGNAL,	SIGNATURE	PIN	PIN	SIGNATURE	SIGNAL
+5V	C7U8	1	28	C7U8	+SV
A12	UUU7	2	27	C7U8	+5V
A7	057F	3	26	N.C.	N.C.
A6	1506	4	25	663P	A8
A5	9A4U	5	24	4A0F	A9
A4	1F37	6	23	OPUO	All
A3	2C9P	7	22	----	O.E.
A2	925A	8	21	FC3F	A10
Al	FC32	9	20	----	C.E.
AO	6H57	10	19	H4P8	D7
DO	4A61	11	18	CH50	D6
D1	SC50	12	17	2837	D5
D2	C6PS	13	16	0043	D4
GND	0000	14	15	U113	D3

After checking all of the above signatures, make sure that the WAIT- line is toggling. If it is not, the Wait Circuit is defective.

SIGNATURE ANALYSIS: I/0 ADDRESS DECODING

Use this procedure when the Z80 Controller Board passes the Signature Analysis Tests of the Address and Data Lines, but still fails to run the LAYP CYC 2 and SW TST 1 Diagnostic Programs.

Begin by connecting J4 of the Z80 Controller Board to the-main DC harness. Insert Test PROM I-/0 SIG into Ul of a properly functioning PROM card. Use a 40-pin ribbon cable to connect the PROM card to J2 of the Z80 Controller Board.

Now set up the Signature Analyzer:

START lead to U4-14: falling edge
STOP lead to U4-12: falling edge
CLOCK lead to U23-17: rising edge
GROUND lead to U4-8

Probe pins 7 and 9-15 on U10 of the Z80 Controller Board for the following signatures:

PIN	SIGNATURE
15	829U
14	7391
13	7506
12	5549
11	5UPO
10	6836
9	8U10
7	8652

If any or all of the signatures are incorrect, check U10, U23, and WRITE line U10-5. if all of the signatures are correct, U10 is functioning correctly.

Now probe for the following signatures at pins 7 and 9-15 on Ull of the Z80 Controller Board:

PIN	SIGNATURE
l5	C67H
14	3FH8
13	U415
12	C8HP
11	UCP6
10	4A23
9	0H42
7	AU06

If all of the signatures are correct, Ull is functioning properly. If any or all of the signatures are incorrect, Ull is defective.

For the final test, probe for the following signatures at Ul9, pins 27 and 29:

PIN	SIGNATURE
27	U799
29	F37C

If both of the signatures are correct, U22 is functioning properly. If either signature is bad, U22 is defective.

CHAPTER 4
MONITOR AND NTSC DECODER BOARD SUPPLEMENT INFORMATION

NTSC DECODER BOARD ALIGNMENT PROCEDURE

PRELIMINARY

Set all six PCB controls to mechanical center except the sub-contrast (R107) which is set to the full clockwise position.

SET UP:

1. Connect a composite video color bar signal at 1.OV pp to the PCB input at P101.

2. Adjust sub-contrast (R107) for maximum contrast with no overdrive. Overdrive appears as vertical white bars between the color bars, most noticeable between the yellow and cyan bars.

3. Adjust sub-brilliance (R130) until the black portion of the color bar pattern just turns black (raster just extinguished).

4. Critically adjust trimmer capacitor C124 to center of color lock-in range. It is a good idea to power PCB monitor off for a few seconds, then back on to ensure color lock.

5. Set chroma input level (R144) fully clockwise, then rotate slowly counterclockwise until color appears, then rotate counterclockwise another 30-40 degrees.

6. Connect scope at 10 microsec/div (AC couple) to blue output (P103-6). Adjust L101 (3.58 MHz trap) for, minimum of 3.58 MHz carrier riding on video signal.

7. With scope at blue output. adjust sub-brilliance (R130) and contrast pre-set (R106) for a black level of 0.5 volts and a peak white level of 4.0 volts respectively.

8. With scope at blue output. adjust sub-color (R139) so that the peak level for the grey bar and the peak level for the blue bar are equal.

9. Connect the scope to the green output (P103-5) and adjust the sub-tint so that the peak level for the cyan bar and the peak level for the green bar are equal.

10. If necessary, re-adjust the contrast pre-set (R106) for a peak white level of 4.0 volts (3.5V above black level).

NOTE: All of the information in this chapter is taken directly from ELECTROHOME ELECTRONICS' Service and Operation Manual: G07-19' R.G.B. Colour Monitor, January 1981, and from ELECTROHOME ELECTRONICS' Supplement Service Data: NTSC Decoder, July 1983.