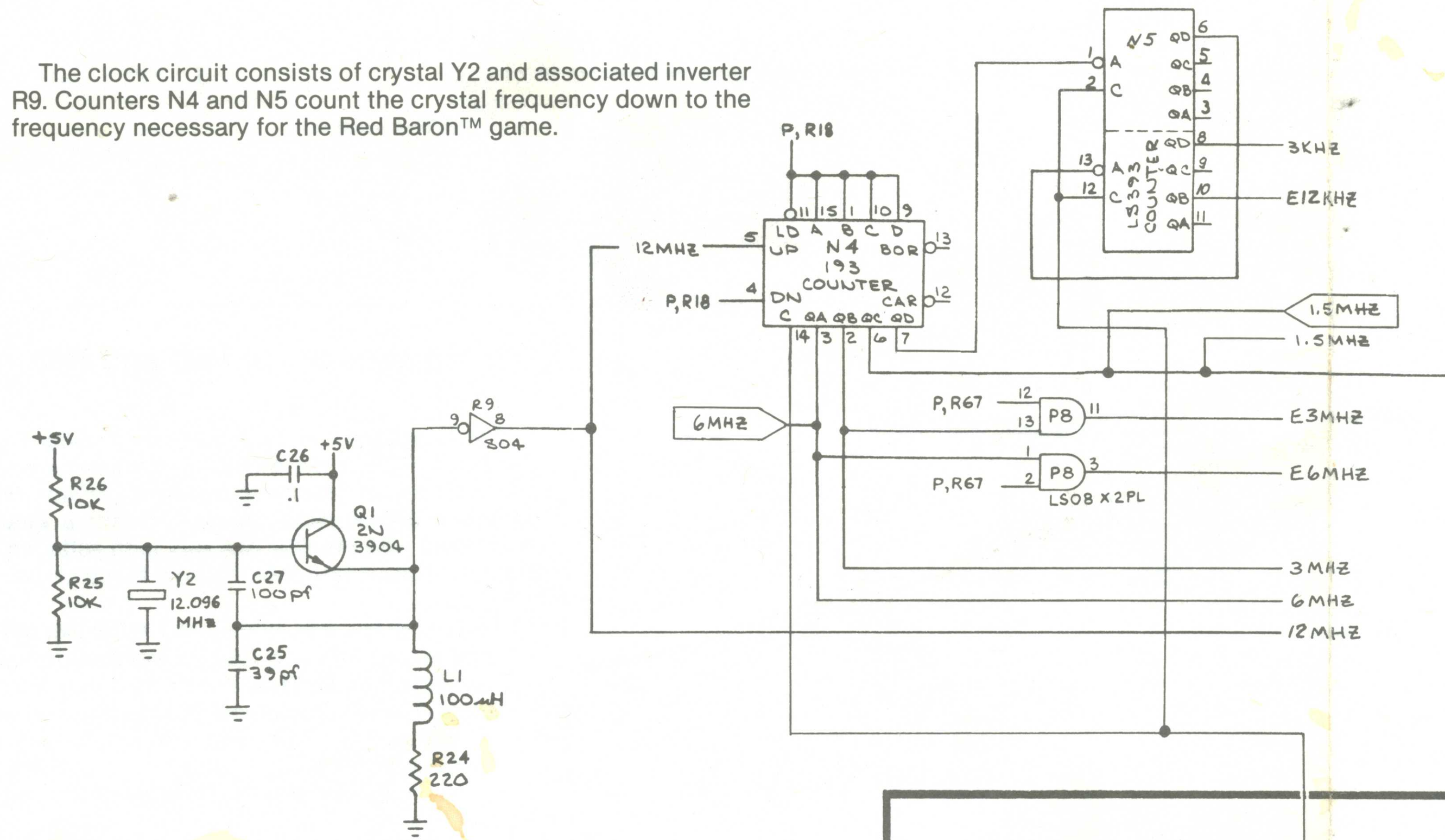
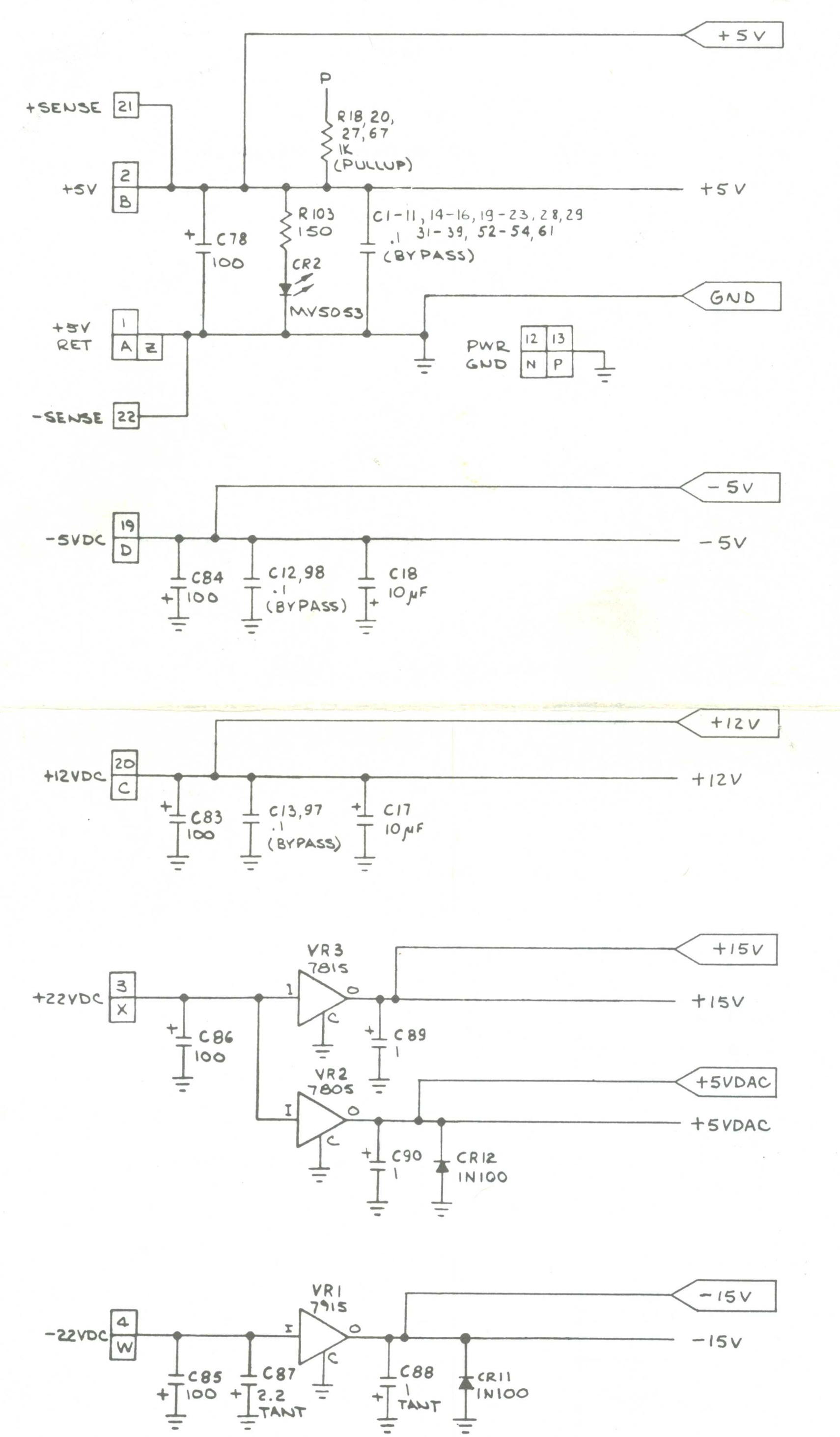
Clock Circiut

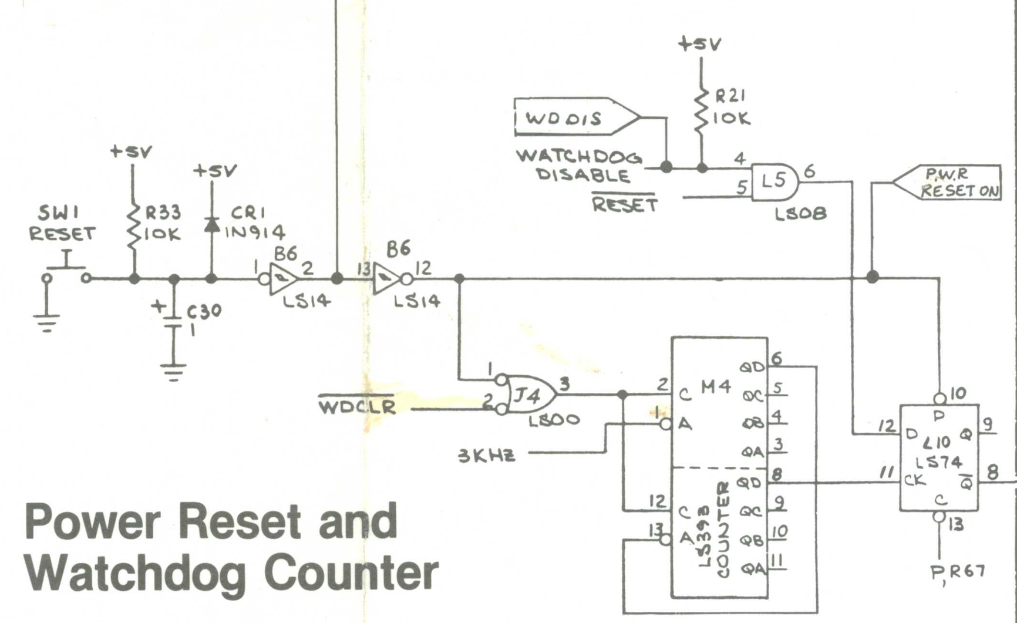
The clock circuit consists of crystal Y2 and associated inverter R9. Counters N4 and N5 count the crystal frequency down to the frequency necessary for the Red Baron™ game.



Power Input



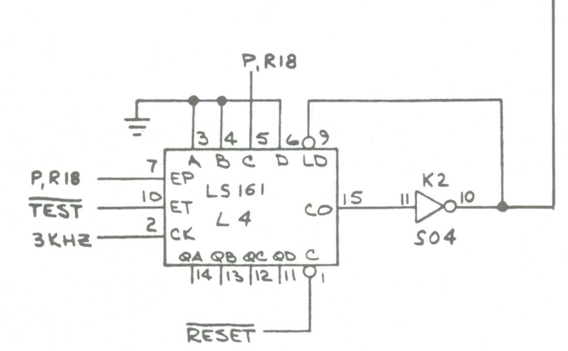
Power Reset and Watchdog Counter



During inital power-up, the delayed charging of capacitor C30 presets flip-flop L10 and clears counter M4. This results in holding RESET input to the MPU low. When the charge of C30 reaches about 1.5 VDC, preset and clear inputs are removed. Counter M4 counts to 128 at 3-KHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter M4 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter M4 will count up to the RESET state and cause the MPU to return to its initialization routine.

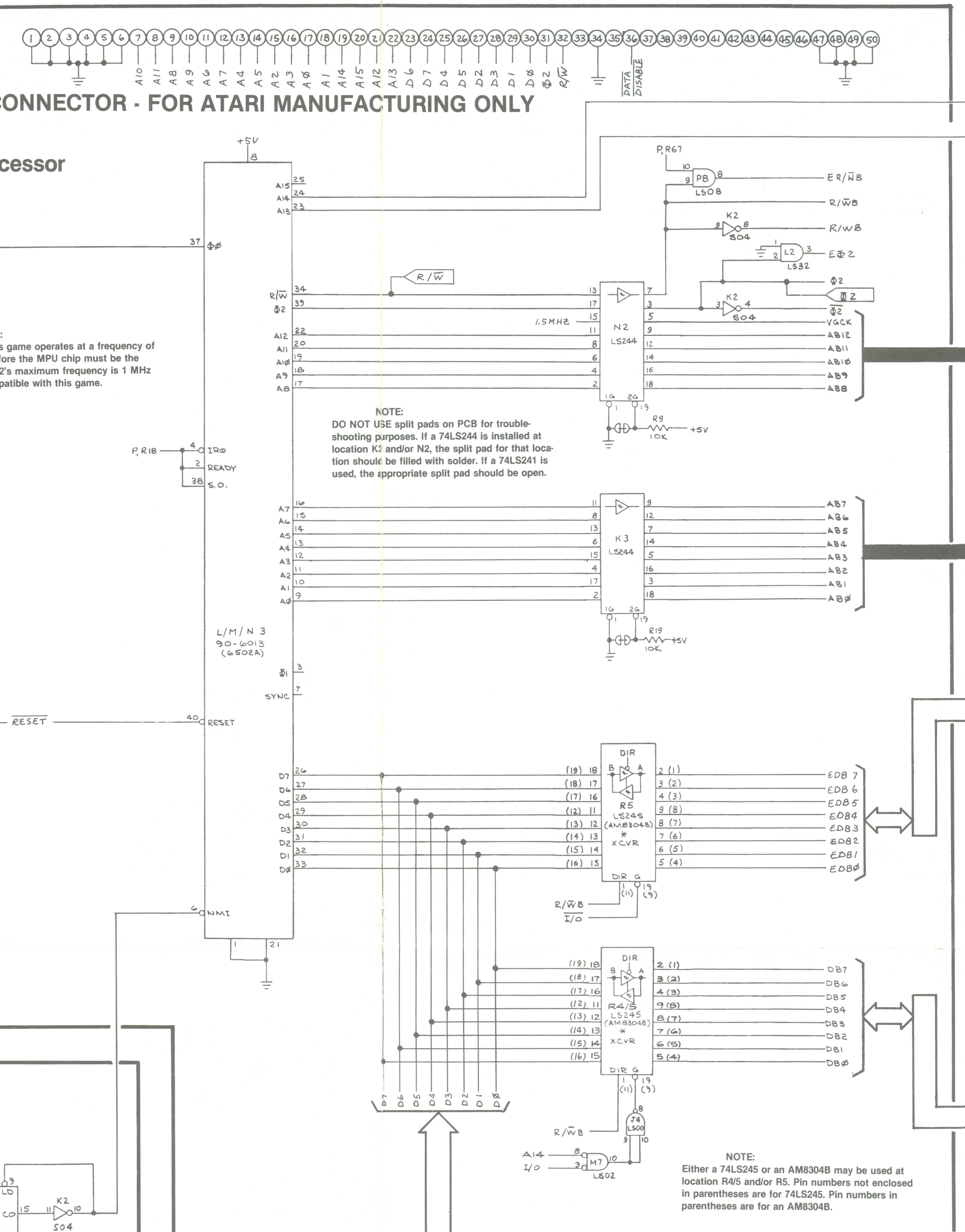
NMI Counter



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter L4. The interrupt occurs when pin 10 of inverter K2 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

TEST CONNECTOR · FOR ATARI MANUFACTURING ONLY

Microprocessor

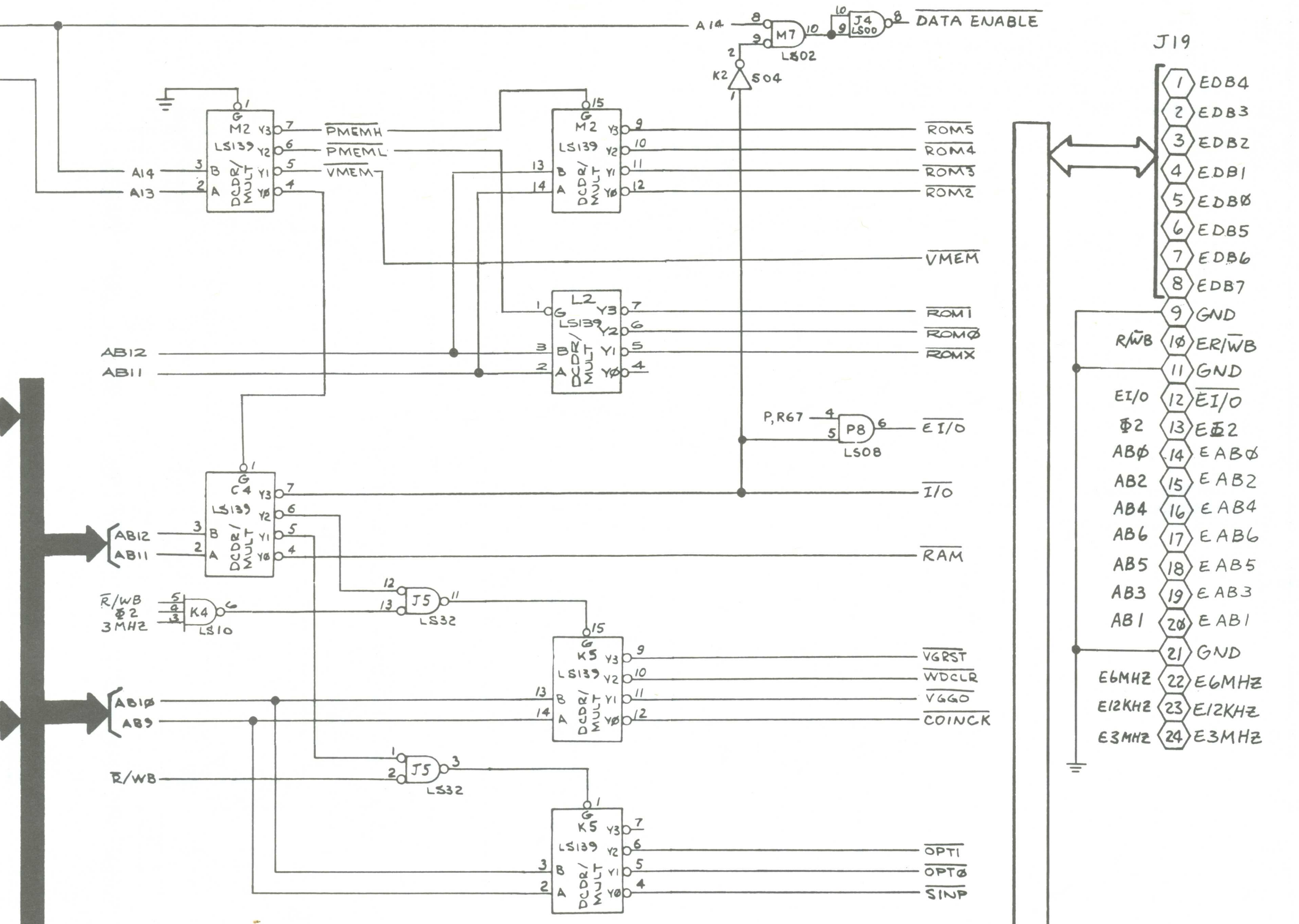


NOTE:
The MPU in this game operates at a frequency of 1.5 MHz. Therefore the MPU chip must be the 6502A. The 6502's maximum frequency is 1 MHz and is not compatible with this game.

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes. If a 74LS244 is installed at location K3 and/or N2, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.

NOTE:
Either a 74LS245 or an AM8304B may be used at location R4/5 and/or R5. Pin numbers not enclosed in parentheses are for 74LS245. Pin numbers in parentheses are for an AM8304B.

Address Decoder

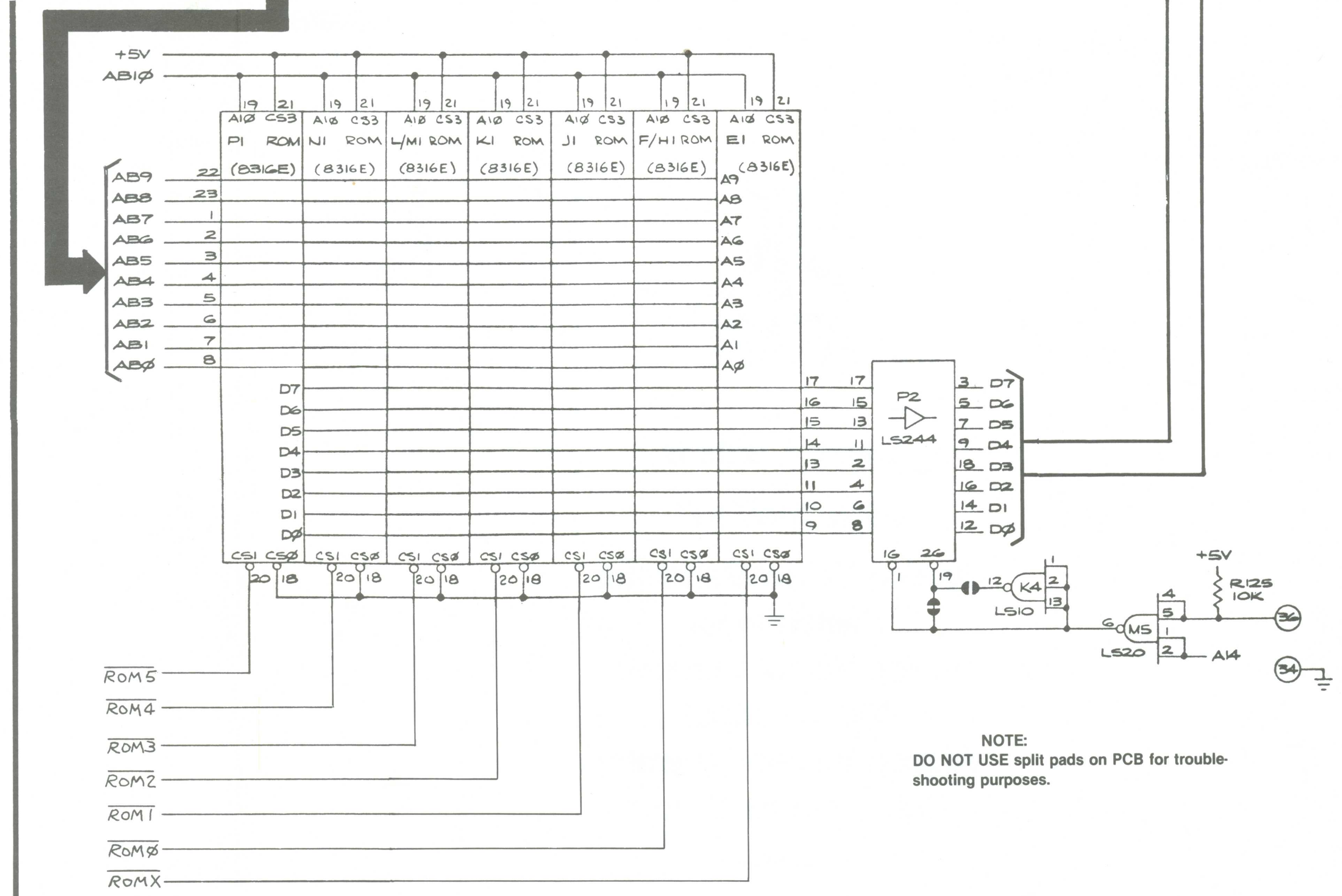


The function of the address decoder is to enable the appropriate circuitry at a particular time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Red Baron™ game.

If you are going to use the Automatic RAM/ROM Tester, remember to remove the MPU L/M/N3 and ground the WDOG DISABLE test point.

RAM Memory

ROM Memory



NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes.

NOTE
- ☐ Indicates Edge Connector
- ⬡ Indicates Interconnect Connector
- Indicates Test Point

MEMORY MAP

HEXA-DECIMAL ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		D	D	D	D	D	D	D	D	Program RAM (1K)
0800	R								D	Right Coin Switch
	R							D		Center Coin Switch
	R						D			Left Coin Switch
	R					D				Slam Switch
	R				D					Self-Test Switch
	R			D						Diag. Step Switch
	R		D							HALT
	R	D								3 KHz
0A00	R	D	D	D	D	D	D	D	D	Option Switch Inputs
0C00	R	D	D	D	D	D	D	D	D	Option Switch Inputs
1000	W								D	Right Coin Counter
	W							D		Center Coin Counter
	W						D			Left Coin Counter
1200	W									Vector Generator Go
1400	W									Watchdog Clear
1600	W									Vector Generator Reset
1800-187F		D	D	D	D	D	D	D	D	Auxiliary PCB Enable
2000-27FF		D	D	D	D	D	D	D	D	Vector RAM (2K)
2800-2FFF		D	D	D	D	D	D	D	D	Vector RAM/Vector ROM (2K)
3000-3FFF	R	D	D	D	D	D	D	D	D	Vector ROM (4K)
4800-7FFF	R	D	D	D	D	D	D	D	D	Program ROM (14K)

ATARI®

Sheet 2, Side A

RED BARON™

Game Microprocessor
Game Address Decoding Circuitry
Analog Vector-Generator PCB Power Input
Clock
NMI Counter
Power Reset and Watchdog Counter
Game Program Memory
Game RAM
Memory Map

Section of 035742-01 & -02 C

A Warner Communications Company