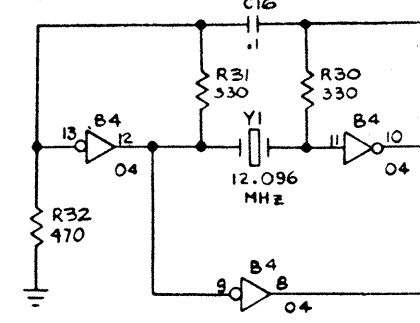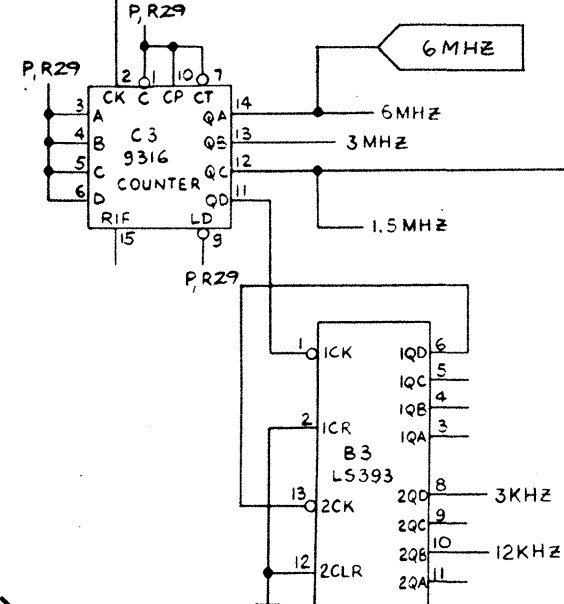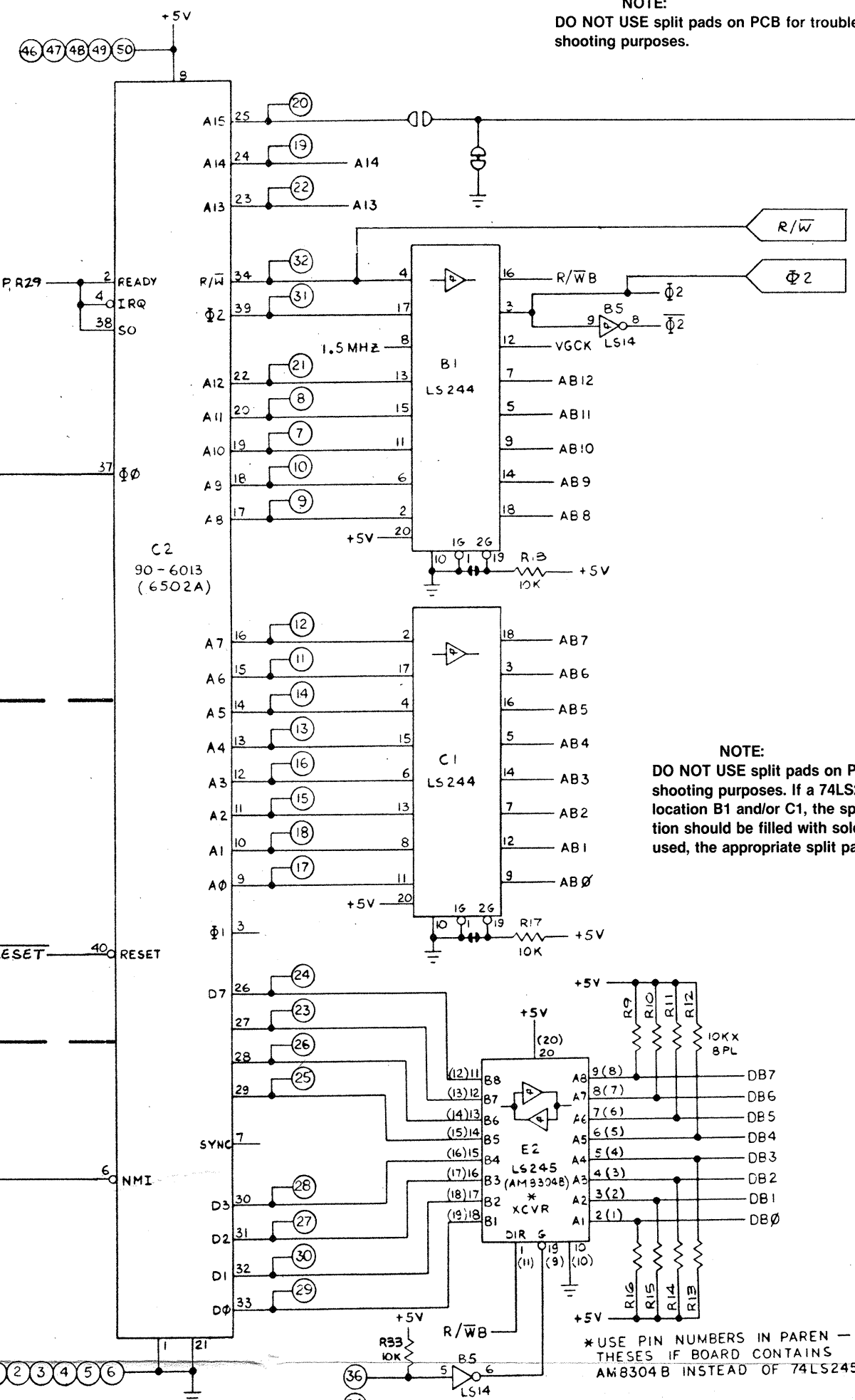## CLOCK CIRCUIT

The clock circuit consists of crystal Y1 and associated inverters and counters C3 and B3. Counters C3 and B3 count the crystal frequency down to the frequencies necessary for the Asteroids Deluxe™ game.

NOTE:
The MPU in this game operates at a frequency of 1.5 MHz. Therefore the MPU chip must be the 6502A. The 6502's maximum frequency is 1 MHz and is not compatible with this game.
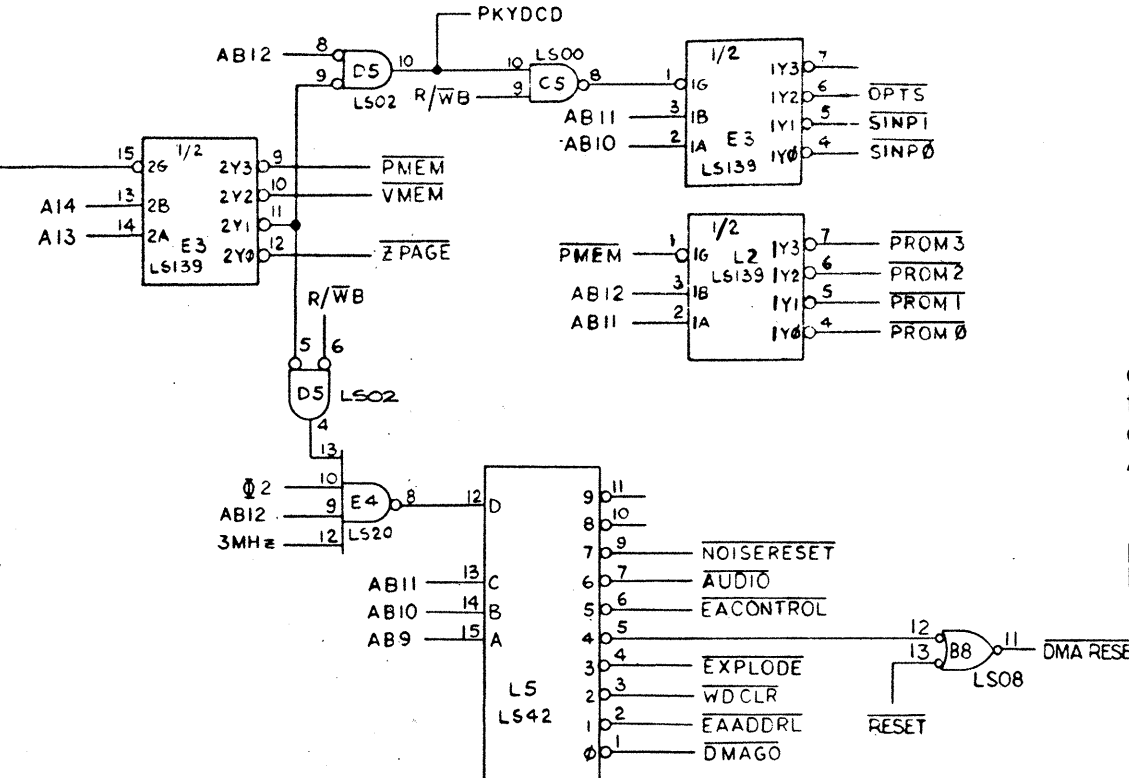
MPU CIRCUITRY

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes.

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes. If a 74LS244 is installed at location B1 and/or C1, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.

NOTE:
Either a 74LS245 or an AM8304B may be used at location E2. Pin numbers not enclosed in parentheses are for 74LS245. Pin numbers in parentheses are for an AM8304B.

* USE PIN NUMBERS IN PARENTHESES IF BOARD CONTAINS AM8304B INSTEAD OF 74LS245.
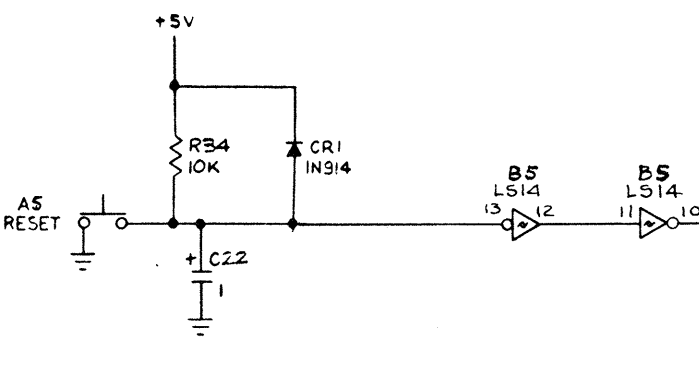
ADDRESS DECODING CIRCUITRY

The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids Deluxe™ game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

POWER RESET AND WATCHDOG COUNTER

During initial power-up, the delayed charging of capacitor C22 causes a preset of flip-flop D3 and a clear of counter D4. This results in holding RESET input to the MPU low. When the charge of C22 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D4 counts to 128 at 3-KHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.
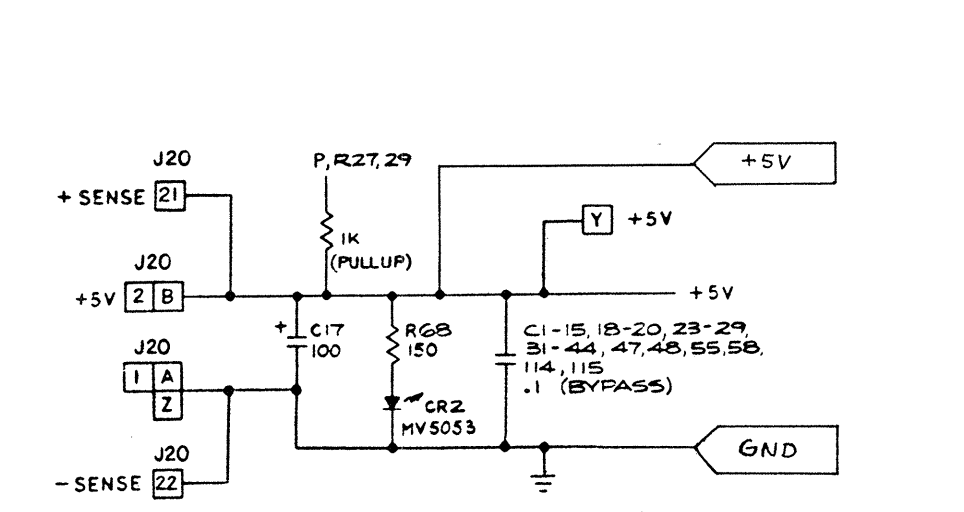
If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D4 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D4 will count up to the RESET state and cause the MPU to return to its initialization routine.

NMI COUNTER

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C4. The interrupt occurs when pin 6 of inverter B4 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

Denotes a test point

MEMORY MAP

HEXADECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0-3FF	0	0	0	0	0																					Scratch RAM
2000	0	1	0	0	0										0	0	R	D								Not used
2001	0	1	0	0	0										0	1	R	D								3 KHz
2002	0	1	0	0	0										1	0	R	D								Vg halted
2003	0	1	0	0	0										1	1	R	D								Shield switch
2004	0	1	0	0	0									1	0	0	R	D								Fire switch
2006	0	1	0	0	0									1	1	0	R	D								Slam switch
2007	0	1	0	0	0									1	1	1	R	D								Self-test switch
2400	0	1	0	0	1									0	0	0	R	D								Left coin switch
2401	0	1	0	0	1									0	0	1	R	D								Center coin switch
2402	0	1	0	0	1									0	1	0	R	D								Right coin switch
2403	0	1	0	0	1									0	1	1	R	D								1-player start switch
2404	0	1	0	0	1									1	0	0	R	D								2-player start switch
2405	0	1	0	0	1									1	0	1	R	D								Thrust switch
2406	0	1	0	0	1									1	1	0	R	D								Rotate right switch
2407	0	1	0	0	1									1	1	1	R	D								Rotate left switch
2800	0	1	0	1	0									0	0	0	R	D	D							Option switch 8, 7 (at R5)
2801	0	1	0	1	0									0	0	1	R	D	D							Option switch 6, 5
2802	0	1	0	1	0									0	1	0	R	D	D							Option switch 4, 3
2803	0	1	0	1	0									0	1	1	R	D	D							Option switch 2, 1
2000	0	1	0	1	1					A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	POKEY
2C40	0	1	0	1	1					A	A	A	A	A	A	A	R									EAROM read
3000	0	1	1	0	0												W									Start VG
3200	0	1	1	0	0					A	A	A	A	A	A	A	W	D	D	D	D	D	D	D	D	Latch EA address/data
3400	0	1	1	0	1												W									Watchdog reset
3600	0	1	1	0	1												W	D	D							Explosion pitch
3C00	0	1	1	1	1												W	D	D	D						Explosion volume
3A00	0	1	1	1	0												W					D				3800 VG reset
3C00	0	1	1	1	1												W									EA control latch
3C01	0	1	1	1	1										0	1	W								D	1-player start LED
3C02	0	1	1	1	1										1	0	W								D	2-player start LED
3C03	0	1	1	1	1										1	1	W							D		Ship thrust sound
3C04	0	1	1	1	1									1	0	0	W							D		Bank select
3C05	0	1	1	1	1									1	0	1	W							D		Left coin counter
3C06	0	1	1	1	1									1	1	0	W							D		Center coin counter
3C07	0	1	1	1	1									1	1	1	W							D		Right coin counter
3E00	0	1	1	1	1												W									Noise generator reset
4000	1	0	0	0	0												R									Vector RAM
4400	1	0	0	0	1												R									Vector RAM
4800	1	0	0	1	0												R									Vector ROM
4C00	1	0	0	1	1												R									Vector ROM
5000	1	0	1														R									Program ROM
6000	1	1	0														R									Program ROM
6800	1	1	0														R									Program ROM
7000	1	1	1														R									Program ROM
7800	1	1	1														R									Program ROM

(Row group labels: INPUTS, OUTPUTS, RAM, ROM)
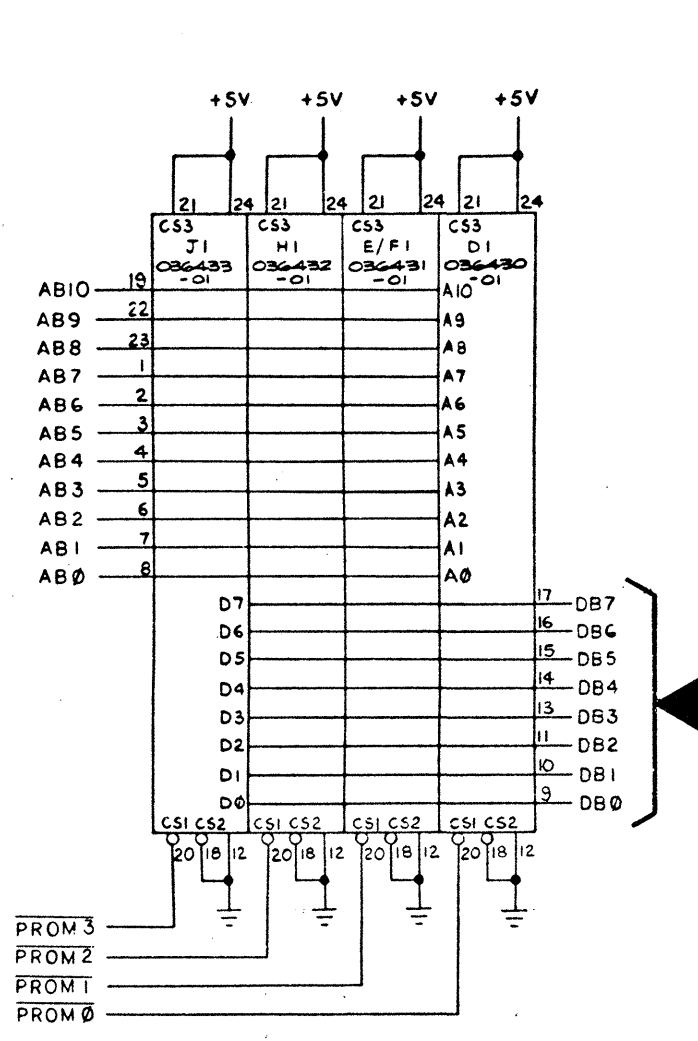
POWER INPUT

This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 25 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.
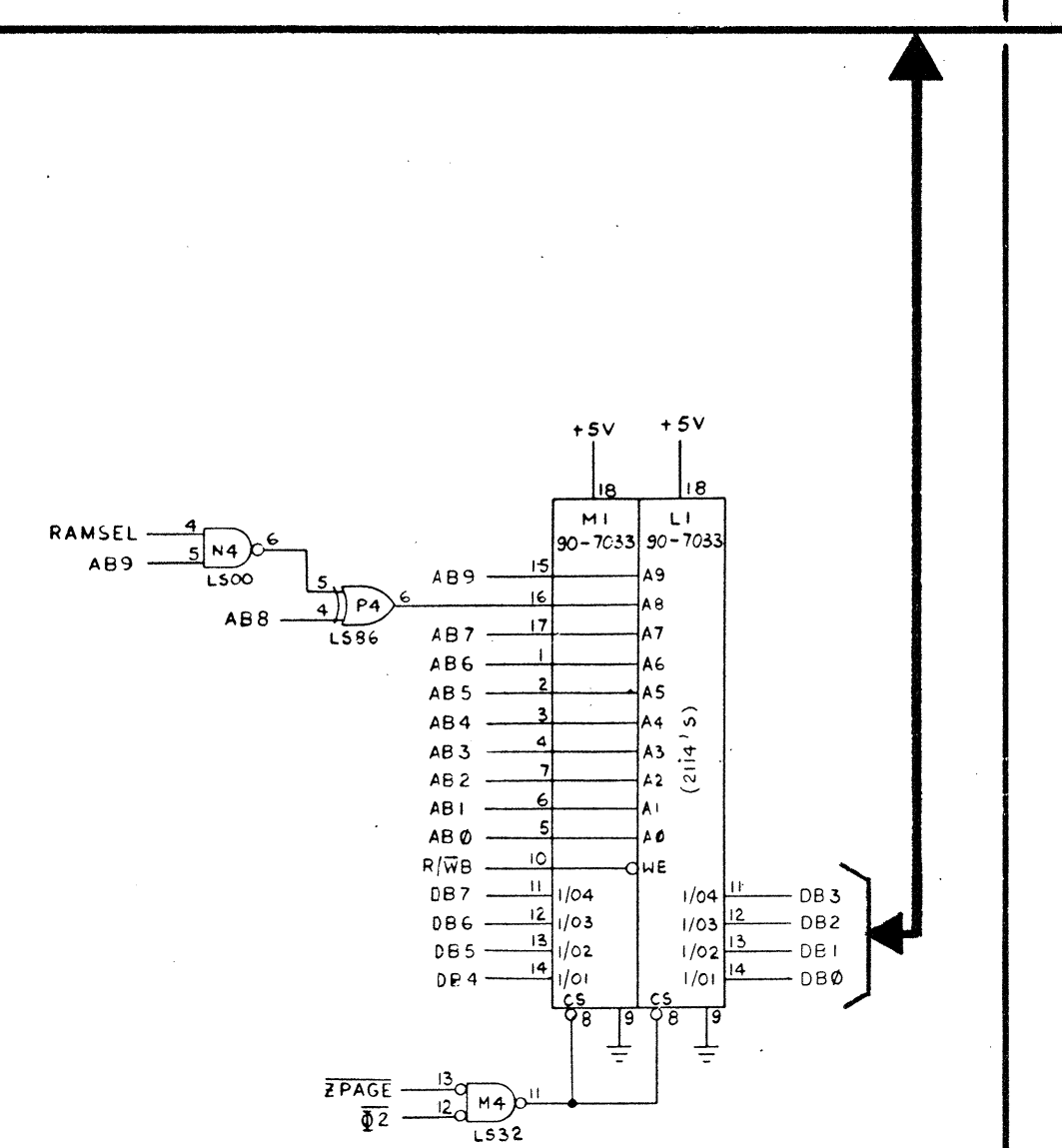
The 25 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR8 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR9 and CR10 rectify the positive pulse of the 25 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR12 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.

Denotes a test point

ROM/PROM CIRCUITRY

**FROM SWITCH INPUTS
SHEET 2, SIDE B**

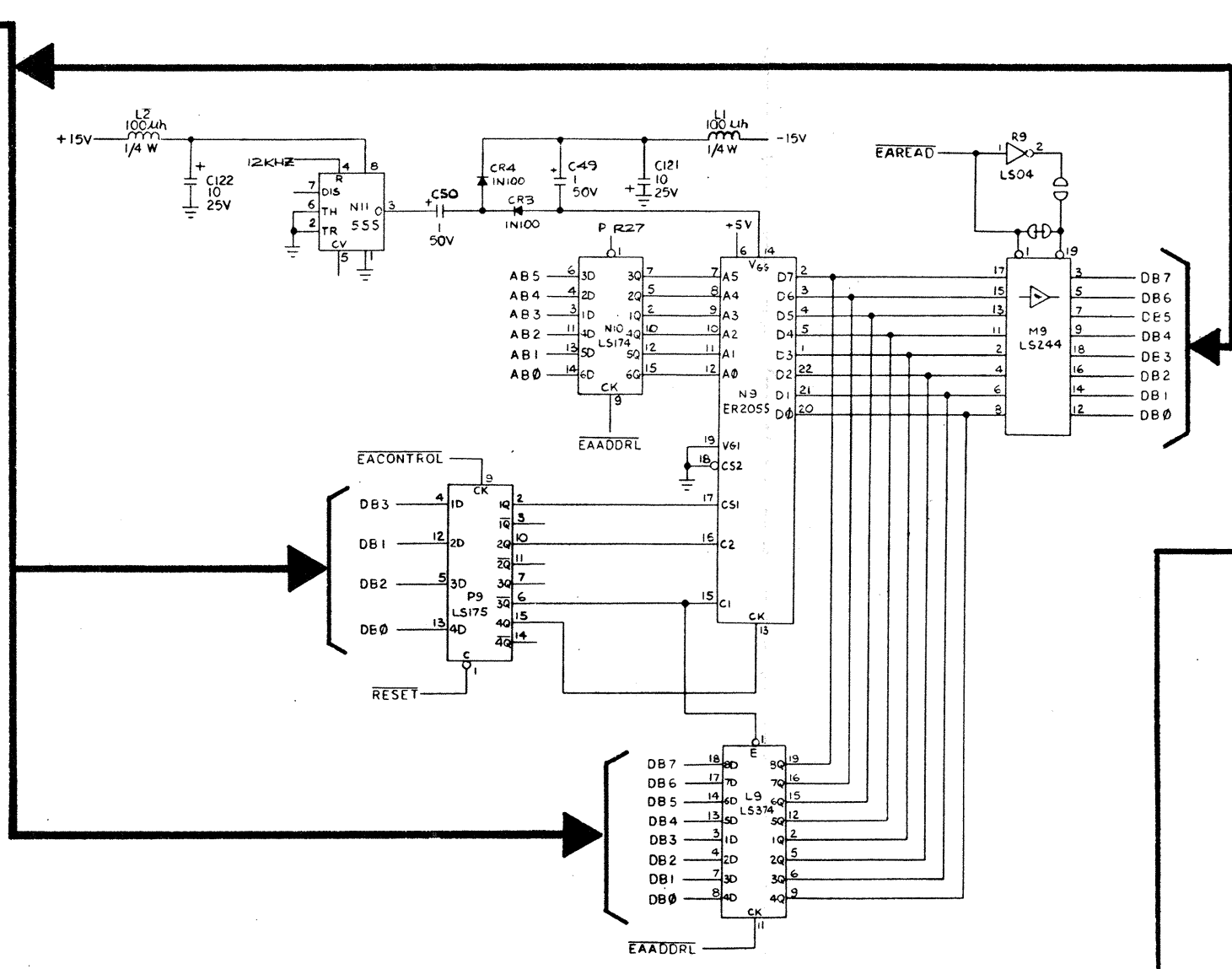Program memory for the Asteroids Deluxe™ game is contained in three ROMs.

RAM CIRCUITRY

The RAM is the temporary storage space for the MPU and is enabled when ZPAGE (Zero Page enable) is low. When R/WB (from the MPU) is low, the RAM stores the data byte input (DB0 thru DB7) at the location addressed by the MPU address bus (AB0 thru AB7). When R/WB is high, the MPU reads the stored data byte at the addressed location.

The signal RAMSEL, when low, has the effect of swapping pages 2 and 3 within the RAM. This allows greater programming flexibility.

HIGH SCORE CIRCUITRY

The High Score Memory circuit consists of an erasable reprogrammable ROM N9, latches L9, P9, N10 buffer M9, and timer N11.

N11 produces a 12KHz O-15V squarewave. This signal when +15, forward biases diode CR4 and allows capacitor C50 to charge the -29V. When it's OV, CR4 is then cut-off and CR3 is forward biased which causes C49 to develop a charge. C49 charges to approximately -28V. This is the potential required for EAROM N9 to operate.

The MPU addresses the EAROM (AB0-AB5) via latch N10, when EAADDRL goes high, and data is latched into the EAROM on DB0-DB7 through latch L9.

The function of the EAROM (read, write or erase) is determined by the MPU on data lines DB0-DB3. Latch D9 receives a high EACONTROL signal from the MPU address decoder and function data is passed to the EAROM.

Data in the EAROM is read by the MPU when the EAREAD is addressed by the MPU after a reset pulse or during self-test.

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Sheet 1, Side B

**ASTEROIDS DELUXE™
Microprocessor
Section of 036471-02 A**

Sheet 1, Side B
DP-165-01 1st printing

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