

STATE MACHINE

The state machine is the "master controller" of the vector ed through latch D8, results in a low BLANK to the Z axis outgenerator circuitry. It receives instructions from the game put. MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program mine how it should use this data: 1) to draw a vector; 2) to move cuting instructions, starting at vector memory location 0. the monitor beam to a new position on the monitor display; 3) to "jump" to a new vector memory address; 4) to return to a that it has completed its current instructions, and is waiting for HALT flip-flop A9, and suspending state machine operation. its next command.

C8, latch D8, clock circuitry A7, and decoder E8. Four bit input tells the ROM that the vector generator has completed its goes high. This means the vector has been drawn. operations.

through its switch input port (buffer M10) on data line DB0. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clock- VMEM goes high.

The microcomputer outputs an address that results in a DMAGO signal that causes HALT to go high, and clears the counter to do so. The state machine reads the vector generator vector generator data latches. This makes TIMERO thru ROM data (via Timer 0-3) and decodes this information to deter-

When the state machine receives the operation code for a previous vector memory address; or 5) to tell the game MPU HALT instruction, it outputs a low HALTSTROBE, setting the

The state machine consists of input gates B8 and E6, ROM and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The HALT input to TIMER0 thru TIMER3 is the operation code input to the state GO flip-flop A9 sets the outputs to ensure that the vector timer machine. The A4 thru A6 address input to ROM C8 tells the and position counters are not active when the state machine is ROM which instructions to perform. Address inputs A0 thru A3 halted. When a low GOSTROBE is clocked through A9, the vecfrom latch D8 tells the ROM which state was last performed. tor timer and X and Y position counters begin to operate from The address A7 input \overline{GO} tells the ROM that the position the GO, \overline{GO} and \overline{GO}^* signals. When \overline{STOP} is clocked through counters are presently drawing a vector. The HALT input to A7 A9, the vector timer has reached its maximum count, and GO

The purpose of the vector timer is to time out the length of time it

takes to "draw" an actual vector on the monitor display. During the

interval when the X and Y position counters are actually drawing the

vector, STOP is high. This prevents the vector generator state

machine from advancing to its next state until the vector currently

being drawn is completed. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next

The vector timer consists of multiplexer F6, decoder E7, LATCH

M7, ADDER M6, and counters B7, C7, and D7. M7 contains a scale

factor which is added in M6 to the four timer signals. If TIMER0 thru

TIMER3 inputs are any state but all high, decoder E7 directly

decodes the sum and loads the decoded low into one of the

counters. When \overline{GO} goes low, the counters count from the loaded

count until the counters all reach their maximum count. This count

is a maximum length of 1024. At this time STOP goes low and clears

If the TIMER signals are all high, ALPHANUM goes low and data

signals DVX11 and DVY11 are decoded by decoder E7. This is added

state in its intended sequence.

the GO flip-flop of the state machine.

to the scale factor and loaded into the counters.

The GO signals load and enable the vector timer and the X

The VGCK input to the clock circuitry is a buffered 1.5 MHz During initial power-up of the game, the HALT signal is clock signal from the microcomputer. This is the same frepreset low. The microcomputer reads the high HALT signal quency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until

The X and Y position counters are two identical circuits. Therefore, the following description discusses only the X position

The X position counters contain rate multipliers (J8 and K8), down/up counters (C9, D9 and E9), multiplexers (D10, E10, and F10), and associated gates (B8 and H10). The output of the down/up counters is a 12-bit binary number that represents the horizontal location of the beam on the monitor screen (or X axis), with 0 being the far left side of the screen and 1023 being the far right side of the screen. Increasing or decreasing this binary number output will cause the beam to move to the right or left, respectively. The vector generator state machine decodes instructions from its memory, and then is capable of using that data to alter the binary count of these counters in one of two ways.

The state machine can preset these counters to an entirely different number from their previous contents. This will cause the beam to "jump" to a new location on the monitor screen instantaneously, i.e., for drawing a new vector from a different starting

"jumping" to this new position, the beam itself is turned off to prevent unwanted lines from appearing on the screen. To preset this new position into the counters, the state generator causes LDSTROBE to go low. At this time, a new 12-bit number (DVX0-11) is loaded into the counters from the vector generator memory data

CK QA QB QC QD

D9 LS191 COUNTER

CK QAQB QC QD

CK QA QB QC QD

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different lengths will still be displayed with the same relative beam inposition than where the previous vector ended. While the beam is tensity. DVX10 and 11 are loaded directly into the counters. DVX10

to control the select input of multiplexers D10, E10, and F10. The UNMDACX1 thru UNMDACX10 (X axis unmultiplexed digitalto-analog converter signals) are transferred and stored at the output of the multiplexers on each rising edge of the 6 MHz clock (from the microcomputer clock circuitry). The DACX1 thru DACX10 signals are sent to the digital-to-analog converters (DACs) in the X video

XVLD 9 88 8 BVLD

axis output, BVLD (beam valid).

The DACX1 and DACX10 outputs represent the physical placement of the beam on the monitor. The far left of the monitor screen is 0, the center is 512, and the far right is 1023. Therefore, if the DACX1 thru DACX10 signal was greater than 1023, the monitor beam would go off the right side of the screen and start again on the left side of the screen, a "wraparound" condition. To prevent a wraparound, the multiplexers' select input from UNMDACX11 goes high when the count is greater than 1023 or less than 0. This selects NMDACX12 to be output from the multiplexers to the DACs, forcing all zeros or all ones, and thus keeping the beam on the appropriate side on the screen, instead of allowing it to wraparound. The XVLD and YVLD (X and Y valid) outputs from the X and Y positon counter multiplexers are gated together to enable the Z

Sheet 2, Side A **ASTEROIDS**

UNMDACY12



Video Generator

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Sheet 2, Side A

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