FLUKE

TroubleShooter

For Digital Board Test Applications

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Inside the Troubleshooter

Increasing the speed of RAM testing with HyperRAM

The new HyperRAM test algorithm (patent pending) was developed by John Fluke Mfg. Co. to provide fast RAM testing while retaining comprehensive fault detection capabilities. HyperRAM is included in Fluke's new HyperTEST™ procedure for fast functional memory testing with the 9100 Series Digital Test System and the 9000 Series Micro System Troubleshooter. Also included in HyperTEST is HyperROM, a new algorithm that greatly increases the speed of ROM testing.

RAM test algorithms and techniques

Various RAM test algorithms now in use balance the need for thorough testing with available test time. Each of these tests sacrifices some fault detection capability to reduce testing time.

The simplest form of RAM test is the read/write test commonly used in power-up self tests. At the other end of the spectrum are complex multipass tests such as the 30N (where N is the number of accesses per memory location), 16N, and 14N tests that improve fault coverage at the expense of speed.

In between the simple read/write and the complex multipass tests is Fluke's 5N probabilistic test called RAM Fast. This patented RAM test algorithm covers most common faults deterministically while detecting other less common faults probabilistically. The chance of detecting faults probabilistically improves with multiple executions of the test or with multiple occurrences of similar faults. The faults detected probabilistically by the RAM Fast test commonly cause multiple occurrences of similar failures. The RAM test algorithm uses pseudo random data to perform five accesses to each RAM address. The speed and fault coverage of this test are excellent.

Fluke's recently developed HyperRAM algorithm expands on the RAM Fast test by providing much faster execution while retaining the same fault coverage. Rather than using an infinite string of random data that must be calculated at each address location, the HyperRAM test uses a small fixed set of random data before beginning the test. This fixed block of random data is reused as many times as necessary to cover the entire range of RAM addresses tested. Eliminating data calculation and utilizing fixed block sizes vastly improves test speed.

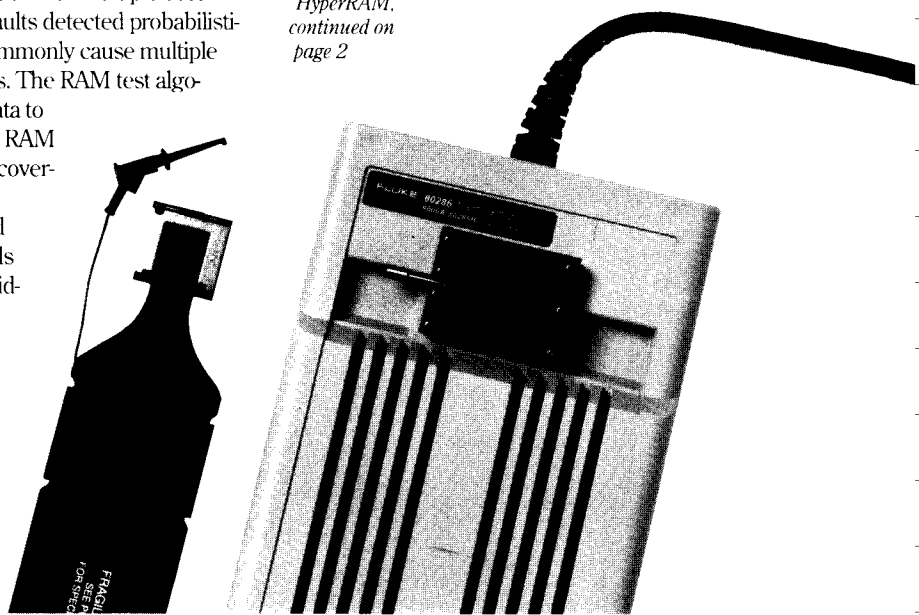
The HyperRAM algorithm, along with optimized test methods, has been incorporated into the 9000A–80286H Microprocessor Interface Pod. The 80286H pod with HyperRAM capability is supported by the Fluke 9000 Micro-System Troubleshooter and the 9100 Digital Test System. Future pods will also incorporate the HyperRAM test function.

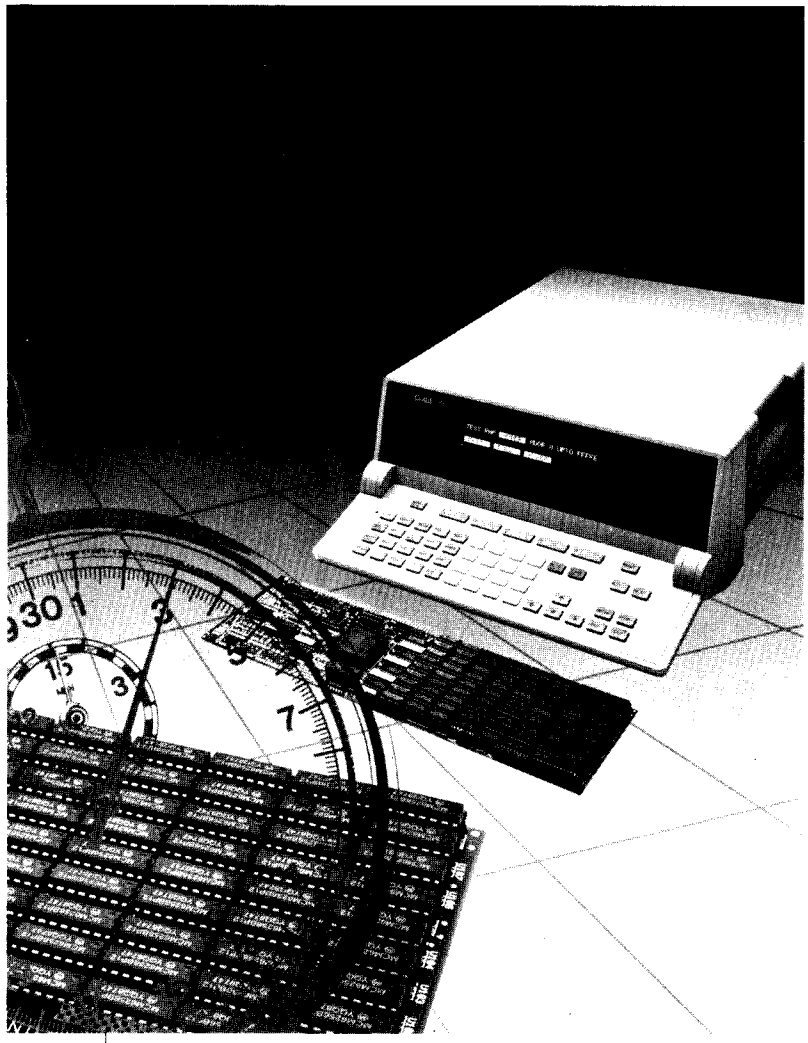
Optimizing features of HyperRAM

The HyperRAM test implemented in the 80286H pod has been optimized beyond the test algorithm. HyperRAM test speed was increased by programming the algorithm in assembly language instead of a high level language like C. To further increase the speed of the HyperRAM test, the 80286H pod uses the following optimizing features:

- memory emulation of overlay RAM
- native processor execution (RUNUUT mode)
- breakpoints

"HyperRAM," continued on page 2





...The HyperRAM algorithm executes a test up to 60 times faster than the RAM Fast test.

HyperRAM...

(cont. from pg 1)

The HyperRAM test is executed in the RUNUUT mode while the algorithm resides in the overlay RAM in the pod. This allows the RAM test to execute considerably faster than traditional microprocessor emulation, since no bus switch or single step operations are required. Further, since overlay RAM in the 80286H pod is high speed, with zero wait states, RUNUUT executes test instructions faster than some UUT based self tests.

Breakpoints send signals to the host test system that a test is complete. A "break" occurs once a preselected event has occurred, such as reaching a specific address or data pattern. Once the test is complete, information can be extracted from memory by the test system. Breakpoints can also be used to check the status of the HyperRAM test without stopping the test. If the test is still running, a "busy" signal is returned to the host test system.

Implementation of HyperRAM

The Fluke HyperRAM test utilizes all of the optimizing features mentioned earlier. The HyperRAM algorithm uses the 80286's string move and compare instructions where possible to quickly copy or test large sections of memory. The test is executed in protected mode, allowing access to the 80286's entire 16M byte address space. Breakpoints allow the 80286H pod to communicate status information to the host test system at regular intervals.

HyperRAM is executed on the 9100 Series in immediate mode by selecting the "HYPER" softkey under the "RAM TEST" menu. This invokes a TL/1 program which requests the RAM test parameters and passes them to the pod. The user enters values for the address space including the starting address, ending address, random number seed, and delay. The TL/1 program then starts the test, monitors its progress, invokes a diagnostic routine if the test fails, and reports the results.

Execution on a 9000 Series instrument is accomplished by writing test parameters to special addresses in the pod using the basic WRITE operation. The test begins executing when the last parameter is entered. Test status is monitored by performing READ operations. On completion, the diagnostic information (e.g., failed address, expected and actual data) is read from additional special addresses in the pod. For more information on performing the HyperRAM test on the 9000 Series Troubleshooter see the 9000A–80286H Istruction Manual, Section 3.

Using a 9100A Digital Test System and a 9000A–80286H Interface Pod, the HyperRAM algorithm executes a test up to 60 times faster than the RAM Fast test (depending on the size of the memory being tested). When testing the memory of an IBM PC/AT, configured with 512K bytes of DRAM running at 6 Mhz with 1 memory access wait state, the test time was reduced from 165 seconds, using the RAM Fast test, to 6 seconds. Test time was reduced from 11 minutes to 13 seconds when testing a 2 Mbyte Intel Above Board 286 expansion RAM card.

Conclusion

As microprocessor-based products become more complex and more memory space is

HyperRAM Fault Coverage

The HyperRAM algorithm detects two types of RAM faults:

- Those that exist (or do not exist) with 100% certainty.
- Those that are detected part of the time with a specified probability.

Although the second category of faults are only detected part of the time, multiple faults multiply the probability that at least one will be detected. The HyperRAM algorithm is designed to detect faults that typically occur in more than one place. For example, address, row, or column decoder failures all cause large sections of RAM to fail simultaneously. If as few as 32 locations are affected (even though the probability of finding a single isolated fault might be only 50%), the chances of not detecting at least one fault in 32 is 1 in 2.15 x 10^9.

Many different types of RAM faults are detected by the HyperRAM algorithm, including stuck memory cells and aliased cells. Stuck memory cells always present the same logic level, 1 or 0, regardless of what the level should be at a particular location. Aliased cells are cells that are effectively "shorted" together; this occurs when data written to one cell is written to other cells. Aliasing may also occur when a single cell is selected on read and write operations even though different addresses are specified.

Faults detected with 100% certainty include:

- Stuck memory cells.
- Stuck data lines.
- Stuck address lines.
- Shorted address lines.

added, demand for a faster RAM test will continue to rise. HyperRAM is designed to answer these demands by optimizing test times without sacrificing the test coverage expected of modern, high quality RAM tests. ■

- Cells at different addresses that are aliases.
- Uni transitional stuck at fault (the cell initially contains one level, but gets stuck after a write to the opposite level).

Faults detected part of the time include:

(The numbers in parentheses indicate the probability of detection on a single test execution).

- A pair of cells within the same address that are aliases (50%).
- Data written to a cell overwrites data in a cell located at a different address (50%).
- Data read from a cell is actually read from a cell located at a different address (aliasing) (75%).
- A cell value that is influenced by the value in a second cell (50%).
- A cell value that is influenced by the value of an address line (50%).
- A cell value that is influenced by the values in N other cells (pattern sensitivity) ($100 \times (.5^N)\%$).
- Shorted data lines, where N is the number of addresses affected ($100 \times (1 - .5^N)\%$).

The HyperRAM test also detects dynamic RAM refresh problems. If the test is invoked with an adequately large delay parameter, all RAM refresh circuit failures are detected. Occasionally, it is necessary to disable the pod's "standby read" feature so that standby reads do not artificially refresh the RAM.

Newsfront

90 Series News— Application Note

The 90 Series Board Testers are surprising many users with their simplicity of operation. However, the turn-on with the unit under test may require special consideration for the way the designer handled some elements of his design. To address this issue Fluke offers an Application Note, "Getting Started with the 90 Series" with seven pages of hints to help insure success. This is highly recommended reading for the service engineer and may provide good advice for the designer as well on the topic of "designing for testability."

Philips Instruments complement Fluke line of board testers

To complement our line of board testers, Fluke offers a broad line of technologically innovative, high performance logic analyzers and digital storage oscilloscopes, with unprecedented ease-of-use. The Philips logic analyzers are ideal for hardware-software integration, plus hardware and software development.

Philips digital storage oscilloscopes offer advanced features like 2GHz bandwidth, user programmable set-up memories, and unmatched calculating and analysis capabilities. Also featured is AUTOSET, for automatic selection of channel, amplitude, timebase and trigger to provide error-free display of any input signal. Philips DSO's also provide a wide range of performance in speed and resolution to capture, display, measure and document even fast-changing signals in a variety of applications. For more information contact Fluke at 1-800-44-FLUKE ext. 77.

9100 On-site service

On-site service for your 9100s is now available. If you're using your 9100s for production test, or they find their way into a critical repair turnaround environment, you demand guaranteed uptime. For approximately 2.3% of the acquisition price, you get on-site repair service that supplements your 90 day warranty and meets this demand. After the end of the 90 day warranty, for only about 6% of the acquisition price, you get extended warranty coverage as well as on-site service for one year to help keep your test operation running smoothly.

In the U.S., call 1-800-44-FLUKE, ext. 73, to find out more about this Fluke service. To order this service in other countries, call your local Fluke representative.

Free training available for 9100 and 9010

With the purchase of a mainframe, Fluke offers free training for 9100 and 9010 customers. Ask your Account Manager about a certificate entitling you to either a hands-on application for the 9010, or a hands-on application and programming course for the 9100. The courses are specifically designed to drive your performance curve higher. This program has been in effect from July 1, 1987 for U.S. customers. Only one certificate per mainframe.

QuickTools ™ Software for the 90 Series

Fluke introduces QuickTools, a software package designed for remote operation and control of the Fluke 90 Series through an IBM PC or compatible. QuickTools makes remote operation of the 90 Series as easy as using the Tester's front panel. This package allows you to use not only all of the 'local' features via the RS-232 interface, but also accesses features not available through the front panel, including:

- Break-Point
- Frame-Point
- External Trigger
- Upload
- Download
- Memory Fill
- and many others!

Also built into QuickTools are features which allow the operator to:

- Stimulate entire board through creation of batch tests
- Create & edit programs using built-in program editor
- Record or print entire interaction between 90 Series and PC
- Make easy remote command syntax calls via pop-up prompting
- Check out program steps on 90 Series while in 'Interactive' mode
- Execute short sequences with function keys

Price: $300, U.S. List ■

A Case History

Using the Fluke Troubleshooter for production testing

By Edward A. Gedeon

The evolution and future direction of a production test system.

For several years, a major manufacturer has been using Fluke Troubleshooters and Instrument Controllers for production testing and repair. Described below is the evolution of the test system and its future direction.

Developing the need

A division of the company is the leading manufacturer of newspaper and commercial printing equipment. In 1979, the "electronics" of a press consisted mainly of switches, relays, and miles of point-to-point wiring. The first microprocessor based systems had just reached the drawing board. These early systems were either functionally identical replacements of older electro mechanical designs, or add-on features that performed single functions such as aligning the margins of the paper entering the press. These new features were very popular with customers, and orders for microprocessor controls increased steadily.

The increased production that followed required increased testing capabilities. At first, each new design had dedicated, stand-alone test fixtures with varying sizes, shapes, connectors, procedures, and test difficulty. One tester had 121 switches and 104 lights on the front panel and stood seven feet tall. It was commonly referred to as "The Port-a-Potty".

Not all fixtures were this complex. For example, our group designed a tester for a microprocessor-based board with separate kernel, RAM, ROM, and I/O line tests. The tests could be run individually or in sequence, with error messages displayed on an alphanumeric display. One could step through a test, loop on an error, or abort the test program. This test fixture was very successful. However, it was designed for on board testing only. We were faced with redesigning identical features into every fixture for each new circuit board. Fortunately, the Fluke 9000 Series has helped simplify the development of test fixtures.

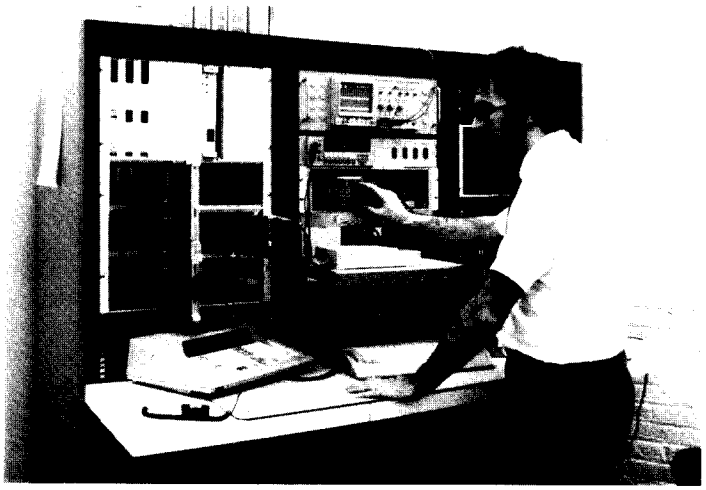
The 9010A Troubleshooter performed all the functions of our previous test system, but was simpler to program. After spending five years working with assembly language, the 9010A instruction set was a welcome change. The 9010A language compiler made programming simpler. Software development time was reduced and the only additional hardware was easily satisfied with off the shelf I/O boards and interface cables.

Used alone, the 9010A still has a few drawbacks. Program size and complexity are limited. Prompts and error messages are limited by the 32-character display. Trying to perform simple arithmetic with the 9010A is difficult, even with the utility subroutines developed by Fluke. These problems were eliminated when the current system was adopted: A 9020A Troubleshooter coupled with a Fluke 1722A Instrument Controller.

The current system

The Fluke 1722A Instrument Controller was first used in 1985, and since then, test programs for over fifty different circuit boards have been developed. The 1722A uses the IEEE–488 bus to control the 9020A Troubleshooter and the 6809 Interface Pod. Test menus and programs are displayed on the touch screen; in most cases, the test operator can run the entire program using only the touch screen. A second 9020A was added to develop an intelligent serial I/O board based in the Motorola 68008 µP. This board was tested using a 68000 pod and an adapter. We kept both test programs in the system, using one for testing 8-bit boards with the 6809 pod, and the other for 16-bit boards using the 68000 pod. We recently added a Fluke 8840A DMM connected to the IEEE-488 Bus and under control of the 1722A.

The remaining hardware in the test system consists of a STD Bus Card Cage (for 8-bit boards), a Gespeac G 96 Card Cage (for 16-bit boards), a power panel which makes various DC voltages available for test purposes, and a



few special purpose interface and I/O boards to monitor signals output from the UUT. We have designed our own interface boards using off the shelf I/O boards.

Test programs are written in BASIC and stored on 5 1/2" diskettes. To help reduce software development time, a library of subroutines for common functions such as touch screen input, menu generation, error handling, and program chaining has been developed. Programming time ranges from one to four weeks depending on the complexity of the board.

Originally, boards that were installed in the same chassis had their programs stored on the same diskette. Soon, two problems arose. First, some systems were more complex than others, so that some diskettes were filled to capacity while others held only two or three programs. Second, when a technician on the manufacturing floor was given a new board to test, he was confused about which diskette contained the test needed. The problem was solved by putting the test programs in numerical order, using the part numbers of the boards being tested, and labeling each diskette with the range of boards it tested.

A typical board test is performed as follows. The test system is set up with the 1722A, or 9020A with interface pod, a CPU under test, and one or two I/O boards. The diskette is loaded into the 1722A disk drive. Then, the menu driver and all of the test programs are copied to the 1722A internal RAM. The IEEE-488 port is initialized, the BASIC shell is loaded, and the main menu is generated, listing all of the test programs on the disk. The test operator touches the 1722A screen next to the name of the test and that test program is executed. As the test progresses, results are displayed on the 1722A's screen. In case of an error, the fault is highlighted, and the operator is given the option of looping on the error, ignoring it and continuing, or aborting the test program and returning to the main menu.

On completing the test, the operator can either return to the main menu or repeat the test program. This "repeat" feature is used to test batches of identical boards. The operator turns off DC power to the card cage, replaces the board just tested, restores power, and restarts the test without re-initializing the system.

Future considerations

The present system has some limitations. Newer test programs take longer to execute because of the complexity of the boards. Because of the limitations of the 1722A and the 9020A, memory testing is becoming a bottleneck. A typical board has 256K to 1 megabyte of RAM. Even with the "Quick RAM" test used by the newer interface pods, 1 megabyte takes over 12 minutes to test. EPROM testing is equally time consuming, as the production software becomes more sophisticated and program size grows geometrically.

Another drawback to the present test system is the bandwidth of the IEEE-488 bus. On one board, two 512 byte FIFO buffers were tested. This required writing thousands of bytes of data from the 1722A to the 9020A, one at a time, then reading them back, and checking the "buffer empty" and "buffer full" flags for errors. Program execution time was 15 minutes for testing a single board.

Still another problem is that the 9020A is designed to operate only with microprocessor-based boards. This means that peripheral boards usually need additional circuitry to interface to the test equipment. As soon as the design engineer has finished a new board, additional time must be spent designing an additional board just to test the first board. The more complex the test set up, the more complicated the test program: 500 line programs are typical.

Fortunately, the 9100 Series of testers offers solutions to exactly the type of problems we are now facing. The 9100A Digital Test System operates much faster than our present system, mostly because there is no IEEE-488 bus. New memory tests are up to 30 times faster than the "Quick RAM" and "Quick ROM" tests now in use.

Instead of designing special interfaces for each design, the I/O modules monitor up to 160 signals. The 20 Mbyte hard disk provides more than enough storage space for our test programs. The programs we have written so far would fill about a quarter of the hard disk. Now, programs can be written in a high level language designed for testing.

Best of all is the built-in fault tracing algorithm. Given a list of devices and interconnections for a particular board, the 9100A can guide the test operator through the troubleshooting procedure. It may also be possible to download interconnection and part information from the CAD system, which would reduce software development time to a few days.

There has been a great deal of success with the test equipment, and Fluke products will continue to be used in the future. With Fluke's help, this manufacturer has applied state-of-the-art electronics to its newspaper and commercial printing equipment.

"The 9100A Digital Test System operates much faster than our present system..."

The benefits of emulative testing

Being application specific, like emulative testing is, has its advantages. Testing is faster and it enforces a logical troubleshooting approach. It even makes general purpose instrumentation like oscilloscopes work better in dynamic µP based circuitry by providing control and stable stimulus.

A. Faster Testing

Emulative board test speeds testing and troubleshooting because it's tests cover the circuits functions so well. This board coverage is achieved because the tests work like the circuit was designed, with the µP in control, in real time.

"Case History," continued on page 12

Diagnostic programming of the Intel 8237A and AMD 9517A

By Frank E. Perry
Techpro Corporation

The DMA Controller

A Direct Memory Access (DMA) Controller is a peripheral interface circuit designed to improve the system performance of microprocessor systems by allowing and controlling high speed data transfers to or from memory and peripheral devices independent of the CPU. The Intel 8237 and AMD 9517A are identical devices: they are programmable, and they have an equal number of data, address, status, and control registers to be addressed under program control to initiate and complete DMA operations. Both controllers support four independent DMA channels.

Within the space limitation of this article it will not be possible to reprint the many technical details describing these controller chips. If the reader is not familiar with some of these details, we recommend he/she consult the Intel Microsystem Components Handbook or the AMD AM 9517A Technical Manual.

Diagnostic Programming

To program the DMA controller, you must test the following:

- The integrity of the data and address buses
- The integrity of the read/write registers
- The internal addressing of the registers
- The request and ask capabilities
- The transfer functions

The Static Test

To program the DMA controller, the first step is to verify that the controller can be statically addressed by the CPU. This is easily accomplished by writing and reading the master clear address and the channel 0 address register. To perform a more complete test, write to the First/Last Flip Flop to set the low byte. Then write a 55hex to the lower byte, followed by an AAhex to the upper byte, and read it back. Then write an AAhex to the lower byte, a 55hex to the upper byte, and read it back. This will detect any stuck or tied bit in both the upper and the lower bytes. To test the First/Last Flip Flop, the lower byte should be read, followed by the register to read verify the least significant byte and the most significant byte of the register. The next write should be made to the register, leaving an arbitrary number such as the address of the register. This procedure should be performed for each address and count register followed by reads of all of the registers to verify that none of the registers were disturbed by a write operation to any of the other registers.

The Verify Test

After statically testing the DMA controller, it is necessary to perform dynamic tests. Dynamic tests are facilitated by the 8237A's verify mode. When verify mode is selected, the controller performs the behavior of a DMA transfer internally without exerting any signals on the address or control lines. To perform a verify operation, an OFhex should be written to the Write All Mask Register Bits register at address base + F to prevent any external requests from interfering with the test. Next, a starting address should be written to the address register of the channel being tested (0 for example) and a count should be written to the count address, (FFFE for example). The Control Register needs to be initialized to a normal state of operation. The Mode Register for the channel should be written to: Select Block mode, address increment, auto initialized disable, and verify transfer. Next the request register should be set to the proper channel. After an appropriate pause for the operation to finish, the status register should be polled to verify that the terminal count is reached, the address and count registers should be read to see if they show the proper values. In the previous example, both registers should read FFFFhex.

The Functional Test

The final test verifies that the controller transfers data. This is accomplished with the memory to memory transfer mode. A section of memory should be loaded with a recognizable pattern. Channel 1 should be programmed to transfer sufficient memory to test the outputs of all 16 address bits of the 8237A. The command register must enable memory to-memory transfer and disable channel 0 address hold. Channel 0 is set to read transfer mode and channel 1 to write transfer mode. The transfer is then requested. After the terminal count has been reached, memory is compared to determine if the data was transferred correctly. In some systems it is not possible to perform a memory to memory transfer due to the structure of the data bus.

"A component as complex as a DMA controller has equally complex interfaces with the system in which it is designed"

Analysis

Failure data from any of the above tests need to be interpreted and analyzed with care. A failure does not automatically result in a valid accusation of the DMA Controller chip. It is important to note that a failure may or may not indicate that the 8237A is faulty. A component as complex as a DMA controller has equally complex

interfaces with the system in which it is designed. A failure may indicate that one of the components that surrounds the controller is faulty rather than the controller itself.

The most ambiguous failure is a failure of the reads of the address and count registers during the Static Tests. If all the registers fail, first check the address and data lines to the 8237A. If these lines can be verified by testing other devices on the same bus (such as the I/O read and write lines and the chip select lines) and test good, then the 8237A is faulty. If some registers pass and others fail, or if the final read operation of the data left in a register fails while the test of the address bus passes, the 8237A is faulty. If a data transfer to the least significant byte passes but the transfer to the most significant byte fails, or vice versa, then the 8237A again is at fault.

The verify test is performed internally. Any failure during this test indicates that the 8237A is not functional and needs to be replaced.

The functional test is system dependent. If a memory to memory transfer fails, the 8237A is suspect; attention should also be focused on components that connect the DMA controller to the data, address and control lines. To further complicate matters, some systems employ channel 0 of the DMA controller to take care of the dynamic RAM refresh. If this register is not restarted immediately after the test, data may be lost and the test pattern in memory may be invalid.

Summary

Functional testing of the 8237A DMA controller is complex. The DMA controllers in and of themselves are very complex. In addition, the DMA controller is interconnected with many components of a computer system because it exchanges information with the memory, peripheral devices and the system control lines. ■

Programming multiplication and division on the Fluke 9010A

By Clinton Koskie
Ramsey Technology, Inc.

Teaching the Troubleshooter.

In testing boards manufactured at Ramsey Technology, it is often necessary to find the ratio of two values. Although finding ratios is a simple matter of division and multiplication, the 9010A can't do math. It isn't even capable of first grade arithmetic like addition and subtraction, let alone more advanced mathematics like multiplication and division.

The addition and subtraction came easy. Fluke offers a utilities tape (9000A–910) that lets the operator perform addition or subtraction on specified registers. With these programs, any two registers can be added or subtracted and the result stored in any selected register. The registers involved in the operation are defined in REGB. For example, if REGB = 398, the operation is performed on REG8 and REG9, and the result stored in REG3.

When using the Fluke language compiler, call the addition routine PROGRAM BINADD and the subtraction routine PROGRAM BINSUB, for example. This makes it possible to locate these programs anywhere in the main program.

Once the 9010A has learned to add and subtract, it is simple to teach it to multiply and divide. One method is through successive addition, but this can take a very long time. A better method is to shift and add (or subtract). With this algorithm, any multiplication operation will take less than .25 seconds. This is slow by most standards, but quite fast for a machine that was never intended to do mathematics.

For the multiplication routine, the multiplicands are brought into the program in REG8 and REG9, and the result is returned in REGB, REG8 and REG9 are not affected.

To increase the accuracy of the result, the division routine is indirect; the dividend is first multiplied by 16 (shift left four times). With the division routine, REG9 is divided by REG8 and the result is returned in REGB. The result returned in REGB in 16 times the quotient of the division because of the scaling of the dividend. The calling program must take this into account.

For both routines, the 9010A register size limits each operand to 32-bits (FFFFFFFF). However, the routines still outperform most calculators. ■

```
PROGRAM MULT
    REG2 = 0
    REGB = 212          ; set up REG assignments for BINADD
    REG1 = REG9
    REG4 = REG8
1: LABEL 1
    REG3 = REG4 AND 1   ; if (LSB of REG4 = 1) then
    IF REG3 = 0 GOTO 2
    EXECUTE BINADD      ; REG2 = REG1 + REG2
2: LABEL 2              ; REG2 contains: partial result
    SHL REG1            ; REG1 = REG1 *2
    SHR REG4
    IF REG4 > 0 GOTO 1
    REGB = REG2
```

```
PROGRAM DIVIDE
    REG1 = REG9 SHL SHL SHL SHL     ; REG1 = Dividend * 16
    REG2 = 1
    REG4 = REG8                     ; REG4 = Divider
    REGB = 114                      ; Set up Register assignments for BINSUB
    REG3 = 0
1: LABEL 1                          ; Scale REG4 such that
    SHL REG4                        ; REG4 * 2^n > REG1
    IF REG4 > REG1 GOTO 2           ; and
    SHL REG2                        ; REG2 = 2^n
    GOTO 1
2: LABEL 2
    SHR REG4
3: LABEL 3
    IF REG1 >= REG4 GOTO 4
    SHR REG4
    SHR REG2
    GOTO 3
4: LABEL 4
    EXECUTE BINSUB                  ; REG1 = REG1–REG4
    REG3 = REG3 OR REG2
    SHR REG4
    SHR REG2
    IF REG2 > 0 GOTO 3
    REGB = REG3
```

The Fluke 90 series: A new emulation technique in testing

A new low-cost and efficient board test solution.

The recently introduced Fluke 90 Series incorporates the DMA method of emulation testing. How does a tester employing this technology operate to perform fault isolation and board testing tasks?

DMA Emulation

DMA emulation is a test approach that fits the critical timing requirements and soldered in manufacturing methods of many new microprocessor-based boards. For several tests, the DMA emulative type tester does not take complete control of the board under test as in the CPU emulative test method. It actually performs tests while the board is operating in its normal environment. This is accomplished by taking temporary control of the address and data buses while the microprocessor is performing internal operations or while the microprocessor is placed in a hold state for a brief period of time.

Because the DMA emulative tester only borrows the address and data buses, it does not require that the microprocessor be removed from the board-under test. The tester simply clips directly to the in place microprocessor or microcomputer, socketed or not, to make its connection to the buses and control lines of the board under test.

Like the CPU emulative tester, the DMA emulation does not require the kernel to be fault free in order to conduct a full set of tests, although CPU emulation usually is able to test a larger portion of the board.

Unlike both CPU and ROM emulation, testing can take place while the board performs its normal operating functions. This means that troubleshooting can be performed on boards that have all components soldered in place or exhibit an intermittent problem when running their own control software.

DMA emulation requires that the microprocessor on the board under test supports DMA and that the DMA request line not be directly tied to ground or VCC. The DMA support requirement limits the ability to test microcontrollers, (devices that contain the CPU, RAM, ROM and I/O interfaces in a single chip) from being tested by the DMA emulative tester. They do not support DMA because their bus and control line structure is contained completely within the chip. Also, some of the first generation microprocessors do not support DMA I/O operations.

The DMA emulative testers generally allow for better price/performance. Tester cost is lower while supporting all preprogrammed kernel testing (i.e., bus, RAM, ROM, I/O), and beyond the kernel troubleshooting with synchronized logic probing and bus line identification.

CPU Emulation

The testing of microprocessor-based equipment by means of CPU emulation has been an effective tool for several years in the 9000 Micro System Troubleshooter Series and the 9100 Digital Test Systems Series. With this approach the tester gains access to the board by means of the microprocessor socket. In most cases, the microprocessor is removed from its socket and the tester, which employs a similar microprocessor, is connected in its place.

CPU emulative testing provides an effective means of testing and troubleshooting the board since test access is at the heart of the board. Testing can be performed even when the trouble symptom is a failed CPU, an associated component or one or more bus lines. The emulative tester requires an interface adapter (often called a pod) to adapt it to the microprocessor on the board-under-test.

The microprocessor in the interface pod, which is similar to the one removed from the board under test allows the tester to take complete control of the board under test. The tester has access to all elements of the kernel (address bus, data bus, RAM, ROM, I/O, etc.) as well as circuits beyond. Complete control of the board under test is available, even to the point of performing single read and write operations to any address.

With the 9000 Series, measurement beyond the kernel is available through the single point probe. The probe can capture activity on any node of the UUT using simultaneously (1) the Signature Analysis technique, (2) transition (frequency) counts and (3) a logic level history. The tester provides the stimulus for a node and the probe measures the resulting activity at that node. By comparing the result obtained on a known good board with that of the board under test, the 9000 Series can achieve full board coverage.

The 9100 Digital Test System expands on this capability with multiple measurement points. Up to 160 points can be added to the 9100A; each of these points has the capabilities of the single point probe described for the 9000 Series above. For both the 9000 and 9100 Series products, the probe or the I/O points may be used to stimulate a node (or multiple nodes) and measure the response at the UUT microprocessor.

The Troubleshooter has addressed many unique applications of CPU emulation over the years.

Low Cost and Efficient Board Testing

Microprocessor-based boards typically are interfaced to a high speed peripheral such as a disk drive, video controller, A/D converter, local area network (LAN), computer aided design (CAD) system, etc., that requires fast data transfers. Typically, DMA is employed to handle these data movements between the RAM and peripheral devices. In this scheme, the DMA controller signals the microprocessor and takes control of the address and data buses.

The DMA emulative tester uses this feature to take control of address and data buses but not for transferring data to or from high speed peripherals. To accommodate the test mode, the microprocessor relinquishes control of the buses as if a DMA operation had been requested by the DMA controller.

The tester contains several packaged test routines that automatically test bus lines, control lines, RAM (both dynamic and static), ROM and I/O functions. The built-in tests, invoked by pressing keys on the control panel, can be executed while the board-under-test is executing its own applications software.

The 90 Series tester is equipped with a test probe that allows logic levels to be checked. The test probe is used with QuickTrace, a method of identifying shorted or stuck address, data or control lines.

With QuickTrace, circuit nodes automatically are identified by name on the tester display when the node is touched by the probe, such as D5 for data line 5. When probing along the bus or signal line, a fault can be indicated when the node no longer is identified on the tester display. Any shorted conditions associated with the test node are reported. QuickTrace also allows specific address, data and control lines to be located at different points throughout the board.

Testing Beyond the Kernel

While bus related tests can quickly pin point a problem to an area (or node) within the microprocessor kernel, they typically cannot trace faults beyond the kernel. If the problem lies outside the kernel, special troubleshooting techniques are needed to isolate the failure.

The DMA emulative tester enables testing outside the microprocessor kernel by taking control of the buses and performing specific tests or monitoring nodes on the board while operating in its normal environment.

By taking control of the buses, specific I/O circuit elements can be addressed and the tester's synchronized logic probe or an oscilloscope can be used to check the addressed nodes. A trigger pulse output furnished by the tester is synchronized to the events generated by the test, allowing examination by the oscilloscope of the conditions on the board.

When testing the board while it is running in its normal operating mode, the trigger output is synchronized to the data valid state on the CPU buses. This tester output permits stable oscilloscope displays for various points on the board regardless of the software being run on the board. The logic probe also can be used in this operating mode to indicate the states of affected nodes.

PC Based Remote Testing Capability

When integrated into a design or test system by means of the RS 232 C interface, the 90 Series tester makes all front panel functions and tests available to the test system. With all tester functions available, programs can be run to perform automated board tests. To assist the user in creating test programs, a special utility program is available to create or edit test procedures. This utility, which can be run on a personal computer, is menu driven and simplifies the writing of test statements that make up the test programs.

In addition to the front panel functions, the remote interface enables expanded testing by accessing functions not available from the front panel. These include memory upload and download commands that allow the test system to write data to designated portions of RAM. They also allow the contents of designated memory RAM and ROM addresses to be passed back to the test system. Remote operation of the 90 Series tester allows trapping of preselected events, such as a specific memory read or write, I/O read or write, opcode fetch or interrupt acknowledgment.

When a specified event takes place, one of three test functions are available to help pinpoint unusual and/or infrequent failures. One function (referred to as breakpoint) halts program operation of the board-under-test when the specified event occurs; the second (framepoint) simply causes the tester to display the status of the address and data lines when the specified event occurs; and the third generates a trigger pulse output when the event occurs. These test functions allow intermittent failures to be detected while the board runs unattended, eliminating the need for the user to monitor the operation of a board that exhibits infrequent failures.

Board Testing, Typical Test Steps

Troubleshooting the microprocessor-based board with the 90 Series tester is performed in a logical manner using the available built-in tests. One of the first checks verifies that no lines of the address, data or control buses are shorted, or stuck high or low. A bus test routine can be invoked that toggles and tests each bus line, then displays the result of the test. With all bus lines checked out as operational, a looping test is performed to toggle all chip select lines. The logic probe verifies that each line is toggled during the test.

The RAM is tested by performing a series of write and read operations to each RAM location. This test verifies operation of the RAM, the corresponding portion

"*Emulation*,"continued on page 12

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emulative tester is the answer. Its small size makes it suitable for field service applications; the remote capabilities facilitate use in a test system environment. ■

Case History...

(cont. from pg 5)

B. Good Characteristics of Troubleshooting

The characteristics of good troubleshooting are designed into the Emulative Board Testers, which can reduce "shotgunning" and improve repair quality.

The logical troubleshooting characteristics include the following steps:

- provide a known stimulus to the circuit
- collect the response
- measure the response
- interpret the measurement
- decide which direction in the circuit to go next.

The above characteristics are critical to ensure quality of repair. Applying them, one can be sure of addressing each part of the circuit in the way it is structured (Bus, RAM, ROM, I/O, etc.) leaving nothing out to hide bugs, defects and faults.

Comparing Fluke Emulative Testers

Troubleshooting is always taught or learned in a logical way but now the Fluke emulative board testers are tools that help enforce the methodology.

The new Fluke 90 Series does its best work simply clipping over the microprocessor, providing stimulus to the device-under-test, clipping over the µP, collecting the response and quickly displaying measurements to the technician or engineer. The user must interpret the circuit measurements, i.e. ROM checksum, logic levels, node identification, etc.

The Fluke 9000 Series (9005A, 9010A, 9020A) is unique in that it provides a similar level of stimulus, response and measurement but adds an important level of test interpretation. Features such as signature analysis (synchronous and asynchronous), logic pulsing, waveform capture, frequency measurements and event counting provides the user with more output to decide what the measurements mean. In this case, several functions are incorporated into one instrument.

The Fluke 9100 Series (9100A and 9105A) delivers on all levels from stimulus to interpretation, incorporating faster memory testing, closed loop digital coverage through I/O modules, etc. Most importantly, it does all of this in a programmed, automated state. The 9100 Series provides an integrated test programming environment, thus offering the user Guided Fault Isolation, or full direction to where to test next to quickly locate faults. ■

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