9000A-006

ASYNCHRONOUS SIGNATURE PROBE

Service Manual

P/N 783944
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FLUKE®

WARRANTY

COVERAGE

Fluke warrants the 9000A-006 Asynchronous Signature Probe to be free from defects in material and workmanship under normal use and service for a period of one (1) year from the date of shipment. This warranty extends only to the original purchaser and does not apply to any product that has been misused, altered, or has been subjected to abnormal conditions of operation.

Fluke's obligations under this warranty is limited to repair or replacement of a product that is returned to an authorized Service Center within the warranty period, provided that we determine that the product is defective. If we determine that the failure has been caused by misuse, alteration, or abnormal conditions of operation, or if the warranty period has expired, we will repair the Probe and bill you for the reasonable repair cost.

SERVICE

If a failure occurs, send the product, postage prepaid, to the closest Service Center with a description of the difficulty. Repairs will be made or the product replaced, and it will be returned, transportation prepaid. Fluke assumes NO risk for damage in transit.

DISCLAIMER

THE FOREGOING WARRANTY IS EXCLUSIVE AND IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. FLUKE SHALL NOT BE LIABLE FOR AND SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

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To enhance your use of this Product, Fluke will be happy to answer your questions about applications and use. Address all correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX C9090, EVERETT, WASHINGTON 98206, ATTN: Sales Department. European customers should contact FLUKE (Holland) B.V., P.O. BOX 5053, 5004 EB, TILBURG, THE NETHERLANDS.

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Section 1
Introduction

PURPOSE OF THE EQUIPMENT 1-1.

Signature troubleshooting supplements the basic functions of the Troubleshooter. This method of troubleshooting is used in situations where the test functions of the Troubleshooter alone do not provide adequate results. This situation usually exists when a fault occurs in a circuit area that operates asynchronously with respect to the processor. In this case, the troubleshooter cannot detect the fault since it is able to examine only processor-synchronous events.

Although the Troubleshooter may not have "visibility" or access into some areas of the UUT, it is usually able to stimulate all functional areas in a consistent and repetitive manner. This type of stimulus is required to take meaningful signatures. The ability of the Troubleshooter to stimulate the UUT makes it an effective tool for signature-type fault isolation methods.

The Asynchronous Signature Option 9000A-006 provides additional Troubleshooting capability for the 9000A series Troubleshooters by using signature-type fault-isolation, events counting, and test-node waveform capture. Control signals from the UUT establish the signature and allow asynchronous operation with respect to the microprocessor bus cycle, i.e., the Pod.

The Asynchronous Signature Option takes signatures at UUT test nodes operating at clock speeds up to 20 MHz. For counting events, the number of data transitions appearing at the probe are accumulated up to a total of 16,777,215.

A waveform display feature permits the Troubleshooter to display a representation of the data appearing at the data probe. The waveform feature is useful for determining the time interval between two signal transitions. The waveform displayed shows the last 640 nanoseconds of data received by the probe before the signature-gathering operation is terminated. The display shows logic high, logic low, and tri-state levels.

During troubleshooting operations, the Troubleshooter display notifies the operator of all test conditions and values. The basic functions of the Troubleshooter, in conjunction with a suitable Interface Pod, provide the necessary stimulus for the UUT during signature troubleshooting operations.

All of these features may be accessed while operating the Troubleshooter in the immediate mode by using the keyboard and display. All features may also be accessed by the use of test programs that pass control and test results through registers.

EQUIPMENT DESCRIPTION 1-2.

General 1-3.

As shown in Figure 1-1, the Asynchronous Signature option consists of the Asynchronous Signature Module mounted within the Troubleshooter case, a separate Clock Module that connects to the Troubleshooter, and operating programs contained on a magnetic tape cassette. (For the Model 9020A, programs are executed from within the host computer.)

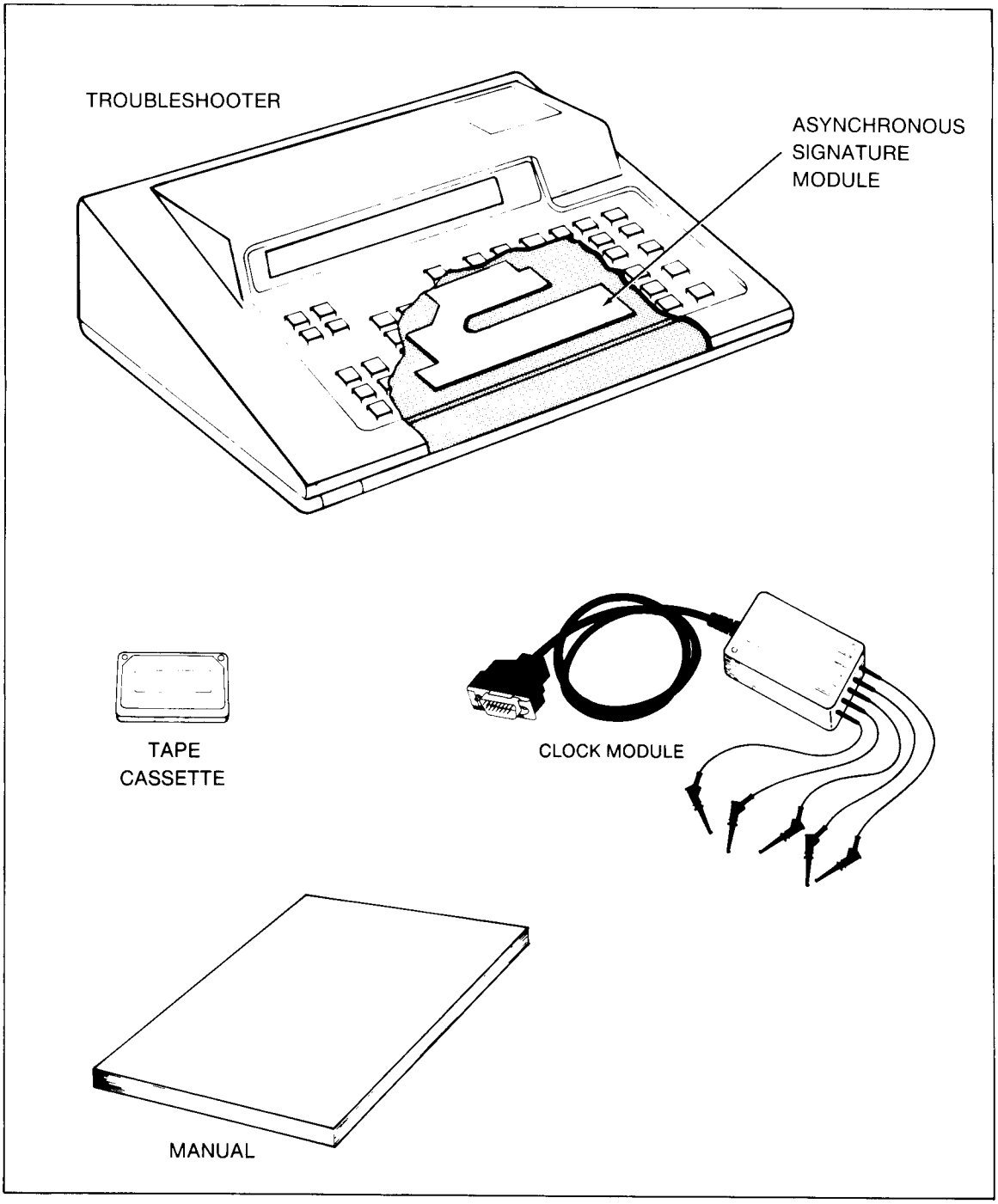


Figure 1-1. Elements of the Asynchronous Signature Option

The Clock Module 1-4.

The Clock Module provides interface and protection between the Troubleshooter and the UUT. Interface is required to effectively connect the sources of the clock, start, stop, and enable signals located on the UUT to the input of the Troubleshooter. A fuse in the ground line provides the necessary protection. An input to the Troubleshooter from the Clock Module provides an indication of the fuse condition.

The Clock Module connects to the Troubleshooter with a 15-pin connector located below the front panel of the Troubleshooter. Connection to the UUT is made by up to five clip leads that protrude from the Clock module. A clip lead is provided for each of the control signal inputs (start, stop, clock, and enable), and one is provided for the ground connection to the UUT.

The Asynchronous Signature Module 1-5.

The Asynchronous Signature Module is a printed circuit board located within the Troubleshooter. It accepts the start, stop, clock, and enable signals from the Clock Module, and the data stream from the Troubleshooter data probe. The Asynchronous Signature Module uses these inputs to generate the corresponding signature, event count, and waveform data. The module sends the calculated signature and event count over the pod bus to the Troubleshooter for display on the front panel.

In addition to the signature and events count functions, a set of registers within the module stores the latest 640 nanoseconds of the data stream gathered by the data probe. The module sends this data to the Troubleshooter for display on the front panel as a waveform.

The Cassette Tape 1-6.

The Asynchronous Signature Option in the models 9005A and 9010A is operated by a series of programs contained on a magnetic tape cassette. Once the programs are loaded into the Troubleshooter RAM, operation of the Troubleshooter in the signature mode is afforded by several front panel keys. Appropriate displays provide the necessary interaction between the Troubleshooter and the operator during signature operations. Operation of the 9020A is a function of the host computer or instrument controller.

ORGANIZATION OF THIS MANUAL 1-7.

This manual documents the Asynchronous Signature Option. The manual provides information for service personnel (Maintenance). Operational and programming procedures for the basic 9000A Series Troubleshooter are documented in the appropriate manual(s).

Note

Information for operating and programming the Asynchronous Signature Probe is available in a separate manual. Order John Fluke Part Number 773259.

SPECIFICATIONS 1-8.

Table 1-1 lists the specifications for the Asynchronous Signature Probe Option.

Table 1-1. Asynchronous Signature Probe Option Specifications

SYNCHRONIZATION AND CONTROL

Start Event:	A selectable positive or negative edge on the Start line, or the Sync signal from the Interface Pod (when used).
Stop Event:	A selectable positive or negative edge on the Stop line, or the Sync signal from the Interface Pod (when used).
Clock Event:	A selectable positive or negative edge, or a combination of both, on the Clock line; or the Sync signal from the Interface Pod (when used).
Enable Event:	A selectable positive or negative level on the Enable line.

ELECTRICAL

Start, Stop, Clock, and Enable lines (through Clock Module):

Impedance:	10 pF/44 kilohms nominal
Threshold:	1.4 volts
Overvoltage:	±15 volts maximum Clock Module ground lead is fuse-protected
Data Channel:	Uses standard data probe supplied with 9000A mainframe

TIMING

Maximum Frequency:

Start, Stop, Clock, and Enable Signals: 20 MHz (50% duty cycle)

Data Signals: 10 MHz (50% duty cycle)

Clock (if stop counter or both-edge modes are used): 10 MHz (50% duty cycle)

Timing Requirements:

Data setup: 20 ns	(Data to be valid at least 20 ns before selected clock edge.)
Data hold: 20 ns	(Data to be valid at least 20 ns after selected clock edge.)
Start/Stop setup: 25 ns	(Start or Stop to be valid at least 25 ns before selected clock edge.)
Enable setup: 20 ns	(Enable to be valid at least 20 ns before selected clock edge.)
Enable hold: 5 ns	(Enable to be valid at least 5 ns after selected clock edge.)

FUNCTIONS

Nodal Signatures:	4-digit algorithm

Table 1-1. Asynchronous Signature Probe Option Specifications (cont)

Transition Counting:	24 bits (0 to 16,777,216 counts)
Waveform Capture:	32 consecutive data samples at 20-nanosecond intervals. High, low, and invalid levels. The 32 samples terminate with the stop event.

SYSTEM COMPATIBILITY

Can be installed in the Fluke 9005A, 9010A, and 9020A mainframes. Cannot be used with 1802 interface pods.

PROGRAM CONTROL

All functions of the Asynchronous Signature Probe Option can be commanded from within a 9010A or 9005A user program. All data measured by this option may be tested in the program. A test program controlling the 9020A may command all option functions and retrieve measured data.

ENVIRONMENTAL

Storage:	-40 to +80 degrees C, RH <75% non-condensing
Operating:	0 to +50 degrees C, RH <75% non-condensing
	0 to +40 degrees C, RH <95% non-condensing

Section 2
Theory of Operation

INTRODUCTION 2-1.

This section contains two block diagram descriptions of the Asynchronous Signature Module housed within the case of the 9000A Series Troubleshooter. The first block diagram description is general; it describes the operating concept of the Signature Module and its relationship to the Troubleshooter and UUT. The second block diagram description covers the module in greater detail.

GENERAL OPERATION 2-2.

The main function of the Signature Module is to receive streams of digital data from the UUT and generate a test result that the Troubleshooter can display as a four-character hexadecimal value (signature). During operation in the signature mode, the Troubleshooter uses the data probe to read the data appearing at the test nodes of the UUT, and it uses the Clock Module to obtain the START, STOP, CLOCK, and ENABLE control signals.

The START, STOP, and ENABLE signals (plus the pod SYNC signal if selected) establish a gate time, and generate CLOCK pulses during the gate time. The START, STOP, and ENABLE signals synchronize the measurement period to the data being read from the UUT by the data probe. The selected START signal specifies the beginning of the signature measurement interval (gate time), which should coincide with the beginning of the test pattern being stimulated within the UUT.

During the measurement interval, the data probe feeds test data through to the data input of the Signature Module, which accepts the data into three separate sections:

1. CRC (signature) section
2. Events section
3. Waveform section

When the selected STOP edge occurs, the gate time concludes, leaving registers in the CRC section loaded with the signature of the clocked-in test data, registers in the events section loaded with the number of selected transitions, and the waveform section registers loaded with a binary representation of the last 640 nanoseconds of probe data. The contents of these three sections are available over the pod bus for display by the Troubleshooter.

Figure 2-1 shows that the Signature Module is connected across the pod bus. Connection to the bus allows the transmission of op codes and data to the module. Connection to the bus also allows the transmission of signature, events count, waveform data, and module status back to the Troubleshooter. The module also uses the handshaking signals (MAINSTAT and PODSTAT) between the Troubleshooter and the Interface Pod.

The Signature Module begins operation when it is selected by the Troubleshooter. To select the Signature Module, the Troubleshooter provides the MAINSTAT signal and sends the module turn-on op code over the pod bus. The control section of the module recognizes the turn-on op code and effectively disconnects the Interface Pod from the pod bus. The Interface Pod remains disconnected from the pod bus until the Troubleshooter releases the Signature Module by means of the turn-off op code.

With the Signature Module selected, the control section receives the op codes from the Troubleshooter and produces the signals necessary to control the various sections of the module shown in Figure 2-1. For example, op codes supplied by the Troubleshooter perform the following operations:

- Place the status of the Signature Module on the pod bus.
- Send control signals to set up the gate section in accordance with the setup selections previously made on the Troubleshooter.
- Clear the gate section, the CRC section, the events section, and the waveform section, then arm the gate section in preparation for the START and STOP signals required to clock in the data from the data probe.
- Place the status of the module on the pod bus during the gate time and when the STOP signal is received.
- Disarm the gate section to prevent further gate action from subsequent START signals.
- Reset (clear) the gate section.
- Send four step commands to shift the signature data (nibble-by-nibble) on the pod bus.
- Send six step commands to shift the event count data (nibble-by-nibble) on the pod bus.
- Send sixteen step commands to shift the waveform data (nibble-by-nibble) on the pod bus.

These Signature Module operations take place when operating the Troubleshooter in the signature gathering mode and when the READ PROBE key is pressed. The control section uses each op code listed in Table 2-1 to perform a specific operation. The overall result of the operations is to take a signature (plus events count and waveform data) and place it on the pod bus where it can be read by the Troubleshooter.

Figure 2-1 shows the relationship of the control section to the other sections of the module (which it controls in response to op codes from the Troubleshooter). Figure 2-1 also shows the control signals from the UUT/and Clock Module and the path of the test data from the data probe.

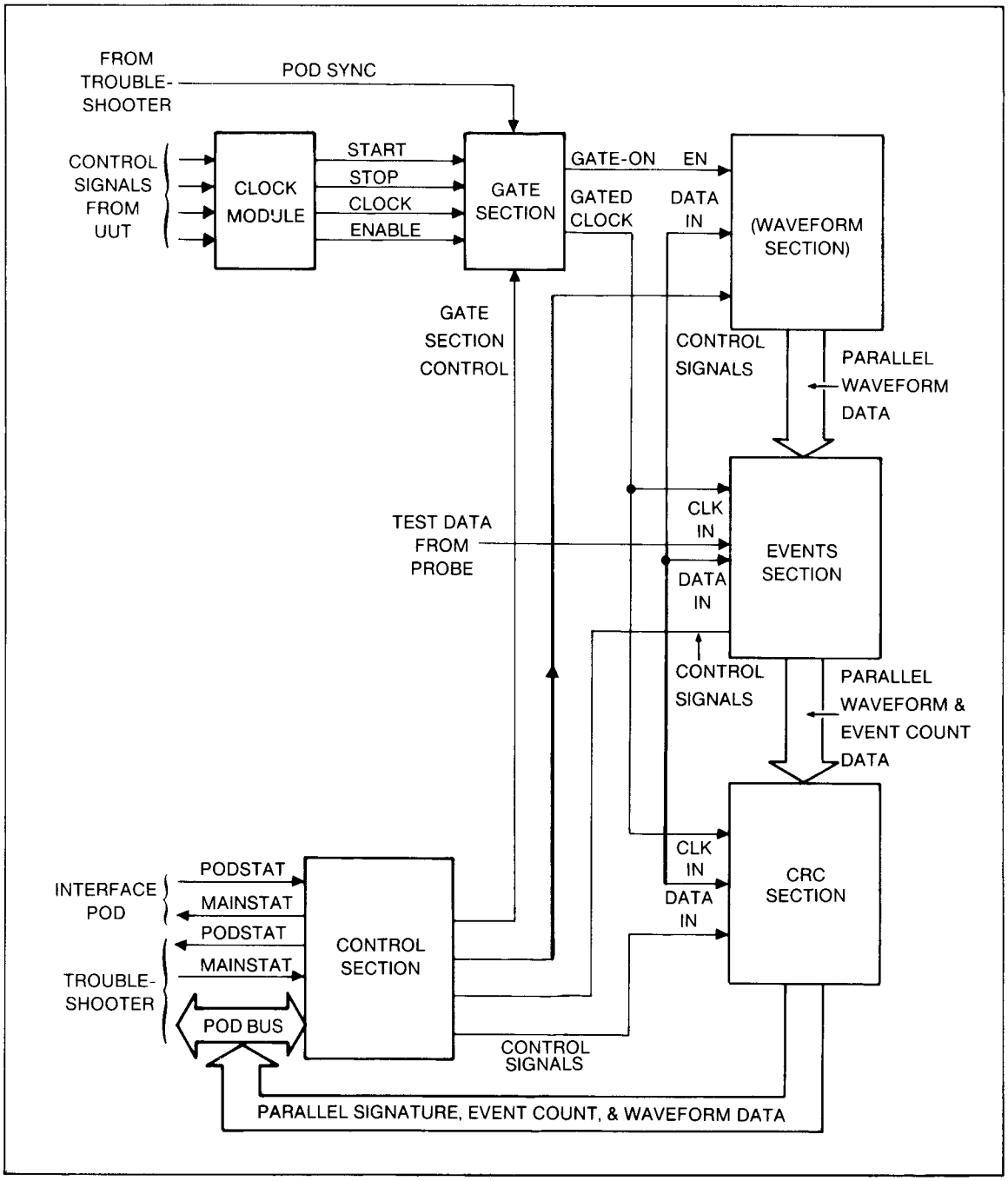


Figure 2-1. Signature Module, General Block Diagram

The START, STOP, CLOCK, and ENABLE signals from the UUT are conditioned by the Clock Module and applied to the gate section of the module. The gate section also accepts the pod SYNC signal (produced by the Interface Pod) as a control signal. The main function of the gate section is to provide gated CLOCK signals to the CRC and events registers. The source of the CLOCK signals may be the clock lead of the Clock Module, or the pod SYNC signal, depending upon the selection made during the setup of the Troubleshooter for signature operation. The control section causes the gate section to select the correct source of the CLOCK signal in response to op codes sent by the Troubleshooter.

Table 2-1. Signature Module Op Codes

OP CODE	FUNCTION
00	Turn on the Signature Module to the pod bus (precede with delay)
10	ENABLE signal to be from Clock Module
11	ENABLE signal to be held in the high (enabled) state
12	CLOCK signal to be from UUT via Clock Module CLOCK lead
13	CLOCK signal to be SYNC signal from Interface Pod
14	START signal to be from UUT via Clock Module START lead
15	START signal to be SYNC signal from Interface Pod
16	STOP signal to be from UUT via Clock Module STOP lead
17	STOP signal to be SYNC signal from Interface Pod
18	ENABLE signal level to be valid high
19	ENABLE signal level to be valid low
1A	CLOCK signal, select rising edge (overridden by op code 30)
1B	CLOCK signal, select falling edge (overridden by op code 30)
1C	START signal, select rising edge
1D	START signal, select falling edge
1E	STOP signal, select rising edge
1F	STOP signal, select falling edge
28	Disarm (causes the module to ignore START signals)
29	Arm (cause the module to act on START signals)
2A	Disable the stop-on-count function (stops on no. of gated CLOCK)
2B	Enable the stop-on-count function
2C	Event count from start to stop
2D	Event count continuously
2F	Initialize event counter
30	CLOCK signal, select both edges
40	CLOCK signal, permit the selection of op codes 1A and 1B
5x	Load stop-on-count value, where x is the least-significant nibble
6x	Load stop-on-count value, where x is the intermediate nibble
7x	Load stop-on-count value, where x is the most-significant nibble
80	Notify the module that the next operation will be a read
90	Shift all registers (next data nibble to the output buffer)
B0	Clear the signature register (prepare for next gate time)
C0	Clear the events counter
D0	Clear the waveform register
E0	Clear the gate section (prepare for next gate time)
F0	Turn off the Signature Module from the pod bus

The gate time (during which the gate section produces the gated CLOCK signals) begins with the selected START signal and ends with the selected STOP signal. The source of the START signal may be the corresponding lead of the Clock Module (i.e., the UUT) or the pod SYNC signal. The source of the STOP signal may the corresponding lead of the Clock Module or the SYNC signal from the interface pod. Selection of the START and STOP signals is a function of control lines from the control section, which in turn are a result of op codes sent by the Troubleshooter.

The CRC section generates the 16-bit signature by using the gated CLOCK pulses to receive the UUT data fed to the module by the data probe. In the absence of the gated CLOCK signals, the CRC section ignores data from the data probe. The four-bit parallel output of the CRC section is available to the pod bus (via a transmit buffer)

but is not placed on the bus until commanded to do so by the Troubleshooter. Since only four bits of signature data are placed on the pod bus at a time, four read operations are required by the Troubleshooter to shift all four characters of signature data through the CRC section and onto the bus.

The events section generates a 24-bit (six hex-digit) count of events (transitions) that take place in the test data input. Events counting is selected to take place only during the gate-time, or continuously (free-running mode). Control lines from the control section select the signal source to be counted and determine whether to count on a continuous basis or only during the time of the gated signals. The output of the events section is applied in four-bit parallel form to a parallel load input of the CRC section. As the Troubleshooter reads the signature from the CRC section, the event section is pulsed to shift its contents into the CRC section behind the CRC data being shifted onto the pod bus. To read the entire contents of the event section over the pod bus, the Troubleshooter performs six more read operations subsequent to the four used to transfer the signature data.

The waveform register receives the serial data fed from the UUT and loads it serially into a 32-bit shift register. The operation of the shift register is such that it always contains a binary representation of the last 640 nanoseconds of test data fed from the probe. This test data can be displayed on the Troubleshooter as a waveform.

The output of the shift register is 4 bits (one nibble) wide, and is available to the Troubleshooter via the events section, the CRC section, and the pod bus. To read the contents of the shift register for display, the Troubleshooter first reads the CRC and event sections. It then commands the control section to issue the necessary shift commands to place each nibble of waveform data on the pod bus. Once the Troubleshooter has read the contents of the waveform section, it can display a representative waveform of the last 640 nanoseconds of probe data.

DETAILED BLOCK DIAGRAM DESCRIPTION 2-3.

Clock Module 2-4.

The primary function of the clock module is to buffer the UUT control signals. Clock module circuitry consists of four analog comparators, one for each of the start, stop, clock, and enable signals. The input of each comparator is compared to a 1.4V reference. Hysteresis is applied to each channel to help reject noise.

Control Section 2-5.

The main functions of the control section are as follows:

- Recognize the turn-on op code from the Troubleshooter.
- Prevent the Interface Pod from receiving the MAINSTAT signal after the turn-on op code and before the turn-off op code have been received.
- Decode the op codes sent by the Troubleshooter over the pod bus and generate the corresponding control signals to the gate, CRC, events, and waveform sections.

Figure 2-2 shows the main elements of the control section, with the Troubleshooter/ Interface Pod connections on the left side and the connections to the remainder of the module on the right side. During operation, the Troubleshooter addresses both the Interface Pod and the Signature Module as required to fulfill testing requirements.

The Interface Pod and the Signature Module are both connected to the same I/O port of the Troubleshooter, and the Signature Module examines each op code placed on the pod bus (by the Troubleshooter) to determine if the Signature Module should turn on or if the Interface Pod should be allowed to respond.

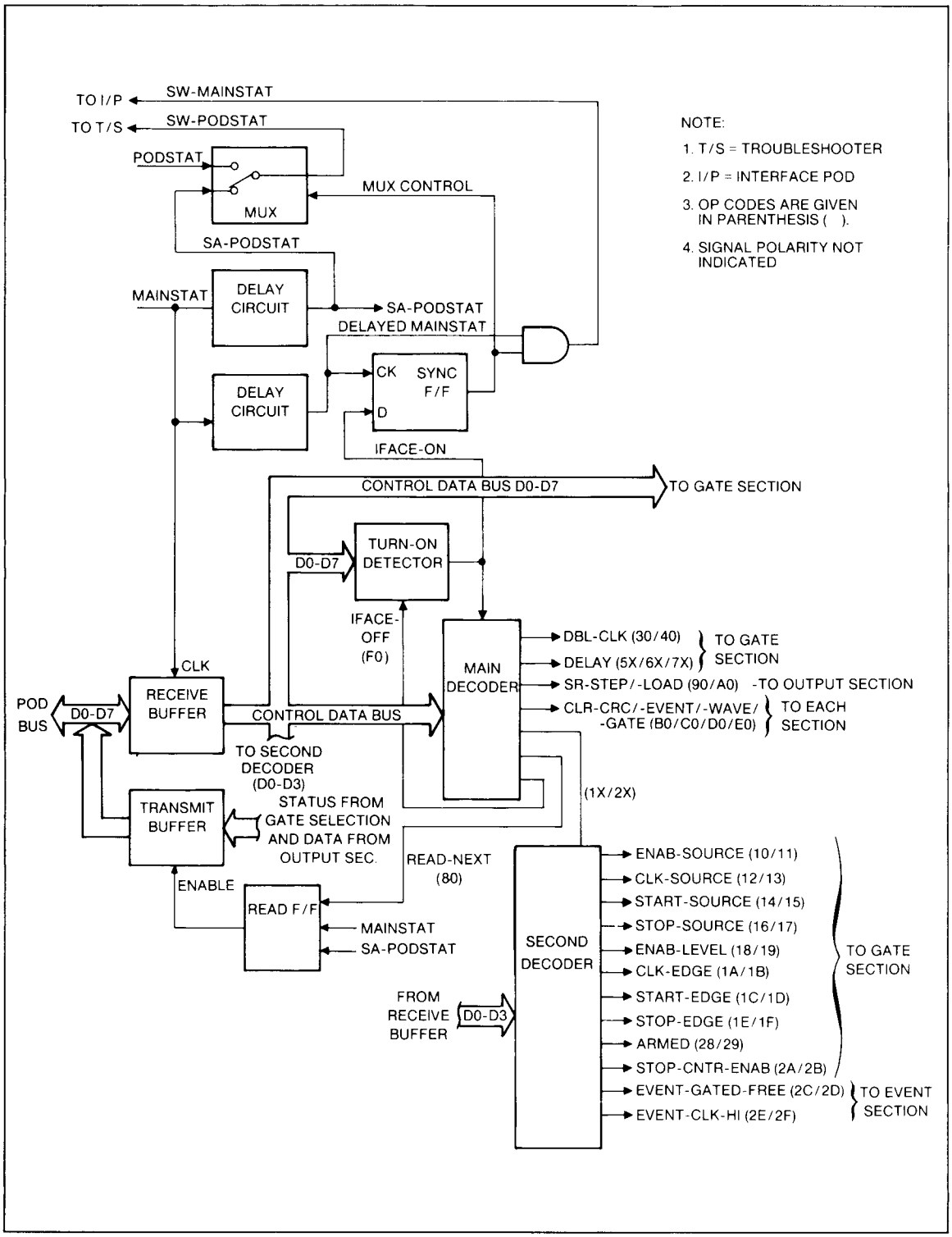


Figure 2-2. Control Section Block Diagam

When the Troubleshooter places a command (op code) on the pod bus destined for the Interface Pod, it pulls the MAINSTAT signal low. The MAINSTAT signal is fed through delay circuit U29/U52 and gate U37 out to the interface pod as the SW-MAINSTAT signal. The delay circuit allows time for the turn-on detector to examine the op code placed on the pod bus to determine whether or not it is a 00H, the Signature Module turn-on op code. Since operation of the pod is asynchronous to the Troubleshooter, the delay provided by U29/U52 is transparent to the pod (i.e., it does not affect pod operation). The PODSTAT signal, required by the Troubleshooter software for handshaking purposes, is routed back from the Interface Pod, through the multiplexer (U52) to the Troubleshooter as the SW-PODSTAT signal.

When the Troubleshooter addresses the Signature Module, it places the turn-on op code (00H) on the pod bus and pulls the MAINSTAT line low. The MAINSTAT signal clocks the receive buffer (U4), applying the op code to the turn-on detector (U7, U16, and U33). The output of the detector enables the main decoder (U18 and U17) and also sets the SYNC flip-flop (U6) to prevent the MAINSTAT signal from reaching the Interface Pod. (If the MAINSTAT signal was allowed to reach the Interface Pod, it would also read the op codes placed on the pod bus for the Signature Module.)

The output of the SYNC flip-flop (U6) also controls the PODSTAT signal multiplexer (U52). When the SYNC flip-flop is set, the multiplexer (U52) is switched so that the PODSTAT signal required by the Troubleshooter software is provided by simply delaying the MAINSTAT signal. The PODSTAT signal is a requirement of Troubleshooter/Interface Pod handshaking, and the synthesized PODSTAT signal sent as a result of delaying the MAINSTAT signal satisfies these requirements.

With the main decoder (U18, U17) enabled, each op code placed on the pod bus by the Troubleshooter and latched (clocked) into the receive buffer (U4) is decoded to a specific Signature Module function. Two of the decoded functions (op codes 1x and 2x) enable the second decoder (U11 and U12). That is, whenever an op code is received that has 1H or 2H as the high nibble, the second decoder latches an output that corresponds to the low nibble. For example, op code 12H sets the CLK-SOURCE line low, while op code 13H sets the same line high. The CLK-SOURCE line is used within the gate section to select the source of the CLOCK signal between the Clock Module and the pod sync signals.

When the Troubleshooter issues a read-next op code (80H) to the control section, the main decoder (U18, U17) enables the transmit buffer (U3) by the read flip-flop (U13 and U16). The function of the read flip-flop is to enable the transmit buffer at the time required by the Troubleshooter software. The transmit buffer is enabled after receipt of the next MAINSTAT signal from the Troubleshooter, and at the time of the SA-PODSTAT signal (delayed MAINSTAT signal).

As long as the main decoder (U18 and U17) does not receive the turn-off op code (F0H) from the Troubleshooter, the second decoder continues to decode the received op codes into specific commands to control the gate, CRC, events, and waveform sections of the module. However, when the Troubleshooter places the turn-off op code (F0H) on the pod bus, the main decoder generates the IFACE-OFF signal. The IFACE-OFF signal resets the SYNC flip-flop (U6). The next MAINSTAT signal causes U47 to change state, allowing the MAINSTAT signal to pass through to the Interface Pod and the PODSTAT signal to pass from the Interface Pod to the Troubleshooter. Under these conditions, communication is restored between the Troubleshooter and the Interface Pod.

Gate Section 2-6.

The main function of the gate section is to provide gated CLOCK pulses, using the START, STOP, CLOCK, ENABLE, and pod SYNC signals, as selected by the operator of the Troubleshooter. The gated CLOCK signals are required by the CRC section to clock in the data appearing at the data probe and to calculate the signature of the data occurring during the gate time. (The gate time is that period between the first selected START edge and the first STOP edge.) The gate section also provides an output (GATE-ON) to the events section so that events can be counted during the gate time (when not operated in the free-running mode).

When the setup of the Troubleshooter is performed (see Section 3), selections regarding the control (START, STOP, CLOCK, and ENABLE) signals are made and stored within the Troubleshooter. When the operator presses the READ PROBE key to read a signature, events count, or waveform, the Troubleshooter sends the control signal selections made during setup to the Signature Module. The setup selections are sent as op codes, decoded within the control section and applied to the gate section as individual control lines.

Figure 2-3 shows each of the control lines from the control section, plus the control signals themselves from the Clock Module and Interface Pod (pod SYNC). The control signal source selector (U34 and U35) permits selection of the source for the START, STOP, CLOCK, and ENABLE signals. The source for the START signal may be the start lead of the Clock Module (EXT-START) or the pod SYNC signal. The source for the STOP signal may be either the stop lead (EXT-STOP) or the SYNC signal from the Interface Pod. The source for the CLOCK signal may be the clock lead (EXT-CLOCK) of the Clock Module or the pod SYNC signal. The source for the ENABLE signal may be the enable lead (EXT-ENAB) of the Clock pod or the logic high (always enabled).

The control signal sources are selected by the four control lines designated START-SOURCE, STOP-SOURCE, ENAB-SOURCE, and CLOCK-SOURCE from the control section. The four control lines reflect the op codes sent by the Troubleshooter to initialize the Signature Module prior to taking a signature, and cause the selector (U34 and U35) to connect the appropriate signal source through to its output. At the output, the selected control signals are applied to the control signal edge selector.

The edge selector (U36) allows selection of the rising or falling edge of each of the selected control signals. (The ENABLE signal is selected as a level since it is not edge-sensitive.) The edges are selected by the control lines designated START-EDGE, STOP-EDGE, CLK-EDGE, DBL-CLK, and ENAB-LEVEL.

The CLK-EDGE and DBL-CLK control lines are applied to selector U25 along with the SELECTED-CLK signal. Selector U25 causes U36 to output CLOCK pulses at a rate of one per selected edge, or one per edge (both edges), depending on the control lines from the control section. In the one-per edge mode, the selected CLOCK signal is doubled, since a CLOCK pulse is provided at the output of U36 for each CLOCK signal edge, both rising and falling.

Operation of the gate section from this point is such that when a selected START edge occurs, the start flip-flop (U48A) is clocked. If the start flip-flop was previously armed (by the ARMED control line and the arm op code), it changes state to produce the START-RECVD signal. The START-RECVD signal is fed to the enable gate (U49), to the stop flip/flop (U48B), and back to the control section as a status line to the

Troubleshooter. Assuming no STOP edge has yet been received, and assuming the enable level is in the enabled state, the enable gate (U49) provides a GATE-ON signal to the clock gate (U24 and U23) (and to the events and waveform sections).

At the time of the first CLOCK pulse after the START signal edge, the clock gate produces its first gated CLOCK pulse to the CRC and events sections. The CLOCK pulse is a result of the edged CLOCK signal applied to the clock gate. The clock gate remains enabled until the selected STOP signal occurs and the stop flip-flop (U48B) changes state to inhibit the enable gate (U49). The enable gate inhibits the clock gate and halts the generation of gated CLOCK pulses. The output of the stop flip-flop is also fed to the control section as a status line back to the Troubleshooter.

Once the STOP edge has been received and the stop flip-flop is set, the control section must produce a CLEAR-GATE signal. The CLEAR-GATE signal is required for the next START edge to set the start flip-flop and begin a new gate time.

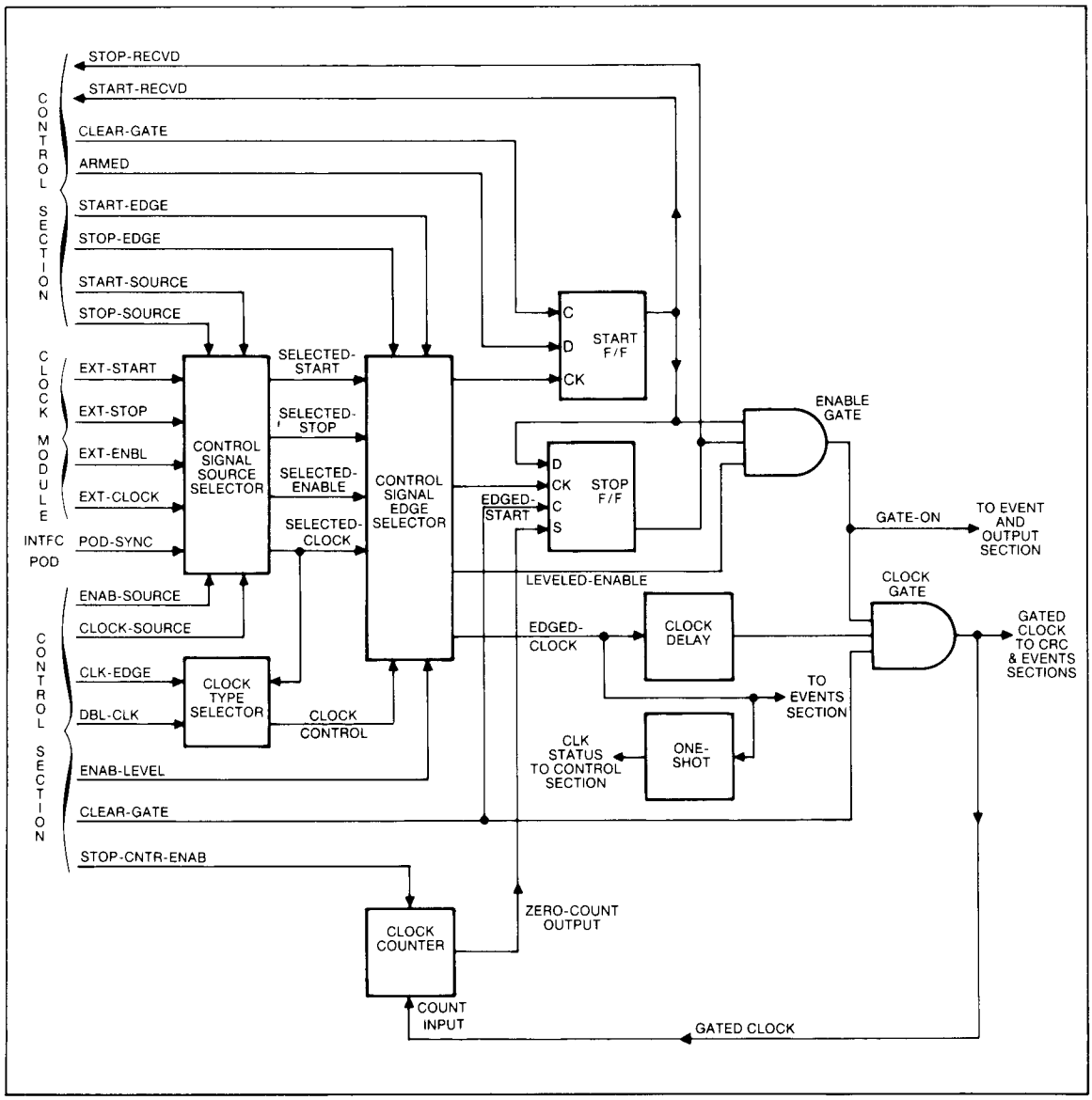


Figure 2-3. Gate Selection, Block Diagram

Clock counter (U20A, U8, U9, U10) creates a STOP edge after a certain number of gated CLOCK pulses. This feature allows selection of a gate time that is equivalent to a specified number of gated clock pulses. The clock counter receives the gated CLOCK pulses fed to the CRC and events sections and decrements from a preset (at the time of initialization) count. When the counter reaches zero, it generates a zero-count output to set the stop flip-flop (U48B) and immediately inhibit the generation of gated CLOCK pulses.

CRC Section 2-7.

The CRC section receives the gated CLOCK pulses from the gate section and the delayed data (high and low) from the delay section and generates the hexadecimal signature of the data through a cyclic redundancy check. As shown in Figure 2-4, the delayed data from the probe is applied through a feedback gating circuit to a 16-bit shift register. The shift register consists of four 4-bit registers, U63 through U66. Each register has serial and 4-bit parallel inputs and outputs, where the output of the first is connected to the input of the second, etc. This arrangement allows data to be shifted through the registers in either serial or four-bit parallel fashion. The four-bit parallel output of the fourth register is fed to the transmit buffer, U3, located in the control section.

Since the CRC register has both parallel and serial inputs/outputs, it can be operated in both parallel and serial modes. When a read probe operation is in progress, the gated CLOCK signal operates the register in the serial mode. In the serial mode, high and low data is applied to the serial input of the first of the four registers and carries through to the fourth as gated CLOCK signals occur. To provide the CRC action of the register, four outputs are taken from the registers. These outputs are fed through exclusive-or gates and clocked through pipeline registers back to the feedback gating circuit formed by U21, U25, and U20.

The feedback gating is necessary to achieve the standard CRC signature result from the probe data and gated CLOCK pulses. The pipeline registers permit the CRC section to operate at a higher speed than that possible with the exclusive-or gates alone.

To handle invalid probe data levels (both VALID-HI and VALID-LOW signals at a low level), a last level register (2D input of U22) is used to store the last valid data level and apply it to the feedback gating. This feature prevents the CRC register from attempting to generate a signature using invalid data. Each register in the CRC section is cleared by the CLR-CRC signal from the control section.

The CRC register also operates in the parallel mode. This mode is used at the end of the signature computation to shift the accumulated signature, four bits (nibble) at a time, onto the pod bus via the transmit buffer. Four shift (load) operations are used to place the four nibbles of signature data on the pod bus. As each shift operation takes place, the parallel output of the events section (EVT-20 through EVT-23) is shifted into and through the CRC register. The CRC register provides the path for the event count and waveform data to reach the transmit buffer and pod bus.

The four-bit output of the last CRC register is fed to the input of the transmit buffer (U3) located in the control section. When the Troubleshooter issues a read-next op code (80H) to the control section, the main decoder enables the transmit buffer. Since the transmit buffer contains the output of the last CRC register, the output of the last CRC register is placed on the pod bus to the Troubleshooter.

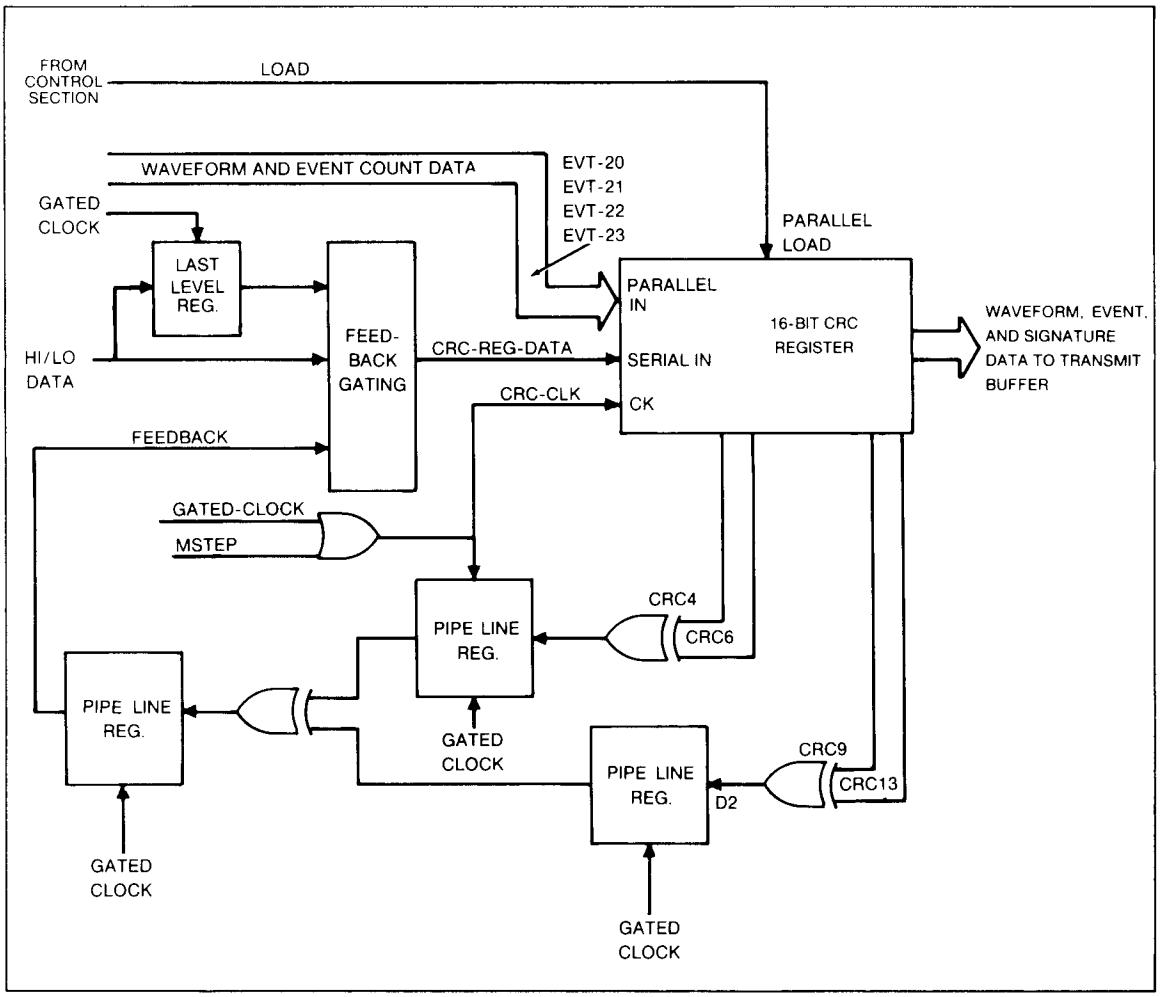


Figure 2-4. CRC Section, Block Diagram

Events Section 2-8.

The events section contains a 24-bit binary counter that consists of six 4-bit registers, U57 through U62. Each register has four-bit parallel inputs and outputs, where the output of the first is connected to the input of the second, etc. As in the CRC register, this arrangement allows data to be shifted through the registers in four-bit parallel fashion. The four-bit parallel output of the sixth register is fed to the parallel input of the CRC register, providing a means for the event count data to be shifted through to the transmit buffer, U3, located in the control section.

As shown in Figure 2-5, the input to the counter is selected from GATED-CLK, EDGED-CLK, GATED-HI, or VALID-HI by 1-of-4 selector, U19. The selected input to the counter is determined by the EVENT-GATED-FREE and EVENT-CLK-HI signals from the control section. The EVENT-GATED-FREE signal causes U19 to select between EDGED-CLK or VALID-HI and GATED-CLK or GATED-HI. The EVENT-CLK-HI signal causes U19 to select between GATED-CLK or EDGED-CLK and GATED-HI or VALID-HI.

The events counter, U57 through U62, counts up using the selected input to clock the first stage.

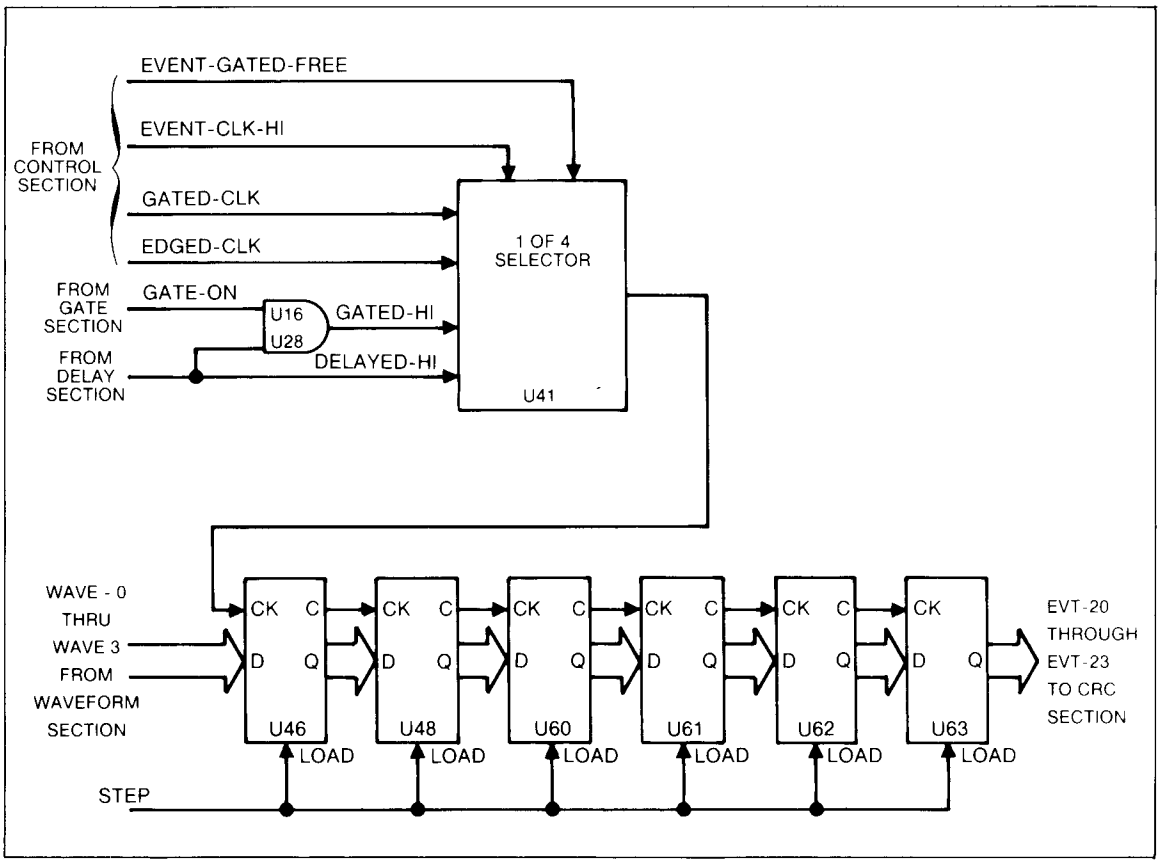


Figure 2-5. Events Section, Block Diagram

Waveform Section 2-9.

The function of the waveform section is to read the probe data on a continuous basis so that it always contains the last 640 nanoseconds of probe data in a binary form. Figure 2-6 shows that the waveform section consists of four 16-bit shift registers, each made up of two 8-bit shift registers connected in series. (Hereafter in this description, the term shift register refers to one of the 16-bit registers, such as that formed by U14 and U15.) One shift register (U14 and U15) receives VALID-HI data from the probe and the PHASE1 signal from the GATED-OSC signal and U42. A second shift register (U40 and U41) receives VALID-HI data and the PHASE2 signal.

These two registers both receive high-level data samples (registers U27, U28, U55, and U56 receive low-level data samples) but are clocked 180 degrees out of phase and 20 nanoseconds apart. The effect of this parallel, but out-of-phase, register arrangement is a doubling of the effective operating speed. That is, the data can be clocked at double the 25 MHz speed of the registers since each register is clocked at the clock speed, but 180 degrees apart.

Since the two registers operate 180 degrees apart, they effectively appear as a single 32-bit register to the incoming high data (or the incoming low data in the case of U27, U28, U55, and U56). As a result, the two registers together always contain a binary representation of valid high conditions at the data probe for the last 640 nanoseconds (32 times 20 nanoseconds). The other two registers (U27, U28, U55, and U56) receive valid low data from the data probe and operate in a manner similar to that described for U14, U15, U40, and U41 to clock in valid low probe data.

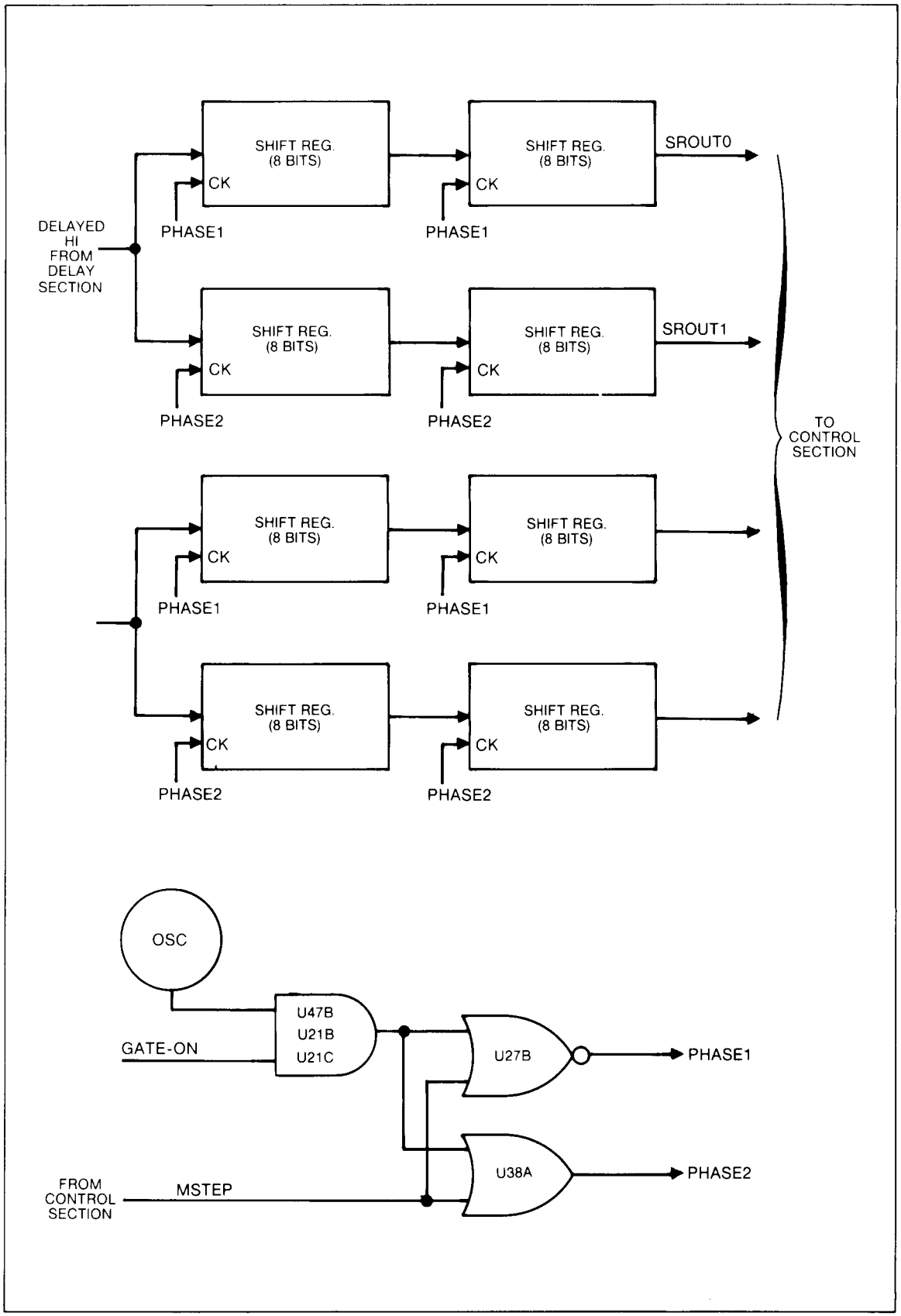


Figure 2-6. Waveform Section, Block Diagam

At the end of a read probe operation (at the end of the gate time), the signature module transmits the waveform data to the Troubleshooter by first halting the 25 MHz shifting action of the registers. With the registers halted, the serial outputs of the four registers apply the oldest nibble of waveform data to the parallel input of the event counter. Each time the Troubleshooter executes the step command (op code 90H), the control section generates the MSTEP signal to shift the waveform registers, the event count registers, and the CRC registers.

By shifting the registers with the MSTEP signal, the waveform data passes through the event count and CRC registers to the transmit buffer. When the Troubleshooter executes a next read command (op code 80H), the data appearing at the input of the transmit buffer is latched into the buffer and placed on the pod bus. To shift the entire contents of all registers onto the pod bus, 26 shift (step) operations are required: four for the CRC register contents, six for the event count register contents, and 16 for the waveform register contents.

Section 3
Maintenance

INTRODUCTION 3-1.

This section provides maintenance information for the Asynchronous Signature Module and includes a performance test, repair precautions, disassembly procedures, and troubleshooting information.

REQUIRED PERFORMANCE TEST EQUIPMENT 3-2.

The equipment required for the performance test and troubleshooting procedures contained in this section are listed in Table 3-1.

Table 3-1. Required Test Equipment

EQUIPMENT TYPE	RECOMMENDED EQUIPMENT
Microsystem Troubleshooter with with Signature Option	Fluke 9010A with 006 option
Oscilloscope	Tektronix 7904
Multimeter	Fluke 8050A
40-Pin DIP Test Clip	
Patch Cable, Micrograbber	

REPAIR PRECAUTIONS 3-3.

SMD Considerations 3-4.

The Asynchronous Signature Module employs SMD (surface mount device) technology for mounting the components on the printed circuit board. The use of surface mount devices prevents the use of conventional desoldering and soldering techniques during repair operations. The removal and installation of surface mount devices requires the correct use of a heat gun and fluxing techniques. Do not attempt printed circuit board repair unless you are skilled in SMD repair techniques.

MOS Considerations 3-5.

CAUTION

Static discharge can damage MOS components contained on the module. To prevent this possibility, take the following precautions when troubleshooting and/or repairing the module.

- Perform all repairs at a static-free work station.
- Do not handle the contact points of the SMDs.
- Attach grounding straps to repair personnel.
- Remove all plastic, vinyl, and styrofoam from the work area.

DISASSEMBLY PROCEDURE 3-6.

The Asynchronous Signature Module is located within the Troubleshooter case. Gain access to and remove the module as follows:

1. Invert the instrument on a clean surface, and remove the seven retaining screws from the bottom side.
2. Carefully return the instrument to the upright position while holding the top cover in place. Once the instrument is in the upright position, remove the top cover and lay it to the right side of the instrument, exposing the Signature Module as shown in Figure 3-1.
3. If it is necessary to remove the module from the base assembly of the Troubleshooter, proceed as follows:
   a. Remove the three screws that secure the Signature Module PCB assembly within the Troubleshooter.
   b. Lift out the module and disconnect the four ribbon cables that extend from the module to the main assembly of the Troubleshooter.

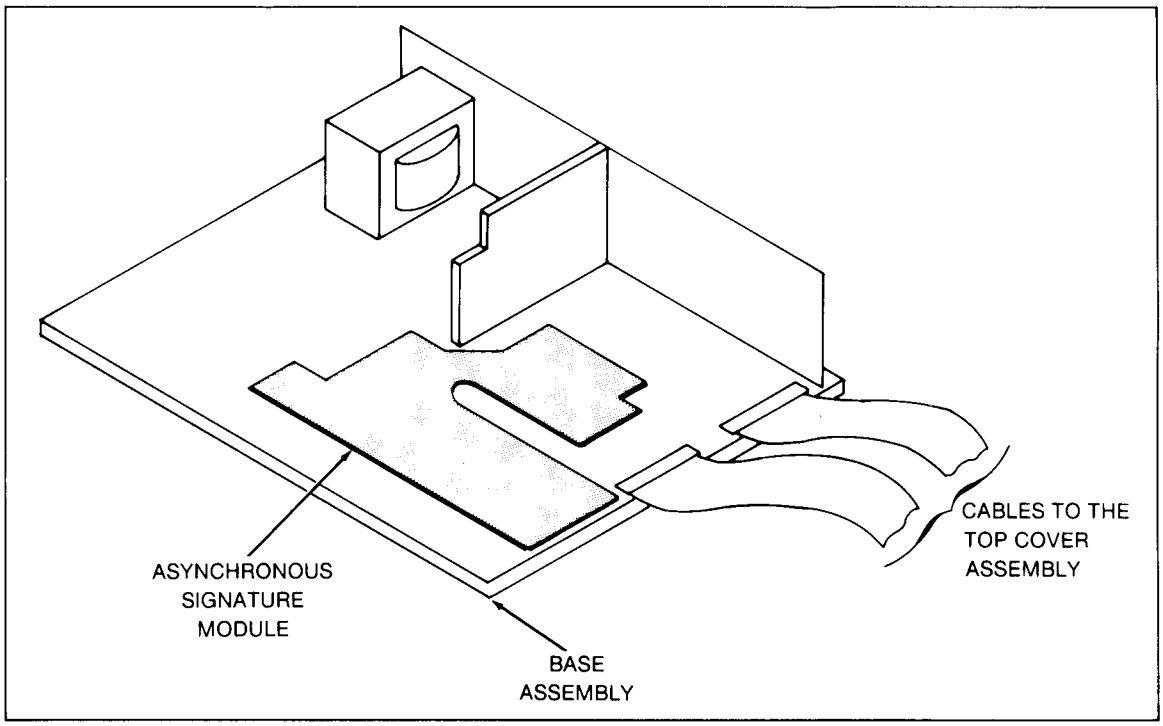


Figure 3-1. Location of Asynchronous Signature Module

PRELIMINARY TROUBLESHOOTING 3-7.

Introduction 3-8.

The following paragraphs provide information to aid in the troubleshooting of the Signature Module. The troubleshooting information is provided in descriptive form followed by tables of signatures for selected test nodes on the module. Since the Interface Pod depends on the Signature Module for the passage of the MAINSTAT and PODSTAT signals that are necessary for Pod/Troubleshooter handshaking and communication, it is first necessary to verify that the Interface Pod is not faulty. Also, since the Signature Module depends on normal operation of the Troubleshooter, it is necessary to verify that the Troubleshooter is not defective.

Once you have determined that a fault exists within the Signature Module, you can begin troubleshooting the module. Troubleshooting the signature module involves verifying signatures at designated test nodes.

Module or Troubleshooter Faulty? 3-9.

The first step in troubleshooting the Signature Module is to determine that the module is defective, not the Troubleshooter. You can make a quick check of Signature Module operation by performing the equipment verification procedure contained in Section 2 of the Operation Manual. If the module fails the functional test, but the Troubleshooter operates satisfactorily when it is used with the Interface Pod, then the Signature Module is defective.

Module or Interface Pod Faulty? 3-10.

Although the Signature Module does not depend upon the Interface Pod for its operation, the opposite is true. The Interface Pod depends on the Signature Module for the passage of handshaking signals (MAINSTAT and PODSTAT) and data between itself and the Troubleshooter. Because the signature module is electrically inserted in the handshaking/data path to the Interface Pod, there is a failure mode of the Signature Module that can render a good Interface Pod non-operational.

The failure mode occurs when the control section in the signature module prevents proper generation and gating of the MAINSTAT and PODSTAT signals to and from the Interface Pod. The failure may also interrupt the passage of data. The easiest way to verify that a particular Interface Pod is operational, and not just being interfered with by the Signature Module, is to use the pod with a known-good Troubleshooter to perform the pod self-test or some similar operation. If a successful pod self-test is possible with the known-good Troubleshooter, then the problem lies in the Signature Module or possibly in the Troubleshooter.

If the control section of the Signature Module is suspect (due to apparent failure of the Interface Pod) and a second Troubleshooter is not available for pod verification, it is possible to temporarily disconnect and bypass the Signature Module, then check operation of the Interface Pod. If the Interface Pod operates normally with the Signature Module disconnected, the control section of the module is defective. To bypass the Signature Module, refer to Disconnecting the Signature Module.

Disconnecting the Signature Module 3-11.

Disconnection of the Signature Module may be performed whenever it is necessary to remove it from the Troubleshooter/Interface Pod data and handshaking signal path. To disconnect the Signature Module, perform steps 1 through 3a of the Disassembly

Procedure, but only disconnect the largest of the four ribbon cables from the Troubleshooter main pcb assembly and the Signature Module. Install an SYP 6520 PIA (part number 536318) in the vacant socket to allow bypassed communication between the Troubleshooter and the Interface Pod.

NOTE

This type of PIA exists on the Signature Module; however, moving the PIA to the main pcb allows the possibility of moving the problem from the Signature Module to the main pcb of the Troubleshooter.

With the Signature Module removed from the data/handshaking signal path of the Interface Pod, normal pod operation should be restored. Verify pod operation by performing a pod self-test or any other test that prompted disconnection of the Signature Module. If the Interface Pod operation now appears normal, the problem exists in the control section of the signature module.

A key device in the control section is the PIA (U2). Verify operation of U2 by removing it (power off) and using it to replace the PIA previously installed in the connector socket on the main pcb assembly. With the PIA from the Signature Module installed on the main pcb assembly, repeat the test performed in the previous paragraph. If the test fails, the PIA is defective. But, if the test does not fail, it probably is good, although the test results are inconclusive. To verify operation of the PIA, replace it in the Signature Module and proceed to Signature Troubleshooting Procedures.

SIGNATURE TROUBLESHOOTING PROCEDURES 3-12.

Getting Started 3-13.

The most efficient method of locating faults within the Signature Module is to employ a second Troubleshooter, hereafter referred to as the test Troubleshooter, equipped with the Asynchronous Signature Option to read signatures at various points on the module. During the signature reading operation, the Troubleshooter in which the defective module is installed is used to stimulate the module with programs 1 and 2 supplied on side B of the cassette tape.

The valid signatures with the corresponding test nodes are listed in tables in Section 5, along with the schematics. Table 5-1 contains signatures for the control and gate sections (defined in Section 2, Theory of Operation) of the defective module when program 1 is running. Table 5-2 contains valid signatures for the signature, events, and waveform sections (also defined in Section 2, Theory of Operation) when program 2 is running.

Signatures are not provided for every possible test node on the module, but signatures are given for particular nodes in each functional section. When you find an invalid signature, trouble is indicated in that section, and you can perform further testing with the aid of an oscilloscope, the schematic diagram, and the Theory of Operation section.

Stimulation of the defective Signature Module (UUT) requires that its five Clock Module leads and Data Probe are properly connected. The connections allow the Signature Module to respond to the test stimulus. The connections listed first allow the defective module to receive the control and data signals necessary to stimulate gate and control sections of the defective module.

After the control and gate sections have been verified as operating normally, the connections are changed to allow the defective module to receive the control and data signals necessary to stimulate the signature, events, and output sections of the defective module.

How the Stimulus Programs Work 3-14.

The first stimulus program (number 1) running in the 9000A with the suspected defective option operates as follows:

wait 200 milliseconds
send opcode 00
send opcode 40
.
(many different opcodes)
.
send opcode E0
send opcode F0
bring PIA pin 19 low
bring PIA pin 19 high
(use of the LOOP key repeats the program)

MAINSTAT is brought low and then high as each opcode is sent. This signal is present on pin 2 of the PIA and is used as the clock for the tester 9000A's signature option. As the stimulus program is repeated, bringing the PIA's pin 19 low stops the current signature cycle and bringing it high starts the next one.

The suspected defective option's clock module is stimulated at the pod-bus. As the various opcode bytes are sent, different logic levels are applied to the clock module's inputs. These levels can be traced through the clock module and the gate section and measured as signatures. Meanwhile, the same opcodes are latched and decoded by the control section to generate additional logic waveforms which can also be measured as signatures.

The second stimulus program (number 2) running in the 9000A with the suspected defective option operates as follows:

The data shift path is repeatedly stepped by the opcode 9X. The data probe is placed on the pod-bus data bit 0 and is stimulated by using 91 and 90 for the 9X opcodes. The highs and lows to the probe tip are decoded by the mainframe and sent to the signature option's data delay section as the signals VALID-HI and VALID-LO. The signals are clocked from the delay section into the waveform capture register and through the data shift path. It is these signals which the tester troubleshooter measures as signatures.

Test Setup, Defective Unit (UUT) 3-15.

Proceed with the test setup for the defective Signature Module as follows:

1. Be sure to disconnect any Interface Pod from the Troubleshooter containing the defective module. Also, be sure that no powered UUT is connected to the unpowered Interface Pod removed from the Troubleshooter, since an unpowered pod is vulnerable to external voltages. Refer to the Interface Pod manual for further details.

2. With power off, connect a 40-pin DIP clip on U2 (6520 PIA) of the Signature Module.

3. Connect the leads of the Clock Module to the pins of the 40-pin DIP clip as listed in Table 3-2. The 40-pin DIP clip provides easy access to the pins of U2.

4. Connect a micrograbber patch cable from pin 14 of the 40-pin DIP clip to pin 3 of U37 mounted on the main PCB of the Troubleshooter.

5. Disconnect the data probe from the Troubleshooter.

6. Load and run stimulus program 1 on side B in the Troubleshooter with the defective module. Press the LOOP key to continuously repeat the program.

When the above steps are completed, proceed with Taking Signatures with the Test Troubleshooter.

Table 3-2. UUT Test Setup, Control/Gate Sections

CLOCK MODULE LEAD	CONNECTS TO U2 PIN NO.
Start	10
Stop	11
Clock	12
Enable	13
Ground	1

Taking Signatures with the Test Troubleshooter 3-16.

Taking signatures at various test nodes of the defective module (the UUT in this case) requires completion of the following steps:

1. Connect the Clock Module leads of the test Troubleshooter to the 40-pin DIP clip on the defective module as listed in Table 3-3.

Table 3-3. Test Troubleshooter Connections

CLOCK MODULE LEAD	CONNECTS TO U2 PIN NO.
Start	19
Stop	19
Clock	2
Enable	no connection
Ground	1

2. Load and run program 0 on tape side A (Initialize Program). Set up the test Troubleshooter as follows:

   Start - rising, external
   Stop - falling, external
   Clock - rising, external
   Enable - always
   Stop Counter - disabled
   Transition count - gated

   or load register 8 with 5000420, and run program 12, then 1 (Interactive Operation Program).

3. Take signatures at the nodes listed in Table 5-1 and verify that the signatures taken match those listed in the table.

4. If all signatures verify as correct, set up the test Troubleshooter as follows to take signatures in the signature, events, and waveform sections of the defective Signature Module:

   Start - rising, external
   Stop - falling, external
   Clock - falling, external
   Enable - always
   Stop Counter - disabled
   Transition count - gated

   or load register 8 with 5000520, and run program 12, then 1.

5. Connect the Data Probe of the defective unit. Attach the Data Probe tip to pin 10 on the DIP clip, and attach the Data Probe ground lead to pin 1 on the DIP clip.

6. The clock module in the defective unit is not used; disconnect it from the DIP clip and troubleshooter.

7. Load and run stimulus program 2 on side B in the defective unit. Press the LOOP key to continuously repeat the program.

8. Take signatures with the test Troubleshooter at the nodes listed in Table 5-2, and verify that the signatures taken match those listed.

Section 4
List of Replaceable Parts

INTRODUCTION 4-1.

This section contains an illustrated parts list for the instrument. Components are listed alphanumerically by assembly.

Parts lists include the following information:

1. Reference Designation.
2. Description of Each Part.
3. Fluke Stock Number.
4. Federal Supply Code for Manufacturers (see the 9000 Series Troubleshooter Service Manual for Code-to-Name list).
5. Manufacturer's Part Number.
6. Total Quantity of Component Per Assembly.
7. Recommended quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of 2 years. This list presumes an availability of common electronic parts at the maintenance site. for maintenance for 1 year or more at an isolated site, it is recommended that a least one of each assembly in the instrument be stocked.

HOW TO OBTAIN PARTS 4-2.

Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. or an authorized representative by using the Fluke Stock Number.

In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To ensure prompt and efficient handling of your order, include the information.

1. Quantity.
2. Fluke Stock Number.

3. Description.

4. Reference Designation.

5. Printed Circuit Board Part Number and Revision Letter.

6. Instrument Model and Serial Number.

A Recommended Spare Parts Kit for your basic instrument is available for the factory. This kit contains those items listed in the REC QTY column for the parts lists in the quantities recommended.

Parts price information is available from the John Fluke Mfg. Co., Inc. or its representative. Prices are also available in a Fluke Replacement Parts Catalog, which is available upon request.

CAUTION

*****

Indicated devices are subject to damage by static discharge.

TABLE 4-1. 9000A-006 FINAL ASSEMBLY
(SEE FIGURE 4-1.)

REFERENCE DESIGNATOR A->NUMERICS--->		S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE---	TOT QTY	R S -Q	N O T -E
		*	CLOCK MODULE ASSEMBLY	755694	89536	755694	1		
A	1	*	MAIN PCA	755728	89536	755728	1		
H	1		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	89536	178533	4		
H	2		CONN ACC,D-SUB,SLIDING LOCK,POST ASSY	353201	89536	353201	2		
H	3		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	1		
MP	1		BRACKET	758599	89536	758599	1		
MP	2		SPACER,HEX,BRASS,6-32X5/8,MALE/FEMALE	757427	89536	757427	1		
MP	3		SPACER,HEX,BRASS,6-32X3/4,MALE/FEMALE	757435	89536	757435	2		
MP	4		BRACKET, CONNECTOR	760033	89536	760033	1		
MP	5		CABLE TIE,6-3/4"L,0.190"W,1.75 DIA	104265	06383	SST-25	1		
MP	6		ACCESSORY KIT	764928	89536	764928	1		
R			RES,CF,39K,+-5%,0.25W	442400	80031	CR251-4-5P39K	1		1
TM	1		9000A-006 OPERATORS MANUAL	773259	89536	773259	1		
TM	2		9000A-006 SERVICE MANUAL	783944	89536	783944	1		
W	1		CABLE, CASE BOTTOM	755744	89536	755744	1		
W	2		CABLE, POWER	755751	89536	755751	1		
W	3		CABLE, PIA	755769	89536	755769	1		
W	4		CABLE, DELAY LINE	755777	89536	755777	1		

RECOMMENDED SPARE PARTS KIT

1 R62 ON 9010A MAIN PCA
R68 ON 9020A MAIN PCA

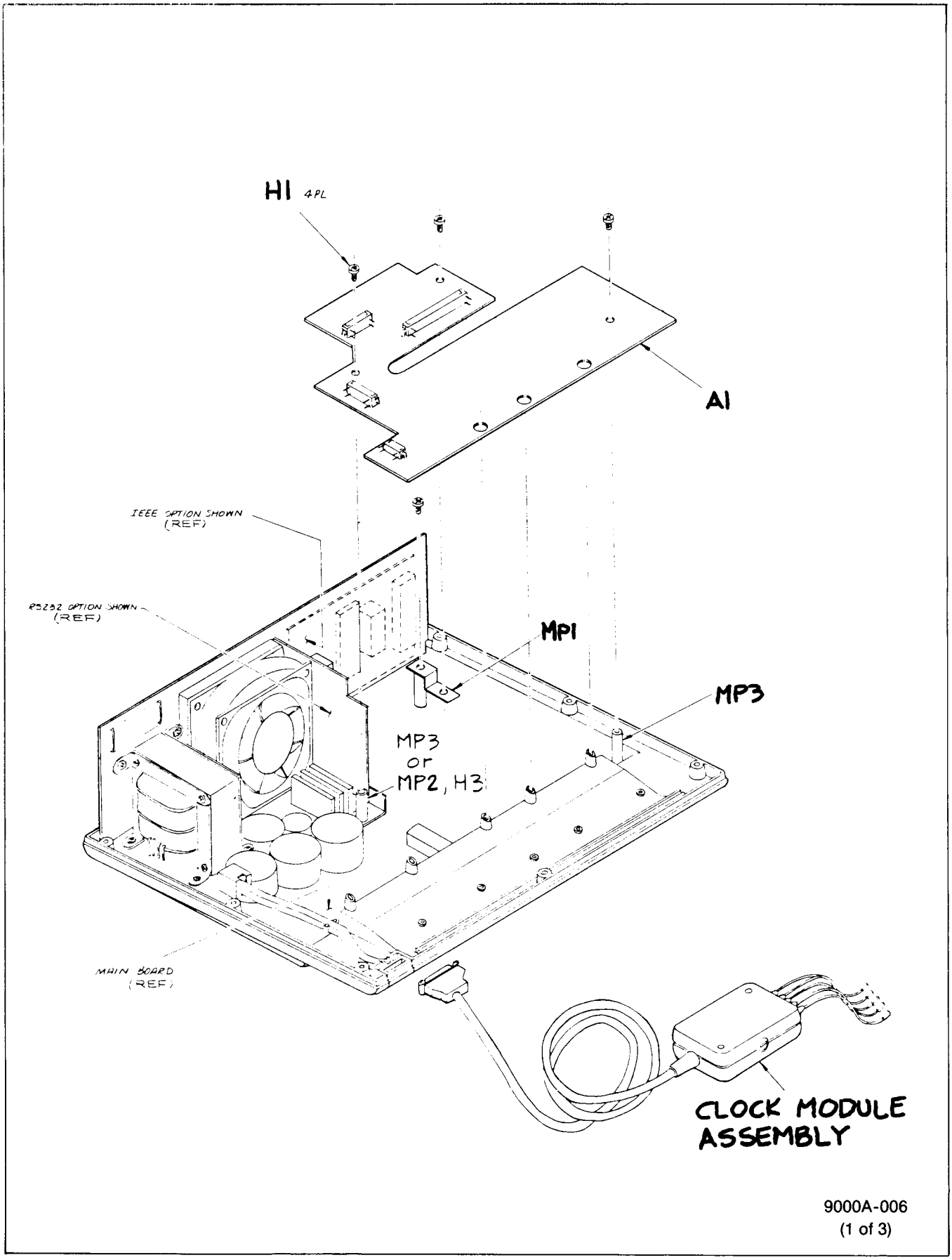


Figure 4-1. 9000A-006 Final Assembly

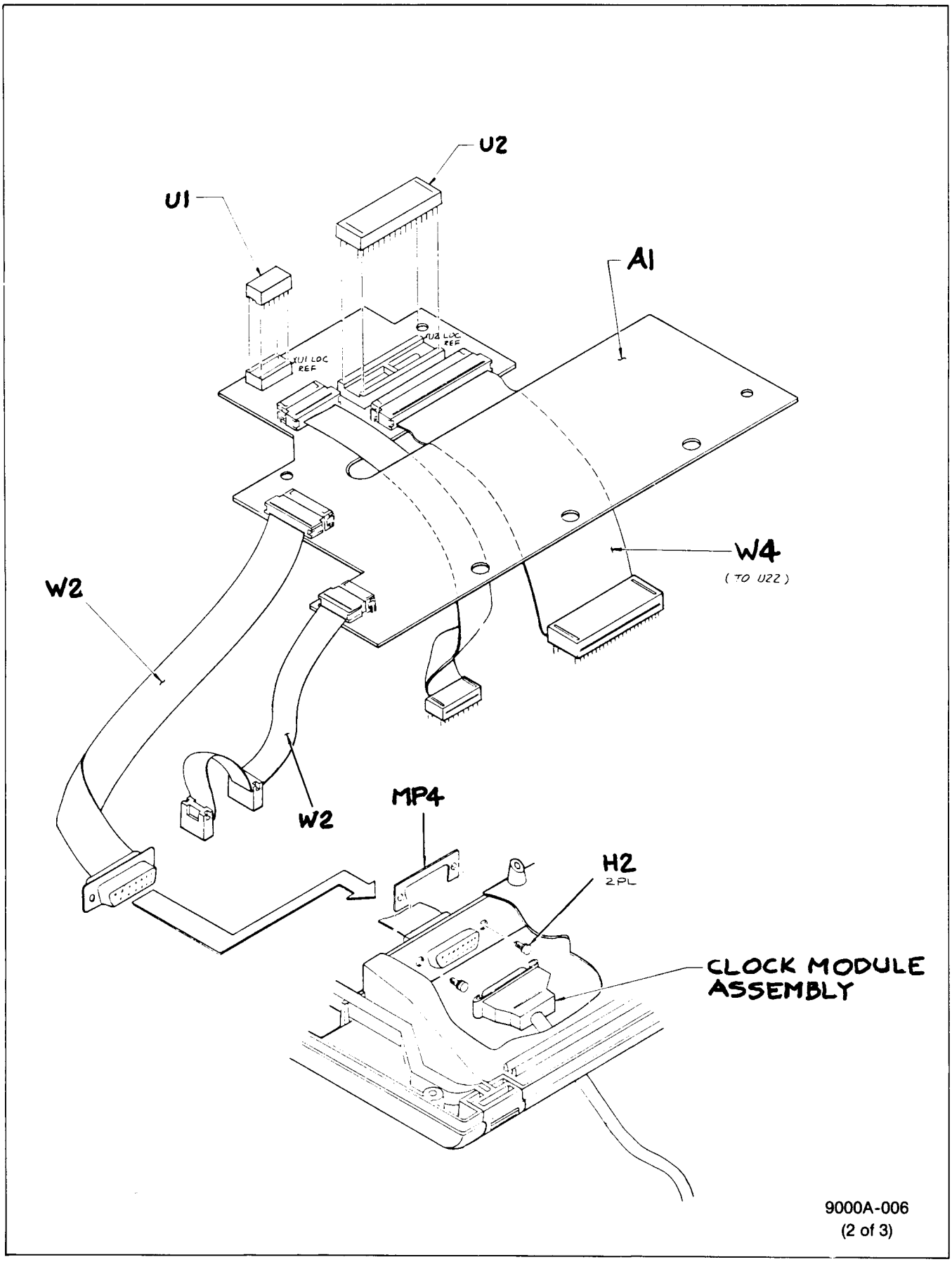


Figure 4-1. 9000A-006 Final Assembly (cont)

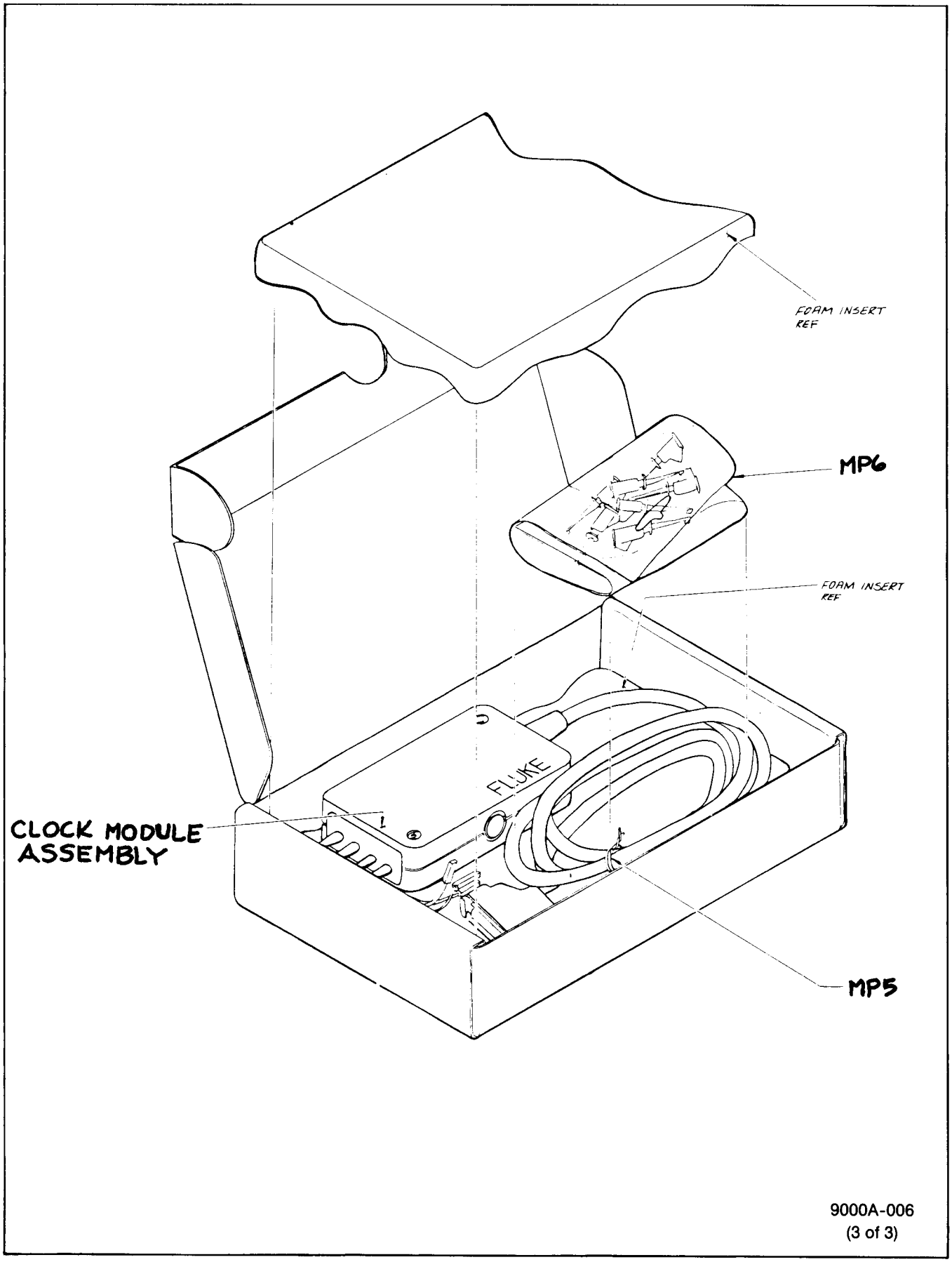


Figure 4-1. 9000A-006 Final Assembly (cont)

TABLE 4-2. A1 MAIN PCA
(SEE FIGURE 4-2.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
C 1- 15, 17,		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	45		
C 18, 23- 34,			747261					
C 37, 40- 54			747261					
C 16		CAP,CER,47PF,+-10%,50V,COG,1206	747352	89536	747352	1		
C 19, 20, 22		CAP,TA,10UF,+-20%,25V	772491	89536	772491	3	1	
C 35, 36		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	89536	740597	2		
C 38		CAP,CER,1000PF,+-10%,50V,COG,1206	747378	89536	747378	1		
CR 1		DIODE,SI,BV=70.0V,IO=50MA,DUAL	742320	89536	742320	1		
J 1		HEADER,2 ROW,0.200CTR,RT ANG,40 PIN	757450	89536	757450	1		
J 2		HEADER,2 ROW,0.100CTR,RT ANG,14 PIN	757443	89536	757443	1		
J 3		HEADER,2 ROW,0.100CTR,RT ANG,16 PIN	417030	89536	417030	1		
J 4		HEADER,2 ROW,0.100CTR,RT ANG,10 PIN	658112	89536	658112	1		
R 1, 2		RES, CHIP, CERMET, 10K,+-5%, 0.125W	746610	89536	746610	2		
R 3, 6		RES, CHIP, CERMET,1.8K,+-5%, 0.125W	746453	89536	746453	2		
R 4, 5		RES,CHIP,CERM,91,+-5%,0.125W	756338	89536	756338	2		
R 7, 8		RES, CHIP, CERMET, 33,+-5%, 0.125W	746248	89536	746248	2	1	
R 9		RES,CHIP,CERM,1K,+-5%,0.125W	745992	89536	745992	1		
R 10, 15		RES,CHIP,CERM,200,+/-5%,.125W	746339	89536	746339	2		
R 11		RES, CHIP, CERMET, 15K,+-5%, 0.125W	746628	89536	746628	1		
R 12, 13, 14		RES, CHIP, CERMET, 18K,+-5%, 0.125W	746636	89536	746636	3		
R 16		RES,CHIP,CERM,4.7K,+-5%,0.125W	740522	89536	740522	1		
U 3	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	89536	742122	1	1	
U 4	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	740928	89536	740928	1	1	
U 5		OSCILLATOR,25.0MHZ,TTL CLOCK	756346	89536	756346	1		
U 6, 22, 24,	*	IC,FTTL,DUAL D F/F,+EDG TRG,SOIC	742163	89536	742163	5	1	
U 48, 50	*		742163					
U 7, 16	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	89536	740878	2	1	
U 8, 9, 10	*	IC,LSTTL, 4 BIT UP/DOWN CNTR,SOIC	742114	89536	742114	3	2	
U 11, 12	*	IC,LSTTL,8BIT ADDRSABLE LATCH,SOIC	742130	89536	742130	2	1	
U 13, 47	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	89536	740985	2	1	
U 14, 15, 27,	*	IC,LSTTL,8BIT S-IN,P-OUT R-SHFT,SOIC	742106	89536	742106	8	2	
U 28, 40, 41,	*		742106					
U 55, 56	*		742106					
U 17, 18	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE,SOIC	740969	89536	740969	2	1	
U 19	*	IC,LSTTL,DUAL 4-1 SELECT/MUX,SOIC	742098	89536	742098	1	1	
U 20	*	IC,FTTL,DUAL 4 INPUT NAND GATE,SOIC	742155	89536	742155	1	1	
U 21	*	IC,FTTL,TRIPLE 3 INPUT NAND GATE	743435	89536	743435	1	1	
U 23, 29	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	89536	740860	2	1	
U 25	*	IC,FTTL,QUAD 2 INPUT NAND GATE,SOIC	772897	89536	772897	1		
U 26, 38	*	IC,TTL,RETRG MONOSTAB MULTIVB S01C	742924	89536	742924	2	1	
U 33	*	IC,FTTL,HEX INVERTER,SOIC	742148	89536	742148	1	1	
U 34, 35	*	IC,FTTL,DUAL 4-1 LINE MUX,SOIC	772806	89536	772806	2	1	
U 36, 51	*	IC,FTTL,QUAD 2 INPUT XOR GATE,SOIC	742171	89536	742171	2	1	
U 37, 52	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	89536	741033	2	1	
U 42	*	IC,FTTL,QUAD 2 INPUT OR GATE,SOIC	743237	89536	743237	1	1	
U 46	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	89536	741025	1	1	
U 49	*	IC,LSTTL,TRIPLE 3 INPUT AND GATE,SOIC	741009	89536	741009	1	1	
U 54	*	IC,COMPARATOR,HIGH-SPEED,14 PIN,SOIC	742197	89536	742197	1	1	
U 57- 62	*	IC,LSTTL,DIV BY 16 BINARY CNTR,SOIC	742247	89536	742247	6	1	
U 63- 66	*	IC,FTTL,4BIT R&L-SHIFT RGSTR,SOIC	742189	89536	742189	4	1	
XU		SOCKET,IC,14 PIN	276527	89536	276527	3		
XU 2		SOCKET,IC,SURFACE MOUNT,40 PIN	769331	89536	769331	1		

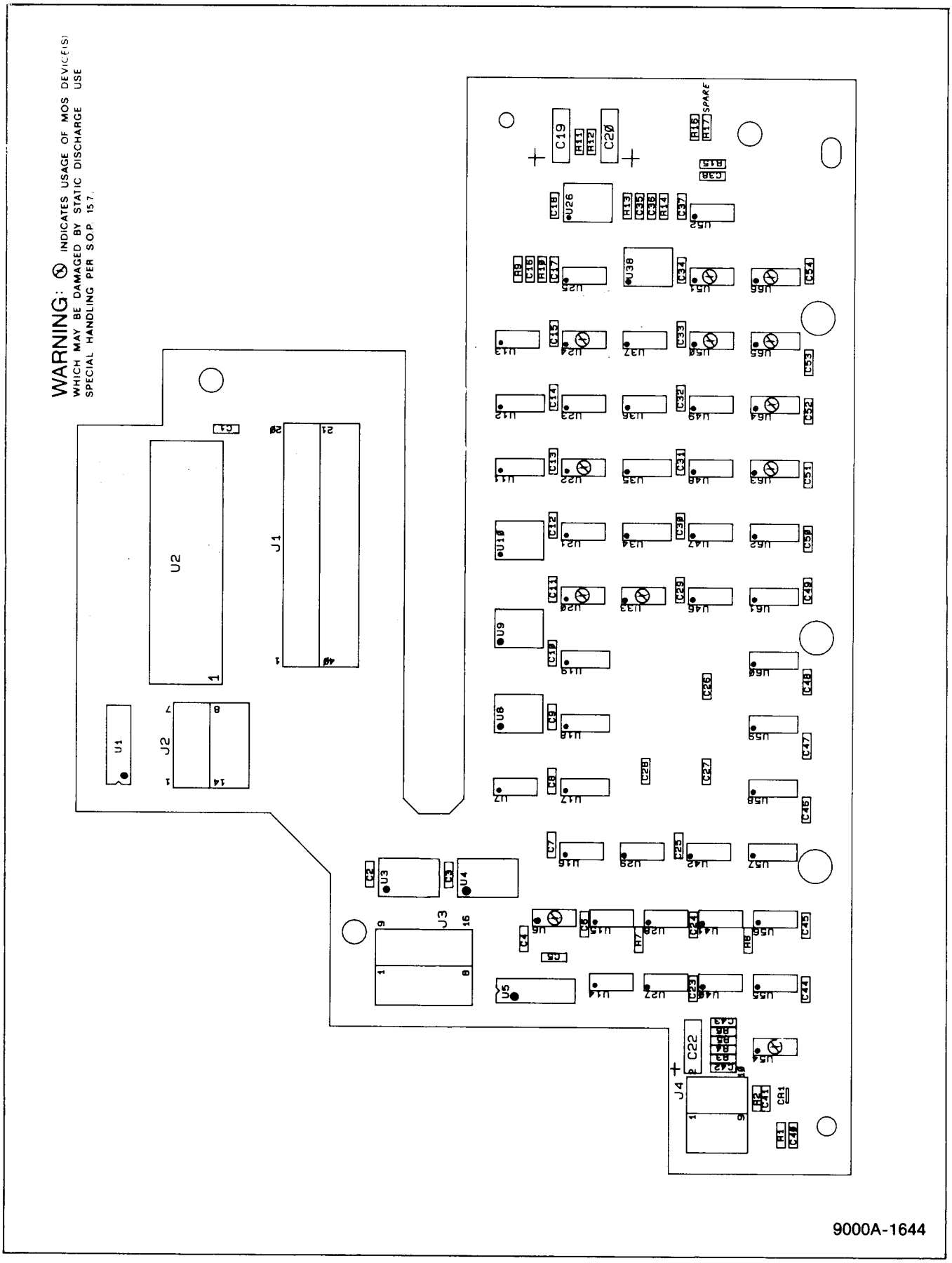


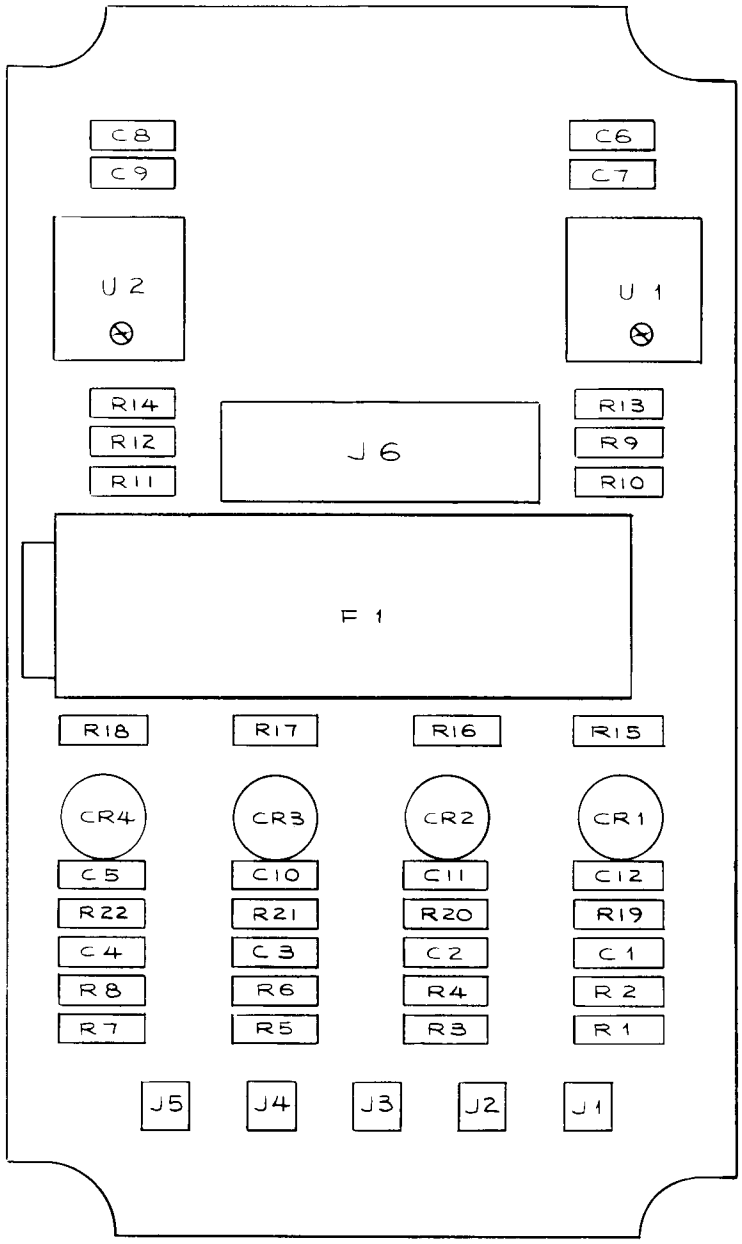
Figure 4-2. A1 Main PCA

TABLE 4-3. CLOCK MODULE ASSEMBLY

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
A 2	*	CLOCK MODULE PCA	767897	89536	767897	1		
F 1		FUSE,1/4 X 1-1/4,FAST,0.25A,250V	109314	71400	AGC1-4	1		
H 1		SCREW,MACH,PHP SEMS,STL,4-40X1/4	185918	89536	185918	2		
H 2		SCREW,MACH,PHP,STL,4-40X1/2	558825	89536	558825	4		
MP 2		SHIELD, CLOCK MODULE	755793	89536	755793	1		
MP 3		CASE, CLOCK MODULE	760025	89536	760025	1		
MP 4		COVER	755686	89536	755686	1		
MP 5		CASE, CLOCK MODULE	760017	89536	760017	1		
MP 6		SPACER,HEX,ALUM,4-40X0.500	192872	89536	192872	1		
W		CABLE, CLOCK MODULE	749895	89536	749895	1		
W		CABLE, MICRO-CLIP	755736	89536	755736	1		
XF 1		HLDR PART,FUSE,CAP,1/4 X 1-1/4,GREY	460238	61935	031.1666	1	5	

TABLE 4-4. A2 CLOCK MODULE PCA
(SEE FIGURE 4-3.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE---	TOT QTY	R S -Q	NOT -E
C 1- 4		CAP,CER,10PF,+-10%,50V,COG,1206	747311	89536	747311	4		
C 5- 12		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	8		
CR 1- 4		DIODE,$I,BV=70.0V,IO=50MA,DUAL	742320	89536	742320	4	1	
F 1		HLDR PART,FUSE,BODY,PWB MT	602763	89536	602763	1		
J 1- 5		PIN,SIGNLE,PWB,0.058 DIA	233411	89536	233411	5		
J 6		HEADER,2 ROW,0.100CTR, RT ANG,16 PIN	417030	89536	417030	1		
R 1- 8		RES, CHIP, CERMET, 22K,+-5%, 0.125W	746651	89536	746651	8		
R 9- 12		RES, CHIP, CERMET, 33,+-5%, 0.125W	746248	89536	746248	4	1	
R 13		RES, CHIP, CERMET,3.6K,+-5%, 0.125W	746537	89536	746537	1		
R 14		RES, CHIP, CERMET, 750,+-5%, 0.125W	746404	89536	746404	1		
R 15- 18		RES, CHIP, CERMET,120K +-5%, 0.125W	746719	89536	746719	4		
R 19- 22		RES, CHIP, CERMET, 10K,+-5%, 0.125W	746610	89536	746610	4		
U 1, 2	*	IC,COMPARATOR,HIGH-SPEED,14 PIN,SOIC	742197	89536	742197	2		

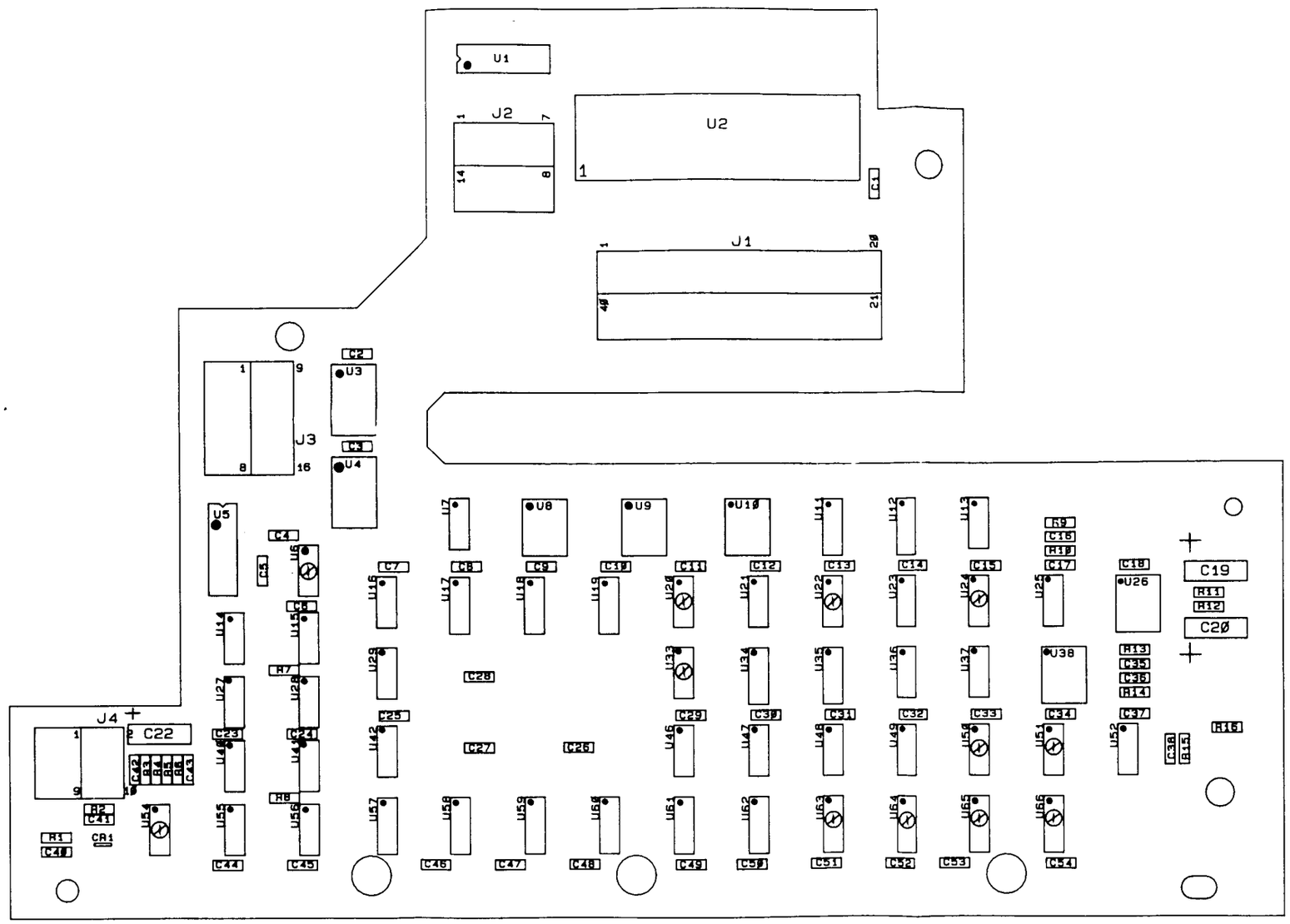


CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

9000A-1615

Figure 4-3. A2 Clock Module PCA

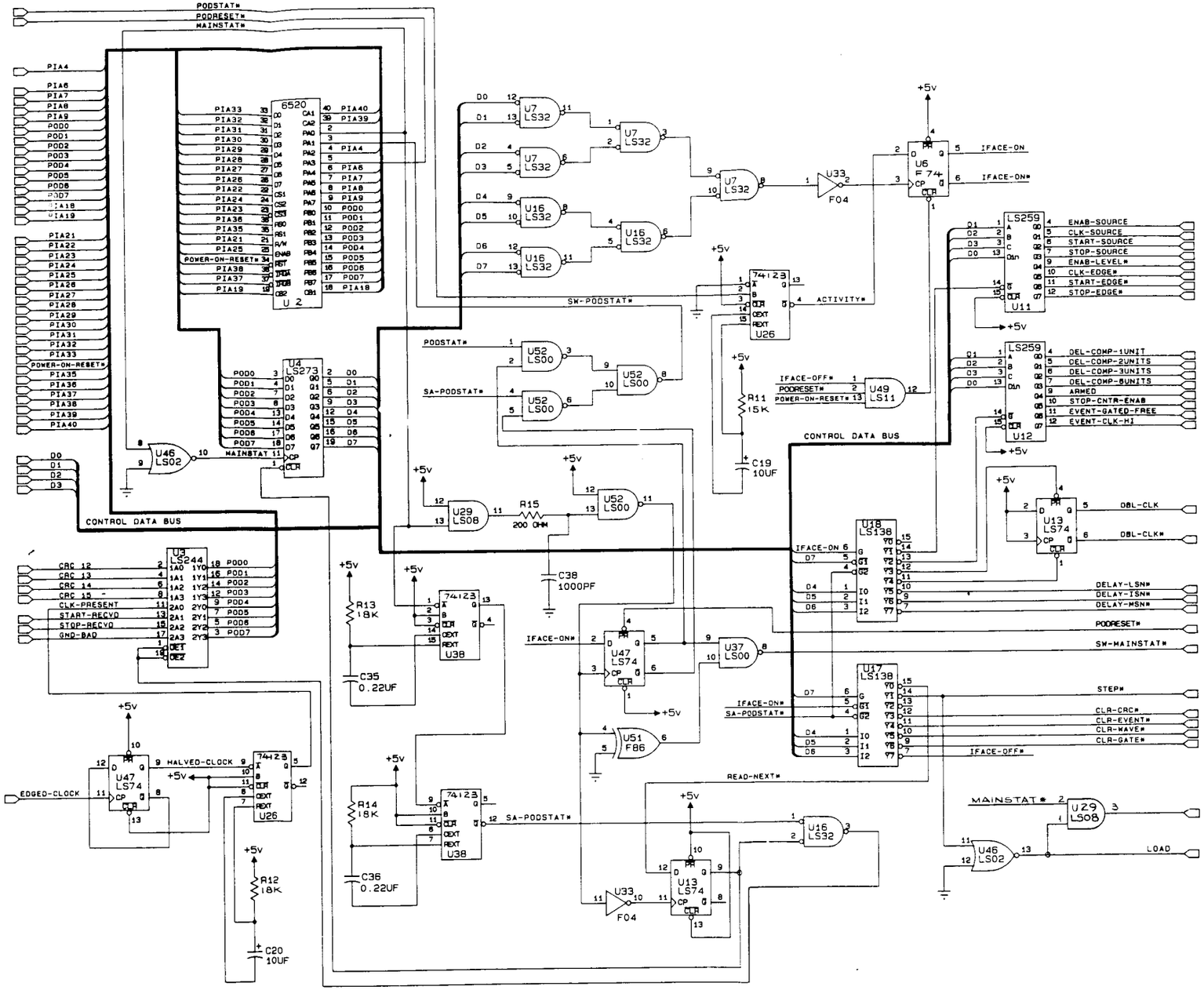
Section 5
Schematic Diagrams



WARNING: ⊘ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 15.7.

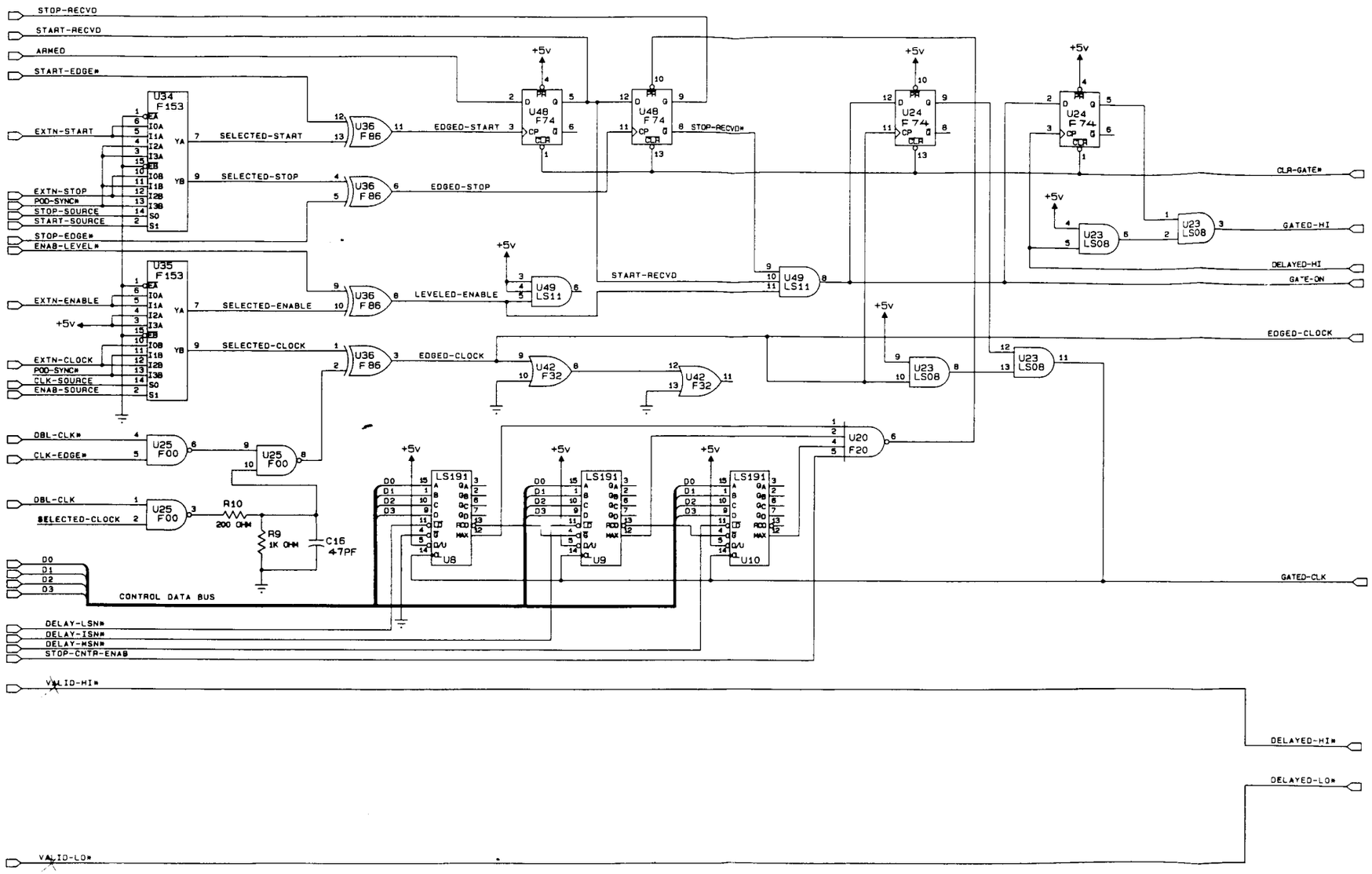
9000A-1644

Figure 5-1. A1 Main PCA



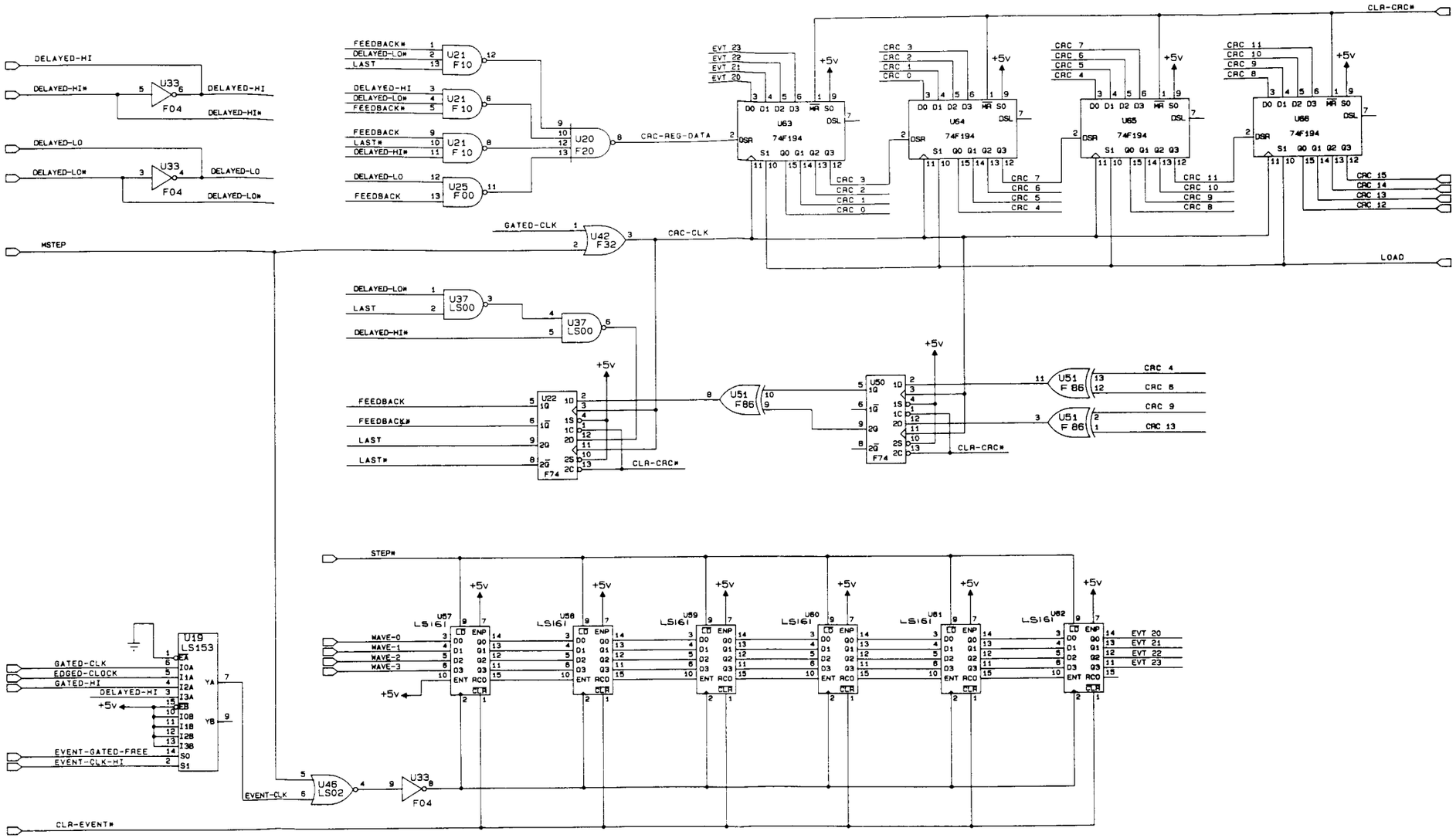
9000A-1044
(1 of 5)

Figure 5-1. A1 Main PCA (cont)



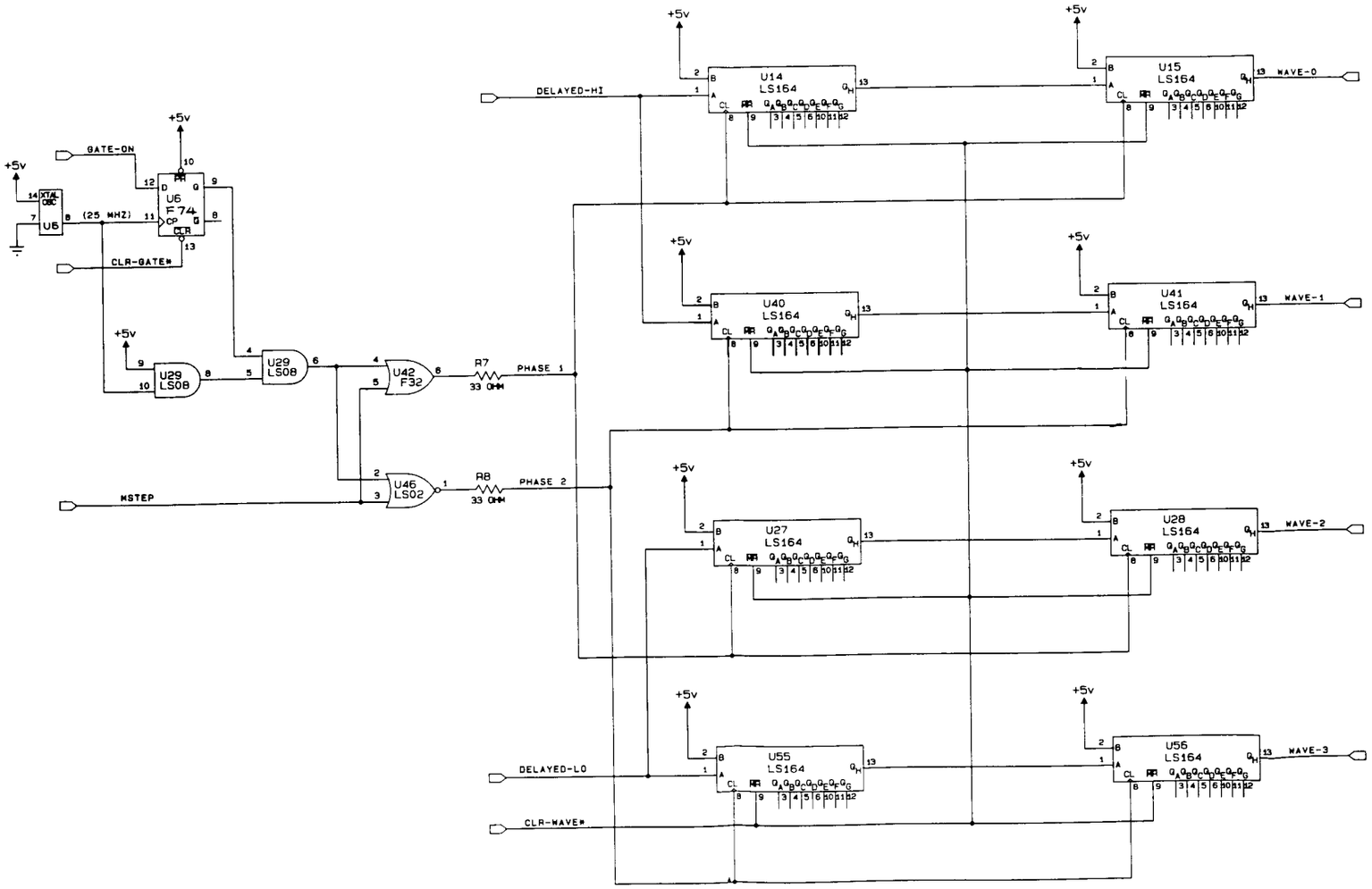
9000A-1044
(2 of 5)

Figure 5-1. A1 Main PCA (cont)



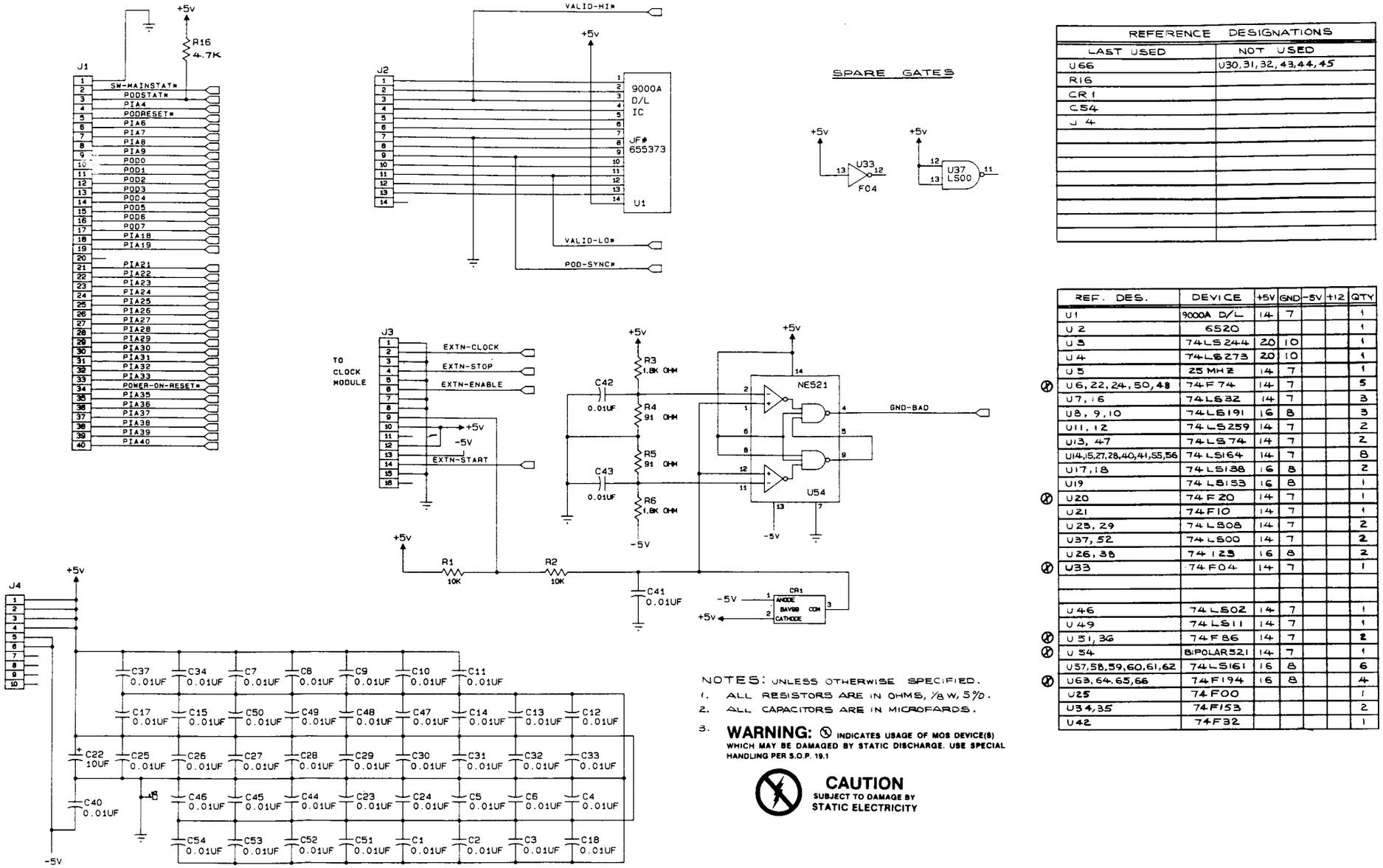
9000A-1044
(3 of 5)

Figure 5-1. A1 Main PCA (cont)



9000A-1044
(4 of 5)

Figure 5-1. A1 Main PCA (cont)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE IN OHMS, ⅛ W, 5%.
2. ALL CAPACITORS ARE IN MICROFARDS.
3. **WARNING:** Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1

CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
U66	U30, 31, 32, 43, 44, 45
R16	
CR1	
C54	
J 4	

REF. DES.	DEVICE	+5V	GND	-5V	+12	QTY
U1	9000A D/L	14	7			1
U 2	6520					1
U 3	74LS244	20	10			1
U 4	74LS273	20	10			1
U 5	25 MHZ	14	7			1
Ⓢ U6, 22, 24, 50, 48	74F74	14	7			5
U7, 16	74LS32	14	7			3
U8, 9, 10	74LS191	16	8			3
U11, 12	74LS259	14	7			2
U13, 47	74LS74	14	7			2
U14,15,27,28,40,41,55,56	74LS164	14	7			8
U17,18	74LS138	16	8			2
U19	74LS153	16	8			1
Ⓢ U20	74F20	14	7			1
U21	74F10	14	7			1
U23, 29	74LS08	14	7			2
U37, 52	74LS00	14	7			2
U26, 38	74123	16	8			2
Ⓢ U33	74F04	14	7			1
U46	74LS02	14	7			1
U49	74LS11	14	7			1
Ⓢ U31, 36	74F86	14	7			2
Ⓢ U54	BIPOLAR521	14	7			1
U37,58,59,60,61,62	74LS161	16	8			6
Ⓢ U63, 64, 65, 66	74F194	16	8			4
U25	74F00					1
U34,35	74F153					2
U42	74F32					1

9000A-1044
(5 of 5)

Figure 5-1. A1 Main PCA (cont)

Table 5-1. Signature Module Signatures (With Stimulus Program 1)

THESE SIGNATURES ARE VALID ONLY FOR BOARD ASSEMBLY REVISION LEVELS 0-3 AND A.

NODE	SIG.	NODE	SIG.	NODE	SIG.	NODE	SIG.	NODE	SIG.
U2-10	631B	U2-11	4DE7	U2-12	96CE	U2-13	348E	U2-14	A2B6
U2-15	44E8	U2-16	E23E	U2-17	204D	U3-1	929C	U3-3	204D
U3-5	E23E	U3-7	44E8	U3-9	A2B6	U3-10	0000	U3-12	348E
U3-13	25FD	U3-14	96CE	U3-15	929C	U3-16	4DE7	U3-17	0000
U3-18	631B	U3-19	929C	U3-20	929C	U4-1	929C	U4-2	631B
U4-3	631B	U4-4	4DE7	U4-5	4DE7	U4-6	96CE	U4-7	96CE
U4-8	348E	U4-9	348E	U4-10	0000	U4-12	A2B6	U4-13	A2B6
U4-14	44E8	U4-15	44E8	U4-16	E23E	U4-17	E23E	U4-18	204D
U4-19	204D	U4-20	929C	U6-1	929C	U6-2	929C	U6-3	DBD2
U6-4	929C	U6-5	929D	U6-6	0001	U6-7	0000	U6-12	0000
U6-13	929E	U6-14	929C	U7-1	5771	U7-2	C3D9	U7-3	14F2
U7-4	96CE	U7-5	348E	U7-6	C3D9	U7-7	0000	U7-8	494E
U7-9	14F2	U7-10	494E	U7-11	5771	U7-12	631B	U7-13	4DE7
U7-14	929C	U8-1	4DE7	U8-2	0E1B	U8-3	0E1B	U8-4	0000
U8-5	929C	U8-6	0E1B	U8-7	0E1B	U8-8	0000	U8-9	348E
U8-10	96CE	U8-11	9B8A	U8-12	9C87	U8-13	0E1B	U8-14	0000
U8-15	631B	U8-16	929C	U9-1	4DE7	U9-2	0F19	U9-3	0F19
U9-4	0E1B	U9-5	929C	U9-6	0F19	U9-7	0F19	U9-8	0000
U9-9	348E	U9-10	96CE	U9-11	9617	U9-12	9DB5	U9-13	0F19
U9-14	0000	U9-15	631B	U9-16	929C	U10-1	4DE7	U10-2	0F98
U10-3	0F98	U10-4	0F19	U10-5	929C	U10-6	0F98	U10-7	0F98
U10-8	0000	U10-9	348E	U10-10	96CE	U10-11	90D9	U10-12	9D04
U10-13	0F98	U10-14	0000	U10-15	631B	U10-16	929C	U11-1	4DE7
U11-2	96CE	U11-3	348E	U11-4	9E97	U11-5	1499	U11-6	D19E
U11-7	331D	U11-8	0000	U11-9	C25C	U11-10	66E8	U11-11	114B
U11-12	5377	U11-13	631B	U11-14	5B9B	U11-15	929C	U11-16	929C
U12-1	4DE7	U12-2	96CE	U12-3	348E	U12-4	3516	U12-5	929C
U12-6	58E4	U12-7	E002	U12-8	0000	U12-9	5F08	U12-10	A439
U12-11	98C9	U12-12	9009	U12-13	631B	U12-14	900C	U12-15	929C
U12-16	929C	U13-1	7F75	U13-2	929C	U13-3	929C	U13-4	D239
U13-5	A4E8	U13-6	3677	U13-7	0000	U13-8	0000	U13-9	929C
U13-10	929C	U13-12	929C	U13-13	929C	U13-14	929C	U14-7	0000
U14-9	9298	U14-14	929C	U15-7	0000	U15-9	9298	U15-14	929C
U16-4	A4AF	U16-5	C27C	U16-9	A2B6	U16-10	44E8	U16-11	C27C
U16-12	E23E	U16-13	204D	U16-14	929C	U17-1	A2B6	U17-2	44E8
U17-3	E23E	U17-4	0000	U17-5	0001	U17-6	204D	U17-7	929C
U17-8	0000	U17-9	929E	U17-10	9298	U17-11	9294	U17-12	928C
U17-13	929C	U17-14	B2CE	U17-15	929C	U17-16	929C	U18-1	A2B6
U18-2	44E8	U18-3	E23E	U18-4	0000	U18-5	204D	U18-6	929D
U18-7	90D9	U18-8	0000	U18-9	9617	U18-10	9B8A	U18-11	7F75

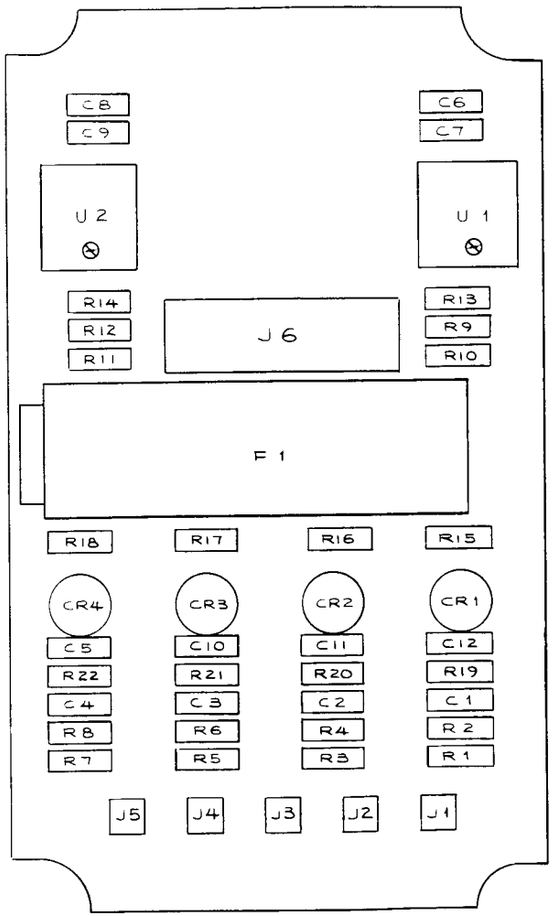
Table 5-1. Signature Module Signatures For Program 1 (cont.)

NODE	SIG.	NODE	SIG.	NODE	SIG.	NODE	SIG.	NODE	SIG.
U18-12	D239	U18-13	900C	U18-14	5B9B	U18-15	494E	U18-16	929C
U19-1	0000	U19-2	9009	U19-8	0000	U19-14	98C9	U19-16	929C
U20-1	9C87	U20-2	9D85	U20-4	9D04	U20-5	A439	U20-6	36A5
U20-7	0000	U20-14	929C	U22-1	928C	U22-7	0000	U22-13	928C
U22-14	929C	U23-7	0000	U23-8	F49F	U23-9	929C	U23-10	F49F
U23-11	0000	U23-12	0000	U23-13	F49F	U23-14	929C	U24-1	929E
U24-2	0000	U24-4	929C	U24-7	0000	U24-8	929C	U24-9	0000
U24-10	929C	U24-11	F49F	U24-12	0000	U24-13	929E	U24-14	929C
U25-1	A4E8	U25-2	5D2D	U25-3	F92D	U25-4	3677	U25-5	66E8
U25-6	509F	U25-7	0000	U25-8	A9B2	U25-9	509F	U25-10	F92D
U25-14	929C	U26-1	0000	U26-2	929C	U26-3	929C	U26-4	929C
U26-8	0000	U26-13	0000	U26-16	929C	U27-7	0000	U27-9	9298
U27-14	929C	U28-7	0000	U28-9	9298	U28-14	929C	U33-1	494E
U33-2	DBD2	U34-1	0000	U34-2	D19E	U34-3	A2B6	U34-4	A2B6
U34-5	631B	U34-6	631B	U34-7	6A6F	U34-8	0000	U34-9	340A
U34-10	4DE7	U34-11	A2B6	U34-12	4DE7	U34-13	A2B6	U34-14	331D
U34-15	0000	U34-16	929C	U35-1	0000	U35-2	9E97	U35-3	929C
U35-4	929C	U35-5	348E	U35-6	348E	U35-7	A48C	U35-8	0000
U35-9	5D2D	U35-10	96CE	U35-11	A2B6	U35-12	96CE	U35-13	A2B6
U35-14	1499	U35-15	0000	U35-16	929C	U36-1	5D2D	U36-2	A9B2
U36-3	F49F	U36-4	340A	U36-5	5377	U36-6	677D	U36-7	0000
U36-8	66D0	U36-9	C25C	U36-10	A48C	U36-11	7B24	U36-12	1148
U36-13	6A6F	U36-14	929C	U40-7	0000	U40-9	9298	U40-14	929C
U41-7	0000	U41-9	9298	U41-14	929C	U42-7	0000	U42-8	F49F
U42-9	F49F	U42-10	0000	U42-11	F49F	U42-12	F49F	U42-13	0000
U42-14	929C	U46-11	B2CE	U46-12	0000	U46-13	2052	U47-1	929C
U47-2	0001	U47-4	929C	U47-5	0000	U47-6	929C	U48-1	929E
U48-2	5F08	U48-3	7B24	U48-4	929C	U48-5	25FD	U48-6	B761
U48-7	0000	U48-8	0002	U48-9	929C	U48-10	36A5	U48-11	677D
U48-12	25FD	U48-13	929E	U48-14	929C	U49-1	929C	U49-2	929C
U49-3	929C	U49-4	929C	U49-5	66D0	U49-6	66D0	U49-7	0000
U49-8	0000	U49-9	0002	U49-10	25FD	U49-11	66D0	U49-12	929C
U49-13	929C	U49-14	929C	U50-1	928C	U50-7	0000	U50-13	928C
U50-14	929C	U55-7	000C	U55-9	9298	U55-14	929C	U56-7	0000
U56-9	9298	U56-14	929C	U57-1	9294	U57-8	0000	U57-9	B2CE
U57-16	929C	U58-1	9294	U58-8	0000	U58-9	B2CE	U58-16	929C
U59-1	9294	U59-8	0000	U59-9	B2CE	U59-16	929C	U60-1	9294
U60-8	0000	U60-9	B2CE	U60-16	929C	U61-1	9294	U61-8	0000
U61-9	B2CE	U61-16	929C	U62-1	9294	U62-8	0000	U62-9	B2CE
U62-16	929C	U63-1	928C	U63-8	0000	U63-10	2052	U63-16	929C
U64-1	928C	U64-8	0000	U64-10	2052	U64-16	929C	U65-1	928C
U65-8	0000	U65-10	2052	U65-16	929C	U66-1	928C	U66-8	0000
U66-10	2052	U66-16	929C						

Table 5-2. Signature Module Signatures (With Stimulus Program 2)

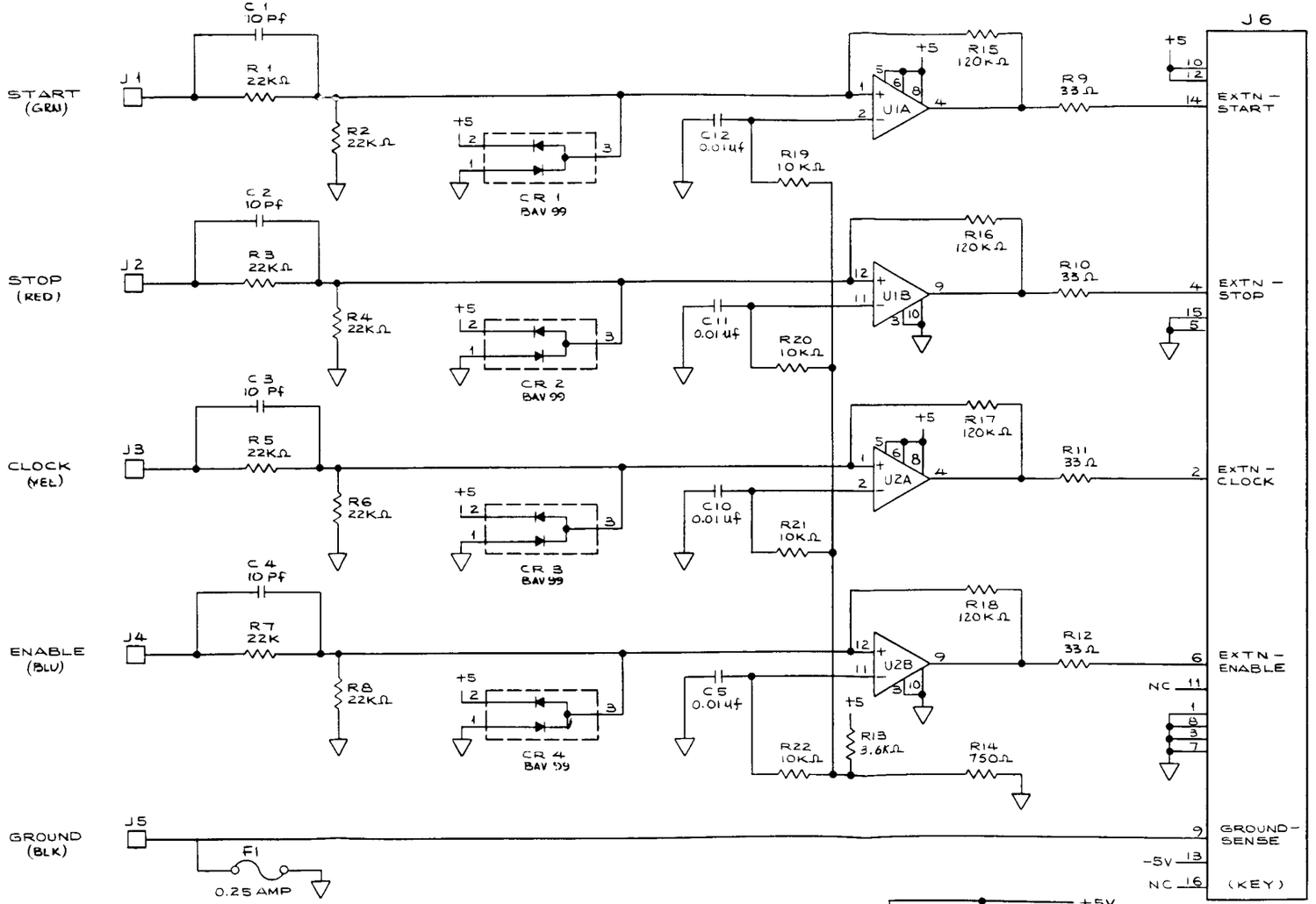
THESE SIGNATURES ARE VALID ONLY FOR BOARD ASSEMBLY REVISION LEVELS 0-3 AND A.

NODE	SIG.	NODE	SIG.	NODE	SIG.	NODE	SIG.	NODE	SIG.
U2-10	AD5E	U3-2	99CB	U3-4	99CB	U3-6	D0B5	U3-8	D0B5
U14-1	AD5E	U14-2	494E	U14-13	D8AD	U15-1	D8AD	U15-2	494E
U15-13	2DD8	U20-8	99E8	U20-9	1E21	U20-10	1E21	U20-12	D2E6
U20-13	87C9	U21-1	7DF8	U21-2	AD5E	U21-3	AD5E	U21-4	AD5E
U21-5	7DF8	U21-6	1E21	U21-7	0000	U21-8	D2E6	U21-9	34B6
U21-10	1FE1	U21-11	E410	U21-12	1E21	U21-13	56AF	U21-14	494E
U22-2	CF64	U22-4	494E	U22-5	34B6	U22-6	7DF8	U22-8	1FE1
U22-9	56AF	U22-10	494E	U22-12	AD5E	U25-11	87C9	U25-12	E410
U25-13	34B6	U27-1	E410	U27-2	494E	U27-13	91E3	U28-1	91E3
U28-2	494E	U28-13	6496	U33-3	AD5E	U33-4	E410	U33-5	E410
U33-6	AD5E	U37-1	AD5E	U37-2	56AF	U37-3	4ACE	U37-4	4ACE
U37-5	E410	U37-6	AD5E	U40-1	AD5E	U40-2	494E	U40-13	D8AD
U41-1	D8AD	U41-2	494E	U41-13	2DD8	U50-2	494E	U50-4	494E
U50-5	494E	U50-6	0000	U50-7	0000	U50-8	CF64	U50-9	862A
U50-10	494E	U50-12	AA5D	U50-14	494E	U51-1	99CB	U51-2	3396
U51-3	AA5D	U51-7	0000	U51-8	CF64	U51-9	862A	U51-10	494E
U51-11	494E	U51-12	2E63	U51-13	672D	U51-14	494E	U55-1	E410
U55-2	494E	U55-13	91E3	U56-1	91E3	U56-2	494E	U56-13	6496
U57-3	2DD8	U57-4	2DD8	U57-5	6496	U57-6	6496	U57-7	494E
U57-8	0000	U57-10	494E	U57-11	DFA2	U57-12	DFA2	U57-13	96EC
U57-14	96EC	U57-15	0000	U57-16	494E	U58-3	96EC	U58-4	96EC
U58-5	DFA2	U58-6	DFA2	U58-7	494E	U58-8	0000	U58-10	0000
U58-11	8238	U58-12	8238	U58-13	CB76	U58-14	CB76	U58-15	0000
U58-16	494E	U59-3	CB76	U59-4	CB76	U59-5	8238	U59-6	8238
U59-7	494E	U59-8	0000	U59-10	0000	U59-11	ACF5	U59-12	ACF5
U59-13	E5BB	U59-14	E5BB	U59-15	0000	U59-16	494E	U60-3	E5BB
U60-4	E5BB	U60-5	ACF5	U60-6	ACF5	U60-7	494E	U60-8	0000
U60-10	0000	U60-11	3B93	U60-12	3B93	U60-13	72DD	U60-14	72DD
U60-15	0000	U60-16	494E	U61-3	72DD	U61-4	72DD	U61-5	3B93
U61-6	3B93	U61-7	494E	U61-8	0000	U61-10	0000	U61-11	7020
U61-12	7020	U61-13	396E	U61-14	396E	U61-15	0000	U61-16	494E
U62-3	396E	U62-4	396E	U62-5	7020	U62-6	7020	U62-7	494E
U62-8	0000	U62-10	0000	U62-11	D5F9	U62-12	D5F9	U62-13	9CB7
U62-14	9CB7	U62-15	0000	U62-16	494E	U63-2	99E8	U63-3	9CB7
U63-4	9CB7	U63-5	D5F9	U63-6	D5F9	U63-8	0000	U63-9	494E
U63-12	8715	U63-13	8715	U63-14	CE5B	U63-15	CE5B	U63-16	494E
U64-2	8715	U64-3	CE5B	U64-4	CE5B	U64-5	8715	U64-6	8715
U64-8	0000	U64-9	494E	U64-12	2E63	U64-13	2E63	U64-14	672D
U64-15	672D	U64-16	494E	U65-2	2E63	U65-3	672D	U65-4	672D
U65-5	2E63	U65-6	2E63	U65-9	494E	U65-12	7AD8	U65-13	7AD8
U65-14	3396	U65-15	3396	U65-16	494E	U66-2	7AD8	U66-3	3396
U66-4	3396	U66-5	7AD8	U66-6	7AD8	U66-9	494E	U66-12	D0B5
U66-13	D0B5	U66-14	99CB	U66-15	99CB	U66-16	494E		



WARNING: Ⓜ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1

9000A-1615



REF. DES.	DEVICE	+5V	GND	-5V	QTY
U1, U2 Ⓜ	NE 521	14	7	13	2

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4W, 5%.

9000A-1015

Figure 5-2. A2 Clock Module Assembly