V. 8-BIT MICROPROCESSOR PODS

WARNINGS

BEFORE PLUGGING IN THE ML4400 TO AN AC POWER SOURCE, VERIFY THAT THE CORRECT VOLTAGE (115 OR 230) HAS BEEN SELECTED VIA THE VOLTAGE SELECTOR SWITCH AT THE UPPER RIGHT OF THE REAR PANEL.

DO NOT INSERT OR REMOVE ANY CAPTURE MODULE, AND DO NOT CONNECT OR DISCONNECT ANY LOGIC POD OR MICROPROCESSOR POD FROM THE ML4400, WITHOUT FIRST POWERING DOWN THE ML4400 VIA THE POWER SWITCH AT THE LOWER RIGHT OF THE REAR PANEL. FAILURE TO DO SO MAY DAMAGE THE UNIT.

A. GENERAL

1. CONNECTIONS AND ADAPTOR POD

See Section II-A.5, "Standard Capture Module and Microprocessor Pods", re connecting Microprocessor Pods to the ML4400.

Note that the following 8-Bit Microprocessor Pods require an Adaptor for ML4100 Microprocessor Pods (AD-4100) when connected to an ML4400. One Adaptor pod is needed for each Microprocessor Pod being used simultaneously (up to a maximum of four).

8I-080 (for Intel 8085, 8031/32, 8035/39/40)
8M-080 (for Motorola 6800, 6802/6808)
8M-089 (for Motorola 6809, 6809E)
8N-080 (for NSC800)
8R-065 (for Rockwell 6502, 65CX02, 6512, 65C112)
8Z-080 (for Zilog Z80)

2. DISASSEMBLY

See Section IV-D.4, "Disassembly Display Mode".

3. CONFIGURATION AND SETUP

When the ML4400 is configured with a Microprocessor Pod instead of a Logic Pod, there are several differences in its Setup screens, as discussed below.

a. Format Display Screen (via Format key)

The ML4400 will automatically configure itself at powerup for synchronous microprocessor cycle data collection. The default State format has four fields defined:

EXT, a binary field for the external probes, and STS, status line (Data Inputs 24-31)
ADR, address bus (Data Inputs 8-23)
DAT, data bus (Data Inputs 0-7)

The Data Inputs are labeled on the Format Display screen as probe numbers.

For all 8-Bit Microprocessor Pods, Data Inputs 0-7 are Data Bus Bits 0-7 (demultiplexed if required). Data Inputs 8-23 are the address bus, although some high-order bits may not be used. Data Inputs 24-31 contain Status and external Data Input lines.

On most Microprocessor Pods, two or four of the highest-numbered inputs are supplied as separate TTL inputs via a 20-pin connector on the side of the Pod. These lines are displayed in the "EXT" field. To use these TTL input lines, attach the 20-socket connector of a probe set from any ML4400 Logic Pod to the side connector on the Microprocessor Pod.

b. Clock Setup Screen (via CLOCK key)

The external clock signal is derived as required from the signals on each microprocessor. (External clock qualification is not used with Microprocessor Pods.)

c. Trigger Words Setup Screen (via TRIGGER key)

When a Microprocessor Pod is used with the ML4400, two additional softkeys are available on the Trigger Words Setup screen:

The ROLL STATUS softkey speeds up editing the Status fields by rolling through common choices for Status values (fetch, read, write, etc.). Status mnemonics are displayed to the right of the Status field.

The STATUS BIT DEF'S softkey opens the Status Bit help window, which defines each bit in the Status field. Depressing the softkey a second time closes the window.

d. Status, State, and State Search Screens

In these screens, status mnemonics are displayed to the right of each Status field.

4. OPERATION

Although all Arium 8-Bit Microprocessor Pods operate similarly, there are some differences among them. These differences and details of the data configuration of each Pod are discussed in Sections V-B and following, with one section for each Pod.

B. 8I-080 MICROPROCESSOR POD (Supports Intel 8085, 8035/8039/8040, 8031/8032)

1. PROBE NUMBERS

Data	Probes 0- 7	
Address	Probes 8-23	(8-19 for 8035/8039/8040)
Status	Probes 24-27	
External	Probes 28-31	

2. STATUS CODES

	8085	8035/39/40	8031/32
Fetch (or PSEN)	0011	X011	X011
Memory Read	0010	X010	X010
Memory Write	0001	X001	X001
I/O Read	0110	X1XX	N.A.
I/O Write	0101	X1XX	N.A.
Interrupt Acknowldgment	0111	N.A.	N.A.
Hold Acknowledgment	1XXX	N.A.	N.A.
Bit 24 =	S0	WR or PSEN	WR or PSEN
Bit 25 =	S1	RD or PSEN	RD or PSEN
Bit 26 =	IO/$\overline{M}$	PROG	N.A.
Bit 27 =	HLDA	N.A.	N.A.

3. SWITCH SETTINGS (8031/32 only)

	Down	Up	
Switch 1	Clocks	Doesn't clock	Read (8031)
Switch 2	Clocks	Doesn't clock	Write (8031)
Switch 3			(Unused)
Switch 4			(Unused)

PSEN always clocks Pod.

4. PROBE COLOR CODES FOR EXTERNAL INPUT LINES

Probe No.	Input Wire	Twisted with	Tip Color
28	Beige	Brown (inactive)	Black
29	Red	Beige (inactive)	Brown
30*	Orange	Beige	Red
31*	Beige	Orange	Black

In the Logic Pod probe sets, the beige wire in each twisted pair is always the ground. But in the Microprocessor Pod probe sets, there are no ground wires, and so the beige wire either carries the input or is inactive.

* The wires for Probes 30 and 31 are twisted together (in the same pair).

C. 8M-080 MICROPROCESSOR POD (Supports Motorola 6800, 6802, and 6808)

1. PROBE NUMBERS

Data	Probes 0- 7
Address	Probes 8-23
Status	Probes 24-27
External	Probes 28-31

2. STATUS CODES

Read	01X1
Write	01X0
Halt/bus available	1X0X
Bus available	1XXX
Bit 24 =	$R/\overline{W}$
Bit 25 =	$\overline{HALT}$
Bit 26 =	VMA
Bit 27 =	BA

NOTE: To detect a reversed Pod connection error, the 6800 Pod loads the target processor's VCC pin with 200 ohms to VSS. If this 25-mA load is unacceptable, remove R7 from the Pod's circuit board, or replace R7 with a resistor of a higher value.

3. SWITCH SETTINGS

For proper Pod operation, use the following switch settings. The switches are located on the same side of the Pod as is the auxiliary probe connector, and are labeled 1, 2, 3, and 4. Up (toward the Pod label) is open; down is closed.

	6802 and 6808	6800
Switch 1	Open/Up	Write Clocking: Open/Up--fall of 02 Closed/Down--fall of DBE
Switches 2-4	(Unused--leave open)	(Unused--leave open)

4. PROBE COLOR CODES FOR EXTERNAL INPUT LINES

Probe No.	Input Wire	Twisted with	Tip Color
28	Beige	Brown (inactive)	Black
29	Red	Beige (inactive)	Brown
30*	Orange	Beige	Red
31*	Beige	Orange	Black

In the Logic Pod probe sets, the beige wire in each twisted pair is always the ground. But in the Microprocessor Pod probe sets, there are no ground wires, and so the beige wire either carries the input or is inactive.

* The wires for Probes 30 and 31 are twisted together (in the same pair).

D. 8M-089 MICROPROCESSOR POD (Supports Motorola 6809 and 6809E)

1. PROBE NUMBERS

	6809	6809E
Data	0- 7	0- 7
Address	8-23	8-23
Status	24-27	24-29
External	28-31	30-31

2. STATUS CODES

	6809	6809E
Last Instruction Cycle	N.A.	X1XXXX
Read	00X1	XX00X1
Write	00X0	XX00X0
Interrupt Acknowledgment	01XX	XX01XX
Sync. Acknowledgment	10XX	XX10XX
Bus Grant Due to Halt	110X	XX110X
Bus Grant	11XX	XX11XX
Bit 24 =	R/$\overline{W}$	R/$\overline{W}$
Bit 25 =	$\overline{HALT}$	$\overline{HALT}$
Bit 26 =	BS	BS
Bit 27 =	BA	BA
Bit 28 =	Ext. Lead 0	LIC
Bit 29 =	Ext. Lead 1	AVMA
Bit 30 =	Ext. Lead 2	Ext. Lead 0
Bit 31 =	Ext. Lead 3	Ext. Lead 1

NOTE: To detect a reversed pod connection error, the 6809 Pod loads the target processor's VCC pin with 200 ohms to VSS. If this 25-mA load is unacceptable, remove R7 from the pod's circuit board, or replace R7 with a resistor of a higher value.

3. PROBE COLOR CODES FOR EXTERNAL INPUT LINES

6809 Probe No.	6809E Probe No.	Input Wire	Twisted with	Tip Color
28		Beige	Brown (inactive)	Black
29		Red	Beige (inactive)	Brown
30*	30*	Orange	Beige	Red
31*	31*	Beige	Orange	Black

In the Logic Pod probe sets, the beige wire in each twisted pair is always the ground. But in the Microprocessor Pod probe sets, there are no ground wires, and so the beige wire either carries the input or is inactive.

* The wires for Probes 30 and 31 are twisted together (in the same pair).

E. 8R-065 MICROPROCESSOR POD (Supports Rockwell 6502, 6512, 65C02, 65C102, and 65C112.)

1. PROBE NUMBERS

Data	Probes 0- 7
Address	Probes 8-23
Status	Probes 24-27
External	Probes 28-31

2. STATUS CODES

	6502 & 6512	65C02, 65C102, & 65C112
Fetch	1X11	1X11
Memory Read	0X11	0X11
Memory Write	0XX0	0X10
Set Overflow Bit	X0XX	X0XX
Bit 24 =	$R/\overline{W}$	$R/\overline{W}$
Bit 25 =	RDY	RDY
Bit 26 =	S.O.	S.O.
Bit 27 =	SYNC	SYNC

NOTE: To detect a reversed pod connection error, the 6502 Pod loads the target processor's VCC pin with 220 ohms to VSS. If this 23-mA load is unacceptable, remove R7 from the pod's circuit board, or replace R7 with a resistor of a higher value.

3. SWITCH SETTINGS

For proper Pod operation, use the switch settings below. The switches are located on the same side of the Pod as is the auxiliary probe connector, and are labeled 1, 2, 3, and 4. Up (towards the Pod label) is open; down is closed.

	6502	65C02, 65C102, 65C112	6512
Switch 1	Open/Up	Open/Up	Write Clocking: Open/Up--Use S2 choice Closed/Down--fall of DBE
Switch 2	Open/Up	Open/Up	Read Clocking: Open/Up--fall of Φ2 Closed/Down--Rise of Φ1
Switch 3	Closed/Down	Open/Up	Open/Up
Switch 4	Open/Up	Open/Up	Closed/Down

4. PROBE COLOR CODES FOR EXTERNAL INPUT LINES

Probe No.	Input Wire	Twisted with	Tip Color
28	Beige	Brown (inactive)	Black
29	Red	Beige (inactive)	Brown
30*	Orange	Beige	Red
31*	Beige	Orange	Black

In the Logic Pod probe sets, the beige wire in each twisted pair is always the ground. But in the Microprocessor Pod probe sets, there are no ground wires, and so the beige wire either carries the input or is inactive.

* The wires for Probes 30 and 31 are twisted together (in the same pair).

F. 8Z-080 MICROPROCESSOR POD (Supports Zilog Z80.)

1. PROBE NUMBERS

Data	Probes 0- 7
Address	Probes 8-23
Status	Probes 24-27
External	Probes 28-31

2. STATUS CODES

Fetch	1011
Memory Read	1010
Memory Write	1001
I/O Read	1110
I/O Write	1101
Interrupt Acknowledgment	1111
Bus Acknowledgment	0XXX
Refresh	1000

Bit 24 =	Write or Fetch or Interrupt Acknowledgment
Bit 25 =	Read or Fetch or Interrupt Acknowledgment
Bit 26 =	I/O or Interrupt Acknowledgment
Bit 27 =	$\overline{\text{BUSAK}}$

3. PROBE COLOR CODES FOR EXTERNAL INPUT LINES

Probe No.	Input Wire	Twisted with	Tip Color
28	Beige	Brown (inactive)	Black
29	Red	Beige (inactive)	Brown
30*	Orange	Beige	Red
31*	Beige	Orange	Black

In the Logic Pod probe sets, the beige wire in each twisted pair is always the ground. But in the Microprocessor Pod probe sets, there are no ground wires, and so the beige wire either carries the input or is inactive.

* The wires for Probes 30 and 31 are twisted together (in the same pair).

G. 8N-080 MICROPROCESSOR POD (Supports National Semiconductor NSC-800.)

1. PROBE NUMBERS

Data	Probes 0- 7
Address	Probes 8-23
Status	Probes 24-28
External (3)	Probes 29-31

2 STATUS CODES

Fetch	X1011	
Memory Read	X1010	
Memory Write	X1001	
I/O Read	X1110	
I/O Write	X1101	
Interrupt Acknowledgment	X1111	(Pod's encoding, not microprocessor's)
Bus Acknowledgment	X0XXX	
Refresh	X1100	(Pod's encoding, not microprocessor's)
Halt	X1000	
Processor was reset	1XXXX	

Bit 24 = S0, High for Write or Fetch or Interrupt Acknowledgment

Bit 25 = S1, High for Read or Fetch or Interrupt Acknowledgment

Bit 26 = $IO/\overline{M}$, High for I/O or Interrupt Acknowledgment

Bit 27 = $\overline{BUSAK}$

Bit 28 = Reset: High for each processor cycle during which Reset Out was high, plus one additional cycle

Bit 29 = External Lead 0
Bit 30 = External Lead 1
Bit 31 = External Lead 2

During operation with internal clock (i.e., asynchronous to the microprocessor), only the data lines are totally "transparent". Both address bytes are registered with D-type registers, and change only on the falling edge of ALE. The Status lines, while not registered, are affected by the encoding logic which marks Refresh cycles (if in NSCREF mode) and Interrupt Acknowledgment cycles.

3. PROBE COLOR CODES FOR EXTERNAL INPUT LINES

Probe No.	Input Wire	Twisted with	Tip Color
29	Beige	Brown (inactive)	Black
30	Red	Beige (inactive)	Brown
31	Orange	Beige (inactive)	Red

In the Logic Pod probe sets, the beige wire in each twisted pair is always the ground. But in the Microprocessor Pod probe sets, there are no ground wires, and so the beige wire either carries the input or is inactive.

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