Am6012/6012A • Am6022/6022A

12-Bit High and Ultra-High Speed Multiplying D/A Converters

DISTINCTIVE CHARACTERISTICS

- All grades 12-bit monotonic over temperature
- Differential nonlinearity to ±0.012% (13 bits) max over temperature (A grades)
- Fast settling output current:
  75ns (Am6022/A)
  250ns (Am6012/A)
- Full scale current: 4mA
- High output impedance and compliance: −5 to +10V
- Differential current outputs
- Low cost
- High-speed multiplying capability
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Low power consumption:
  230mW (Am6012/A)
  500mW (Am6022/A)

GENERAL DESCRIPTION

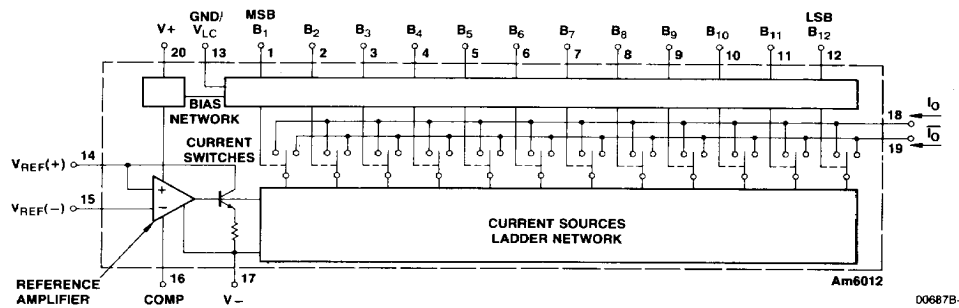
The Am6012/6022 series of 12-bit monolithic multiplying digital-to-analog converters represent new levels of speed, accuracy and low cost. The Am6012 and its high-performance, pin-compatible twin, the Am6022 are the first 12-bit DACs to be built using standard processing without the need for thin-film resistors or active trimming.

The Am6012/6022 design guarantees a more uniform step size than is possible with standard binarily weighted DACs. This ±1/2 LSB differential nonlinearity is desirable in many applications where local linearity is critical. The uniform step size allows finer resolution of levels and in most applications is more useful than conformance to an ideal straight line from zero to full scale.

The Am6012/6022 have high voltage compliance, high impedance dual complementary outputs which increase their versatility and enable differential operation to effectively double the peak to peak output swing. These outputs can be used directly without op amps in many applications. The dual complementary outputs can also be connected in A/D converter applications to present a constant load current and significantly reduce switching transients and increase system throughput. Output full scale current is specified at 4mA, allowing use of smaller load resistors to minimize the output RC delay which usually dominates settling time at the 12-bit level.

The Am6012/6022 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as tight as 0.012% (13 bits), for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range. Device performance is essentially independent of power supply voltage, and devices work over a wide operating range from +5 and, −12V to ±18V.

FUNCTIONAL DIAGRAM



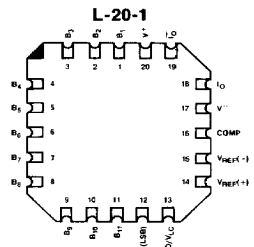
ORDERING INFORMATION

Package Type	Temperature Range	Differential Nonlinearity	Am6012 Order Number	Am6022 Order Number
Ceramic DIP	−55 to +125°C	±0.012%	AM6012ADM	AM6022ADM
Ceramic DIP	−55 to +125°C	±0.025%	AM6012DM	AM6022DM
Ceramic DIP	0 to +70°C	±0.012%	AM6012ADC	Am6022ADC
Ceramic DIP	0 to +70°C	±0.025%	AM6012DC	AM6022DC
Plastic DIP	0 to +70°C	±0.012%	AM6012APC	AM6022APC
Plastic DIP	0 to +70°C	±0.025%	AM6012PC	AM6022PC
Leadless Chip-Carrier	−55 to +125°C	±0.012%	AM6012ALM	AM6022ALM**
Leadless Chip-Carrier	−55 to +125°C	±0.025%	Am6012LM	Am6022LM**
Leadless Chip-Carrier	0 to +70°C	±0.012%	Am6012ALC	Am6022ALC**
Leadless Chip-Carrier	0 to +70°C	±0.025%	Am6012LC	Am6022LC**
Dice	−55 to +125°C	±0.012%	Am6012AXM	Am6022AXM**
Dice	−55 to +125°C	±0.025%	Am6012XM	Am6022XM**
Dice	0 to +70°C	±0.012%	Am6012AXC	Am6022AXC
Dice	0 to +70°C	±0.025%	Am6012XC	Am6022XC

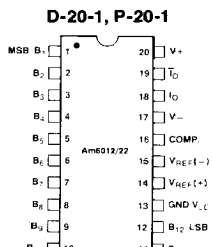
*Also available with burn-in processing. To order, add suffix B to part number.
**To be announced

CONNECTION DIAGRAMS – Top Views

L-20-1



D-20-1, P-20-1



Note: Pin 1 is marked for orientation.

00687B-ANA

Am6012/6012A

MAXIMUM RATINGS (above which useful life may be impaired)

Operating Temperature		Power Supply Voltage	±18V
Am6012ADM, Am6012DM	−55 to +125°C	Logic Inputs	−5 to +18V
Am6012ADC, Am6012DC	0 to +70°C	Analog Current Outputs	−8 to +12V
Storage Temperature	−65 to +125°C	Reference Inputs V_{14}, V_{15}	V− to V+
Lead Temperature (Soldering, 60sec)	300°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
		Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for $V^+ = +15V$, $V^- = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified.

Parameter	Description	Test Conditions	Am6012A Min.	Am6012A Typ.	Am6012A Max.	Am6012 Min.	Am6012 Typ.	Am6012 Max.	Units
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	–	±.05	–	–	±0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohms typ.	−5	–	+10	−5	–	+10	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$	–	±0.2	±1.0	–	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		–	–	0.10	–	–	0.10	μA
t_S	Settling Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	–	250	500	–	250	500	nsec
t_{PLH} t_{PHL}	Propagation Delay − all bits	50% to 50%	–	25	50	–	25	50	nsec
C_{OUT}	Output Capacitance		–	20	–	–	20	–	pF
V_{IL}	Logic Input Levels: Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels: Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current	$V_{IN} = -5$ to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	$V_- = -15V$	−5	–	+18	−5	–	+18	Volts
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +13.5V to +16.5V, V− = −15V	–	±.00005	±.001	–	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		V− = −13.5V to −16.5V, V+ = +15V	–	±.00025	±.001	–	±.00025	±.001	
V+	Power Supply Range	$V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−10.8	−18	–	−10.8	
I+	Power Supply Current	V+ = +5V, V− = −15V	–	5.7	8.5	–	5.7	8.5	mA
I−			–	−13.7	−18.0	–	−13.7	−18.0	
I+		V+ = +15V, V− = −15V		5.7	8.5	–	5.7	8.5	
I−			–	−13.7	−18.0	–	−13.7	−18.0	
P_D	Power Dissipation	V+ = +5V, V− = −15V	–	234	312	–	234	312	mW
		V+ = +15V, V− = −15V	–	291	397	–	291	397	

Am6022/6022A

MAXIMUM RATINGS (above which useful life may be impaired)

Operating Temperature		Power Supply Voltage	±18V
Am6022ADM, Am6022DM	−55 to +125°C	Logic Inputs	−5 to V+
Am6022ADC, Am6022DC	0 to +70°C	Analog Current Outputs	−8 to +12V
Storage Temperature	−65 to +125°C	Reference Inputs V_{14}, V_{15}	V− to V+
Lead Temperature (Soldering, 60sec)	300°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
		Reference Input Current (I_{14})	1.25mA

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ELECTRICAL CHARACTERISTICS

These specifications apply for $V^+ = +15V$, $V^- = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified.

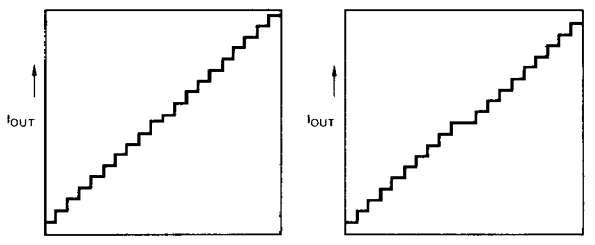
Parameter	Description	Test Conditions	Am6022A Min.	Am6022A Typ.	Am6022A Max.	Am6022 Min.	Am6022 Typ.	Am6022 Max.	Units
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	±0.012	–	–	±0.025	–	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.995	4.063	mA
TCI_{FS}	Full Scale Tempco		–	±5	–			–	ppm/°C
			–	±.0005	–	–	±.00	–	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range R_{OUT} > 10 megohms typ.				5	–	+10	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$	–		–	–	±0.4	–	μA
I_{ZS}	Zero Scale Current			0.10	–	–	0.10	–	μA
t_S	Settling Time	T… LSB, … bits ON o… FF … C	–	75	–	–	75	–	nsec
t_{PLH} t_{PHL}	Propagation Delay – a…	S…	–	10	–	–	10	–	nsec
C_{OUT}	…tput …		–	10	–	–	10	–	pF
V_{IL}	Logic …	Logic "0"	–	–	0.8	–	–	0.8	Volts
V_{IH}	L… ls	Logic "1"	2.0	–	–	2.0	–	–	
I_{IN}	Lo… Input Current	$V_{IN} = -5$ to $+15$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+15	−5	–	+15	Volts
I_{REF}	Reference Current Range	$V_{REF(-)} = 0V$	0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = 0pF	–	16.0	–		16.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +13.5V to +16.5V, V− = −15V	–	±.00005		–	±0.0005		%FS/%
$PSSI_{FS-}$		V− = −13.5V to −16.5V, V+ = +15V	–	±.00025		–	±.00025		
V+	Power Supply Range	$V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−10.8	−18	–	−10.8	
I+	Power Supply Current	V+ = +5V, V− = −15V	–	11	–	–	11	–	mA
I−			–	−24	–	–	−24	–	
I+		V+ = +15V, V− = −15V		13.0	–	–	13.0	–	
I−			–	−24	–	–	−24	–	
P_D	Power Dissipation	V+ = +5V, V− = −15V	–	415	–	–	415	–	mW
		V+ = +15V, V− = −15V	–	555	–	–	555	–	

ACCURACY SPECIFICATIONS

The design of the 6012/22 emphasizes differential linearity which is a measure of the uniformity of each step in the transfer characteristic. The circuit design, described in greater detail on page 6, requires resistor matching and tracking tolerances of 8 times lower than that of previous designs to achieve and maintain monotonicity over temperature. This advantage has been used in the 6012A/22A to provide 13-bit differential nonlinearity over temperature, a level of performance not generally available in previous designs, even when using thin film resistors.

The figures illustrate that ±1/2 LSB (13-bit) differential nonlinearity guarantees a converter with 4096 distinct output levels. ±1 LSB D.N.L. guarantees monotonicity, so that when the input code is increased the output will not decrease. Note that nonlinearity, or deviation from an ideal straight line through zero and full scale, cannot be visually determined from the figures. In most applications, 12-bit resolution and differential linearity are more important than linearity. This is especially true in video and graphics, where the human eye has difficulty discerning nonlinearity of less than 5%.

DIFFERENTIAL NONLINEARITY
WORST CASE AT TEMPERATURE EXTREME



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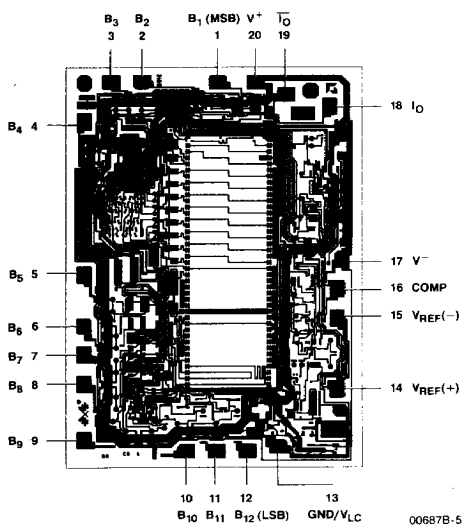
METALLIZATION AND PAD LAYOUT

Am6012



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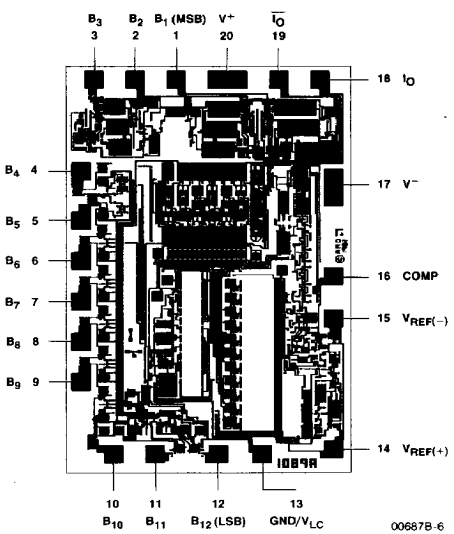
Am6022



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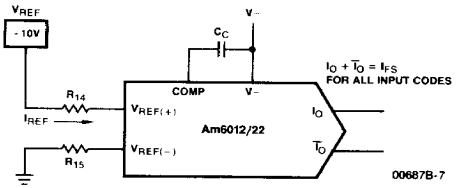
DIE SIZE 0.093" X 0.134"

APPLICATION HINTS:

1. Reference current and reference resistor.

There is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$



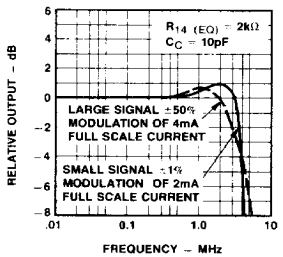
2. Reference amplifier compensation. (Am6012)

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

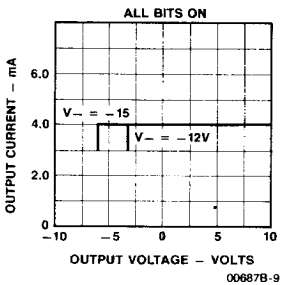
MINIMUM SIZE COMPENSATION CAPACITOR (I_{FS} = 4mA, I_{REF} = 1.0mA)

R_{14} (EQ) (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response

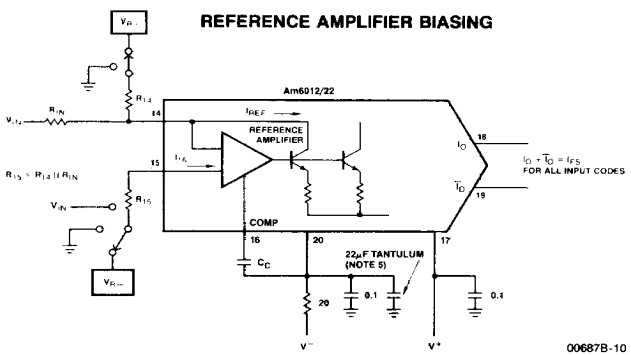


Output Voltage Compliance



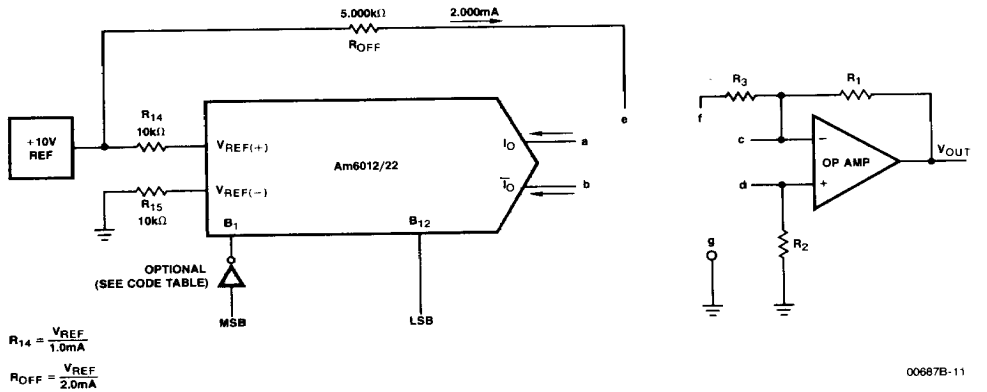
Note: A 0.01μF capacitor is recommended for fixed reference operation.

REFERENCE AMPLIFIER BIASING



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1) Am6012	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1) Am6012	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $C = 5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V– with 20Ω and bypass with 22μF tantulum capacitor.



CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
UNIPOLAR	Straight binary; one polarity with true input code, true zero output.	a-c b-g R1 = R2 = 2.5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a-g b-c R1 = R2 = 2.5K	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
			Positive full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
			Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
SYM-METRICAL OFFSET	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
	s complement; o et half scale, symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
OFFSET WITH TRUE ZERO	Offset binary; offset half scale, true zero output.	e-a-c b-g R1 = R2 = 5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			− LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000
	2's complement; offset half scale true zero output MSB complemented (need inverter at B1).	e-a-c b-g R1 = R2 = 5K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

SEGMENTED DAC DESIGN INFORMATION

The design of a 12-bit D/A converter has traditionally required precision thin film resistors, a trimming method, and a binarily weighted ladder network. The 6012/22 is a 12-bit DAC which uses diffused resistors and requires no trimming, cutting, blowing, or zapping to guarantee monotonicity for all grades over the temperature range. A proprietary design technique, departing from the traditional R-2R approach used in virtually all high speed high resolution converters, provides inherent monotonicity and differential linearity as high as 13 bits. This guarantees a more uniform step size over the temperature range than available trimmed 12-bit converters. The converter's performance is immune to variations in temperature, time, process, and mechanical stress. The circuit also features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In most converter applications, uniform step size is more important than conformance to an ideal straight line. Most 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±1/2 LSB (±.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. This new circuit uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current switched R-2R DAC since it is slower, has a voltage output, and if implemented at the 12-bit level would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

The technique used in the Am6012 combines the advantages of both the R-2R and 2^nR approaches. It is inherently monotonic, fast, and uses untrimmed resistors which are actually fewer in number than the classic R-2R ladder.

In order to properly describe the new design technique, the standard R-2R ladder approach used in previous 12-bit DAC's will first be discussed. Figure 1 shows the twelve-bit currents which are used in all possible binary combinations to generate 4096 analog output levels. The resistor ladder tolerance is most critical for the major carry, where the 11 least significant bits turn off and the most significant bit turns on. If the MSB is more than 1μA low, or −.05%, the converter will be nonmonotonic. Table 1 shows the maximum tracking error which can be allowed over a 100°C range to maintain monotonicity, which is ±1 LSB D.N.L. Achieving ±1/2 LSB differential nonlinearity is especially difficult since it requires a tracking temperature coefficient of ±1.25 ppm/°C.

Figure 2 shows the transfer characteristic for the new technique, called the segmented DAC. The 4096 output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources, as shown in Figure 3. The resistors which determine monotonocity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

At each segment endpoint, monotonicity is assured because no critical resistor tolerances are involved. For example, at the midpoint of the transfer characteristic, as shown in Figure 2, $I_{4,0}$ is actually generated by the same segment resistor as $I_{3,511}$ and has been incremented by the remainder current of the 9-bit DAC.

In the segmented DAC, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high speed fully differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long term characteristics are not degraded.

TABLE 1
RESISTOR SPECIFICATIONS

Ladder Type	No. of Resistors	Initial Matching Required for ±1 LSB DNL (%)	Tracking Required for ±1 LSB DNL (ppm/°C)		Tracking Req'd. for ±1/2 LSB DNL (ppm/°C)
			0 Initial DNL	1/2 LSB Initial DNL	1/4 LSB Initial DNL
Straight R-2R	37	±.05	5	2.5	1.25
Segmented 3 Bits + 9 Bits	24	±.4	40	20	10

Figure 1. Traditional R-2R D/A Converter.

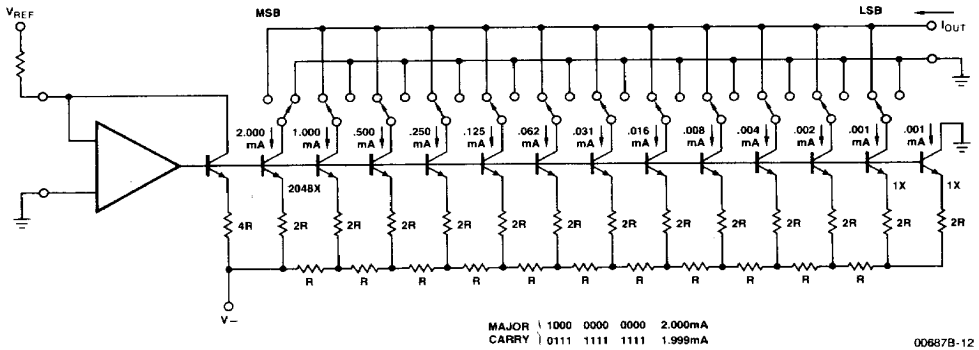


Figure 2. Transfer Characteristic of Segmented Design.

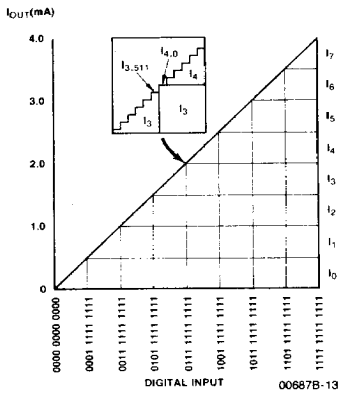


Figure 3. Segmented DAC Functional Diagram Used in Am6012/22.

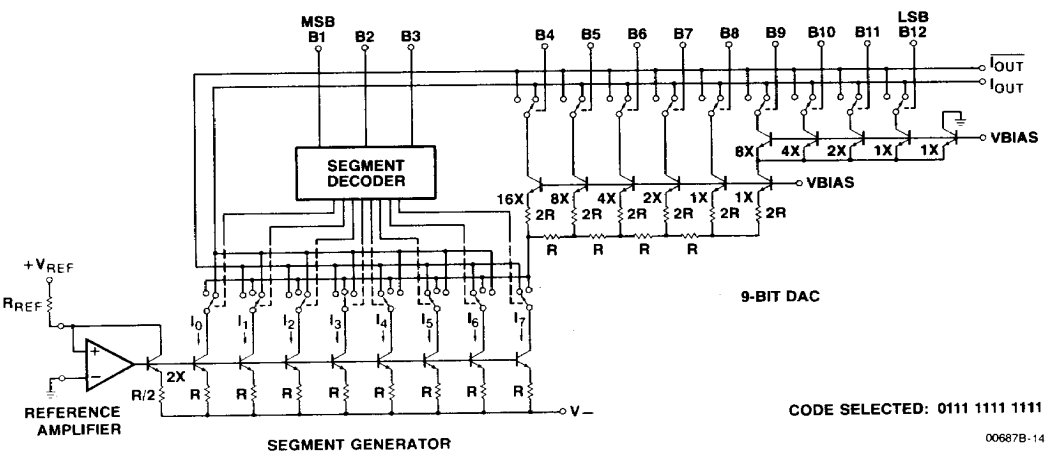
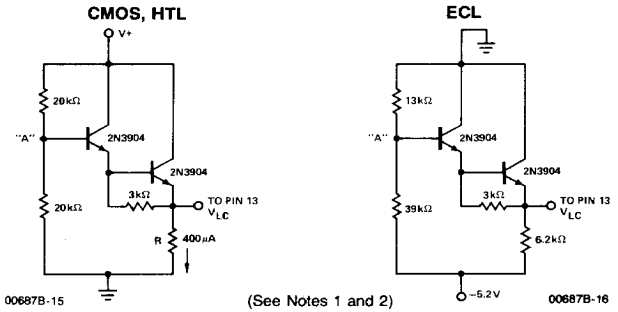
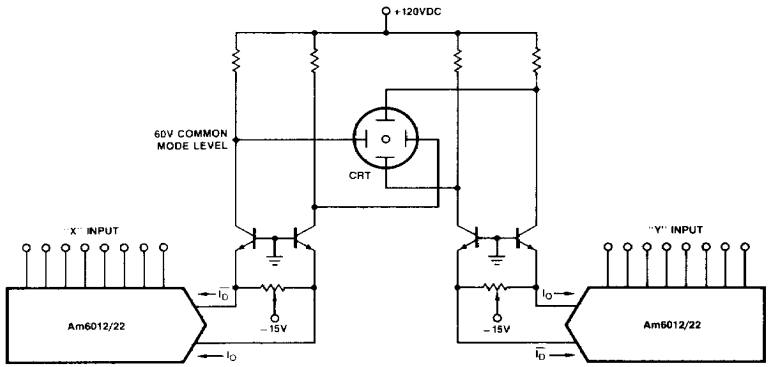


Figure 4. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs.



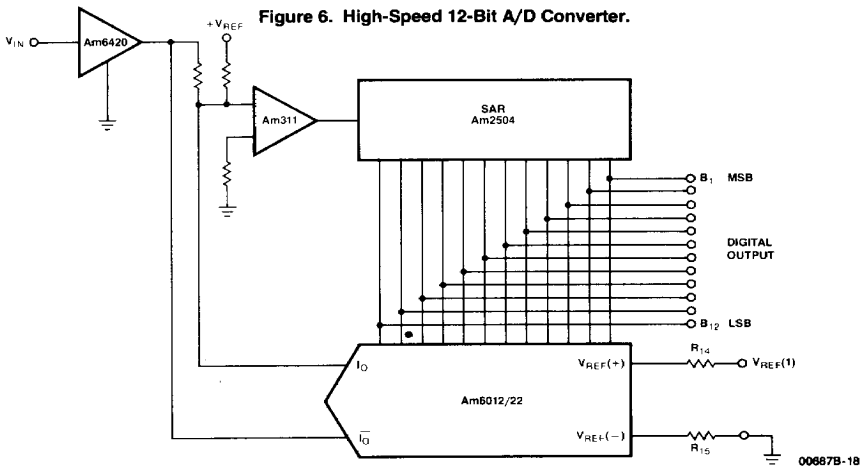
Notes:
1. Set the voltage "A" to the desired logic input switching theshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the DAC on ±15V supplies.

Figure 5. CRT Display Driver.



Notes: 1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Figure 6. High-Speed 12-Bit A/D Converter.



Am6012
12-Bit High-Speed DAC

By Brian Gillings
Advanced Micro Devices

00165A-ANA

INTRODUCTION

Advanced Micro Devices' Am6012 is the first 12-bit DAC ever built using standard processing without the requirements of thin film resistors and/or active trimming of individual devices. The result is a high-speed and high-accuracy converter with low cost. Offering a ±½ least significant bit (LSB) differential nonlinearity, the Am6012's uniform step size allows finer resolution of levels, and in most applications is more useful than conformance to an ideal straight line from zero to full scale.

DESCRIPTION OF THE Am6012

Figure 1 shows a simplified schematic for a traditional R-2R D/A converter used in previous 12-bit DACs. Twelve current sources are used in all possible binary combinations to generate the 4096 analog output levels. The resistor ladder tolerance is most critical at the major carry where the 11 least significant bits are turned off and the most significant bit (MSB) turns on. If the MSB is more than −0.05% low, the converter will be nonmonotonic. Achieving the initial resistor matching for ±1LSB differential nonlinearity (±0.05%) has required precision resistors plus some sort of trimming method, such as laser trimming, cutting, blowing or zapping to guarantee monotonicity for all grades over the temperature range. The Am6012 uses a proprietary design technique, departing from the traditional R-2R design, which offers inherent monotonicity and differential nonlinearity as high as 13 bits (0.012%). The performance of the converter is immune to variations in temperature, time, process and mechanical stress.

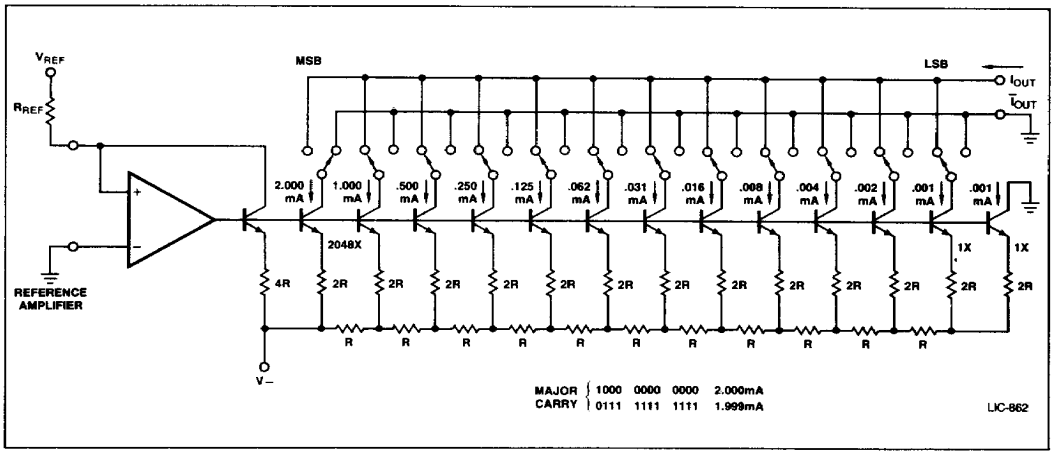


Figure 1. Traditional R-2R D/A Converter

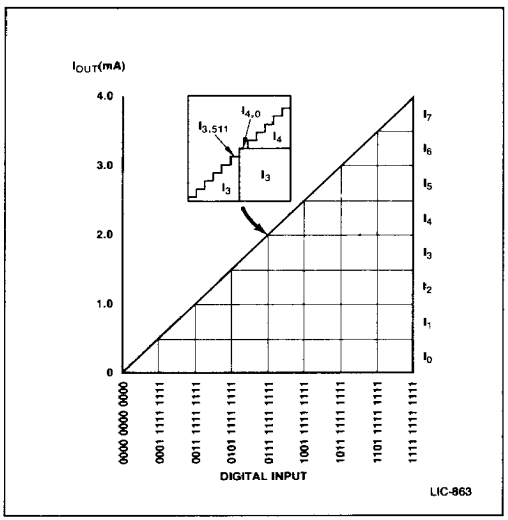


Figure 2. Transfer Characteristic of Segmented Design

Figure 2 shows the transfer characteristic for the new technique called a segmented ladder used in the Am6012. The 4096 output levels are composed of eight groups of 512 steps each.

Each step of the group is generated by a 9-bit DAC and each of the segment slopes is determined by one of eight equal current sources as shown in Figure 3. The resistors that determine monotonicity are in the 9-bit DAC, and the major carry of the 9-bit DAC is repeated in each of the eight segments. This results in the need for eight times lower initial resistor accuracy and provides tracking to maintain a given differential nonlinearity over temperature.

If we assume that the input code is all ZEROES, the first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output I_{OUT}. An increasing digital input code selects a new segment for every 512 counts. The previous segment is fed to output I_{OUT} where the new group is added to it, thus ensuring monotonicity independent of segment resistor values.

In the segment DAC, the precision of the eight main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in a R-2R DAC. Thus, if the resistor tolerances were the same, then the segmented approach would actually be higher in linearity than that of the R-2R design.

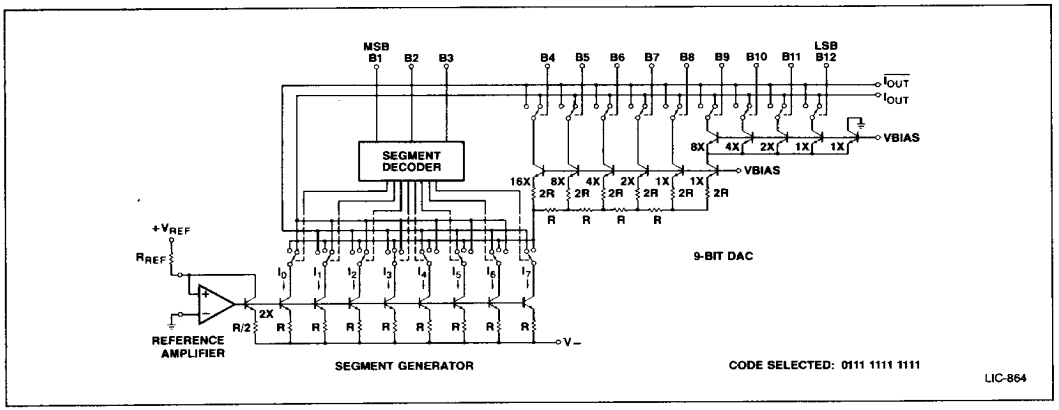


Figure 3. Segmented DAC Functional Diagram Used in Am6012

The 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by using scaled emitters to split the current actively. All of the current switches in the step generator are fully differential switches capable of switching low currents at high speed. This allows the use of a binarily scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Like other monolithic DACs, the Am6012 has two types of errors that cannot be eliminated by adjustment. They are integral nonlinearity and differential nonlinearity. The integral nonlinearity shown in Figure 4 is the maximum deviation of the transfer function from the straight line drawn from actual zero through the full-scale output of the converter. Integral nonlinearity is expressed in LSBs or as a percentage of full-scale. Some products use the "best fit" straight line and specify the deviation in LSBs, however, this straight line will usually not terminate at the full-scale value. The user then must adjust his converter to this full-scale value, but is then unable to calibrate the converter to benefit from the better value offered by this specmanship. Most users are interested in the absolute value of the full-scale output and can calibrate it either manually or automatically.

Differential nonlinearity (DNL) is a measure of the deviation of each individual step size from the ideal least significant bit. A DNL of more than 1LSB defines nonmonotonicity, and a perfect converter has a zero DNL.

The Am6012A is specified as having 13 bits of DNL over temperature, a level of performance generally not available in other 12-bit converters even when using thin film resistors. This ±½LSB (13-bit) DNL guarantees the converter has 4096 separate and distinct output levels, whereas a ±1LSB DNL only guarantees monotonicity. It must be stressed again that these DNL figures are guaranteed over the complete temperature range. Also, DNL gives a measure of curve smoothness. The DAC transfer function may be more than 1LSB nonlinear and yet be smooth and useful with ½LSB DNL. This is especially true in video and graphics where the human eye has difficulty discerning nonlinearity of less than 5%. In most applications, 12-bit resolution and DNL are more important than integral nonlinearity. Figure 5 shows the nonlinearity of an actual device.

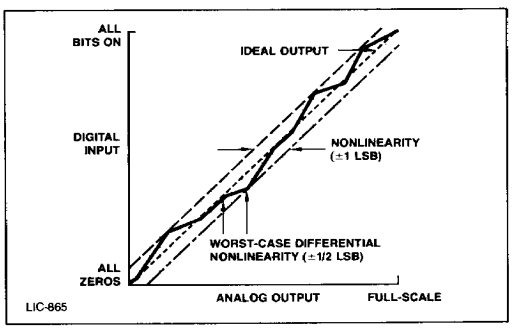


Figure 4. Monotonic DAC with ±1 LSB Nonlinearity and ±1/2 LSB Differential Nonlinearity

MULTIPLYING DAC

The Am6012 uses a fixed reference for most applications, but it can also handle an AC reference source. The output current I_{OUT} is a product of the digital input and analog reference voltage (V_{REF}) or current (I_{REF}).

The output current for current reference can be expressed as:

$$I_O = 4 \cdot I_{REF}\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \frac{B_4}{16} + \frac{B_5}{32} + \frac{B_6}{64} + \frac{B_7}{128} + \frac{B_8}{256} + \frac{B_9}{512} + \frac{B_{10}}{1024} + \frac{B_{11}}{2048} + \frac{B_{12}}{4096}\right)$$

where B_1 is MSB.

The Am6012 has complementary/differential current outputs. The complement of I_O is expressed as:

$$\overline{I_O} = I_{FS} - I_O$$

where the addition of I_O and $\overline{I_O}$ is a constant regardless of the digital code.

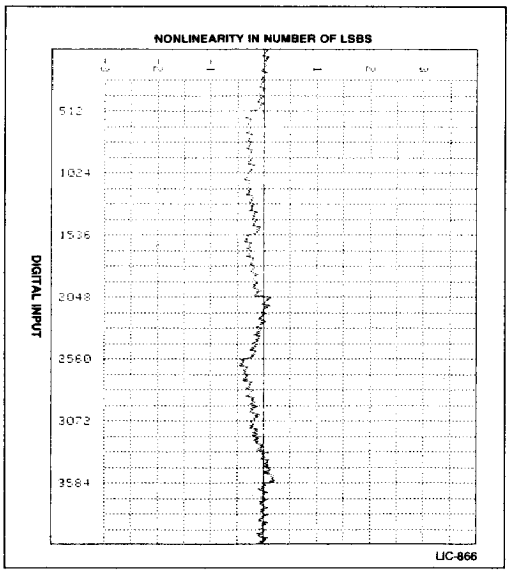


Figure 5. Nonlinearity Plot of Actual Device

Figures 6 and 7 show the relationship of I_{REF} to I_O and $\overline{I_O}$ for the basic DC connections. The reference may be positive or negative, and a bipolar output voltage may be obtained using the high-compliance current outputs alone or with an output op-amp, as described later.

An application of the external positive reference voltage ($+V_{REF}$) forces current through a reference resistor (R_{REF}) into the reference input ($V_{REF(+)}$), which is a virtual ground created by the reference amplifier feedback loop. Reference current (I_{REF}) is defined as:

$$I_{REF} = \frac{+V_{REF}}{R_{REF}}$$

A +10V supply for $+V_{REF}$ is recommended for optimum full-scale temperature operation. Resistor R_{15} minimizes the temperature coefficient of output offset voltage of the reference amplifier by matching it to R_{14}.

In negative reference applications, the external negative reference voltage is applied to the negative reference input ($V_{REF(-)}$) of the Am6012. The voltage at ($V_{REF(+)}$) pin tracks the voltage at ($V_{REF(-)}$). I_{REF} flows from ground through R_{REF} into the ($V_{REF(+)}$) input.

This connection produces high impedance at the ($V_{REF(-)}$) input, thus isolating the signal source from the load. Again, R_{15} is normally used to cancel input bias current errors and is nominally equal to R_{REF}.

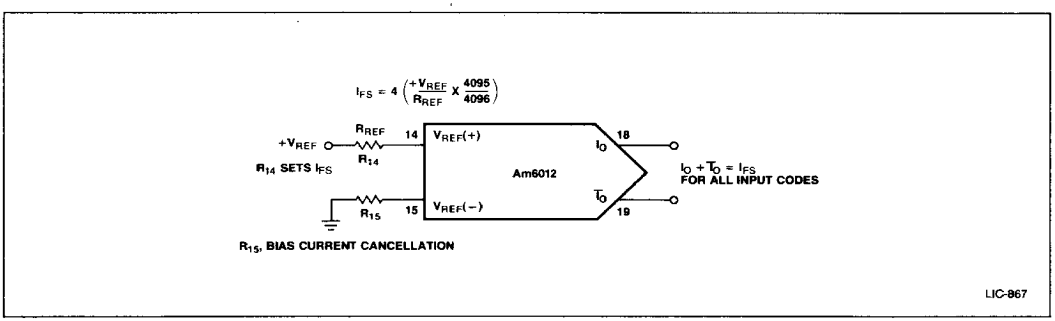


Figure 6. Positive Reference Connection

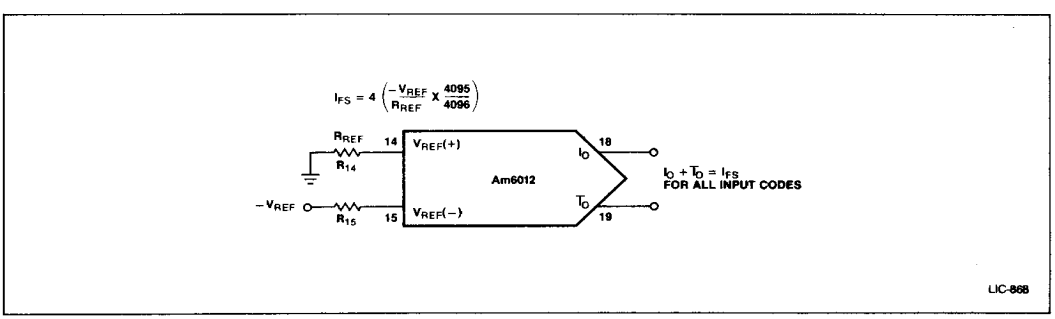


Figure 7. Negative Reference Connection

BIPOLAR OPERATION

Figure 8 shows a low input impedance bipolar connection. The current into ($V_{REF(+)}$) is I_{REF} plus I_{IN}. I_{REF} must be equal to or greater than the maximum negative value of I_{IN}, so the reference amplifier will not turn off. For a high-impedance connection (Figure 9) I_{REF} is calculated from:

$$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$$

where $+V_{REF}$ must be equal to or greater than the maximum positive value of V_{IN}. The I_{REF} current range is set at a minimum of 0.2mA and a maximum of 1.1mA. Fifty percent modulation is recommended to maintain speed and linearity (0.55mA ±0.5mA) over commercial temperature range.

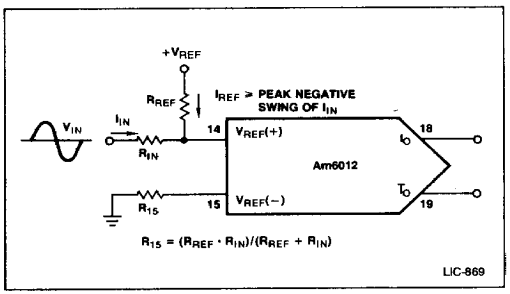


Figure 8. Low Input Impedance Bipolar Reference

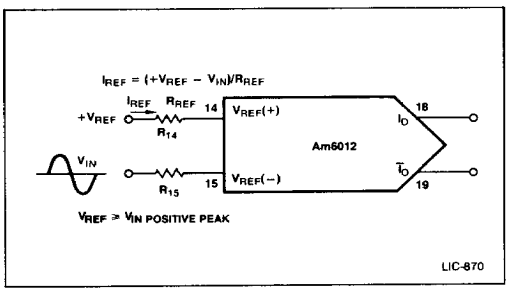


Figure 9. High-Input Impedance Bipolar Reference

REFERENCE AMPLIFIER COMPENSATION

For AC reference applications, a minimum-value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance seen at ($V_{REF(+)}$). Table 1 gives the compensation capacitors required for different values of R_{REF}; and Figure 10 shows the frequency response of the reference amplifier with R_{REF} = 2K and C_C = 10pF.

For the fastest response to a pulse, low values of R_{REF} should be used resulting in a low C_C value. When R_{REF} is 800 ohms, C_C is not required and a full-scale transition of 1μsec maximum and 500nsec typical is obtained. For fixed reference operation a 0.01μF capacitor should be used.

AC COUPLED MULTIPLICATION

Sometimes multiplying applications are more easily achieved by AC coupling, and a high impedance input is often required to avoid loading the high source impedance. Figure 11 uses the

TABLE 1. MINIMUM SIZE COMPENSATION CAPACITOR

(I_{FS} = 4mA, I_{REF} = 1.0mA)

R_{14} (EQ) (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

C_C pin as the input. This is possible because the C_C connection is $2V_{BE}$ away from the ladder determining resistors internal to the Am6012 and gives wider bandwidth than using the reference amplifier.

VOLTAGE OUTPUTS USING Am6012

The settling time for the Am6012 is specified for the current mode or the fastest operating mode. Many DAC applications require a current-to-voltage conversion. This can be achieved simply by connecting a low-value resistor directly to the output. If the output current is 4mA, a unipolar output would limit the resistor value to 1.25K ohms to ground because of the −5V DAC output voltage compliance limitation. The output settling time is determined by the RC time constant produced by the DAC output capacitance of 20pF (plus stray capacitance) and the value of the load resistor. Settling to 0.01% (±½LSB) of full-scale would require approximately 300nsec, or nine time constants. An operational amplifier

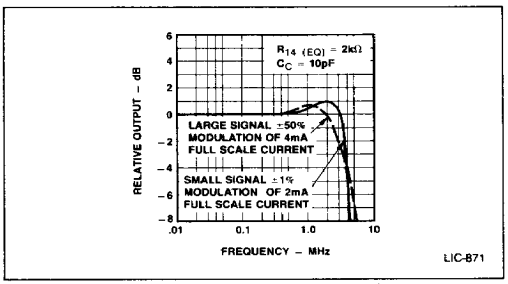


Figure 10. Reference Amplifier Frequency Response

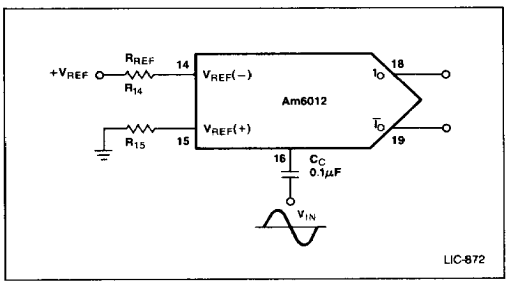


Figure 11. High-Impedance AC-Coupled Multiplication

is required if lower output impedance or larger output swings are desired, but some settling time will be lost because the output response is limited by the amplifier's slew rate and settling time. A feedback capacitor C_f (Figure 12) can compensate for the pole produced by the DAC output capacitance, op-amp input capacitance and the feedback resistor. Careful selection of this capacitor also optimizes the response time. Fastest operation is achieved by minimizing lead lengths, impedances and stray capacitances and bypassing the supplies to the DAC and operational amplifier.

The Am6012 has a maximum zero scale current of 0.1μA over the full temperature range. This represents only 1/10LSB zero offset error. Therefore, the only error that needs to be corrected will be the operational amplifier offset voltage. A typical amplifier, such as the LF156, has an offset voltage (V_{OS}) of 13mV over temperature and 0.5μV/°C per mV change in average temperature coefficient with V_{OS} adjusted to zero. This will produce a total error of 1LSB over temperature, whereas if the LF156A were used only ¼LSB error would occur. In Figure 13 the V_{OS} of the amplifier should be adjusted to zero with all of the bits turned OFF. One LSB is equal to 10/4096V = 2.44mV.

UNIPOLAR OPERATION (Figure 13)

Gain adjustment

Turn all the bits ON and adjust gain trimmer R_1 until the output is 9.9976V. This represents 1LSB less than the nominal 10V full-scale because the DAC outputs 4096 levels including zero so V_{FS} = 4095/4096 (10V) = 9.9976V.

BIPOLAR OPERATION (Figure 14)

This configuration will provide a bipolar output voltage from −10.000V to 9.9951V for an offset binary digital input code.

Offset Adjustment

With all bits OFF, adjust offset trimmer R_2 to give −10.000V at the output.

Gain

Turn all the bits ON, and adjust gain trimmer R_1 to give an output voltage of 9.9951V.

By using Figure 15 and Table 2, different input code formats and output polarities can be accommodated.

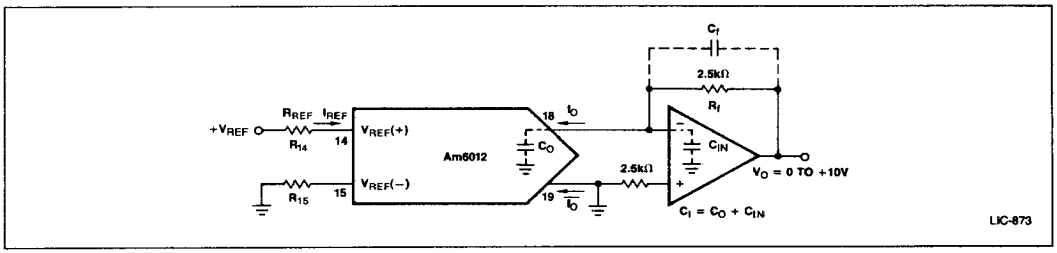


Figure 12. Voltage Output DAC

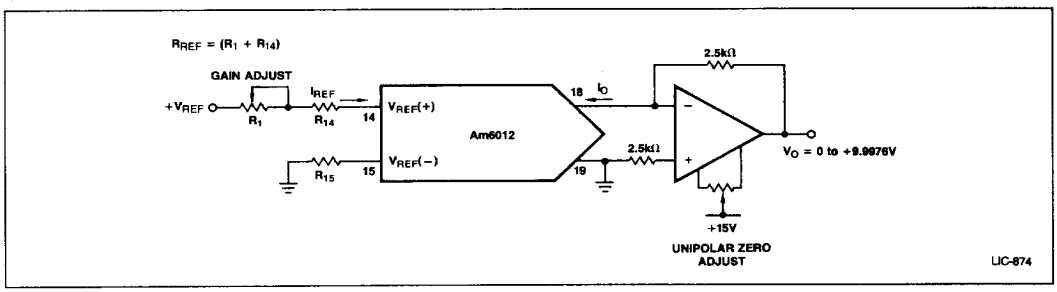


Figure 13. +10V Full-Scale Unipolar DAC

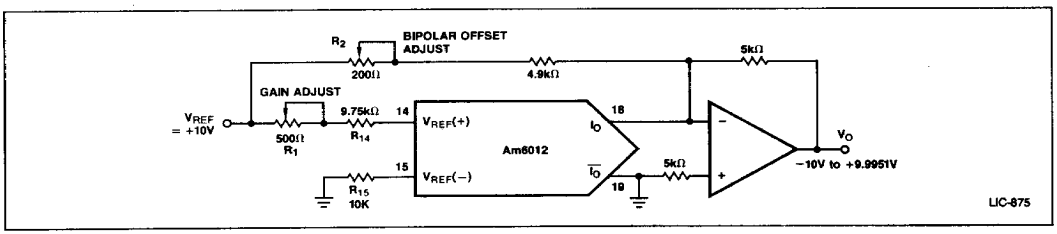


Figure 14. ±10V Full-Scale Bipolar DAC

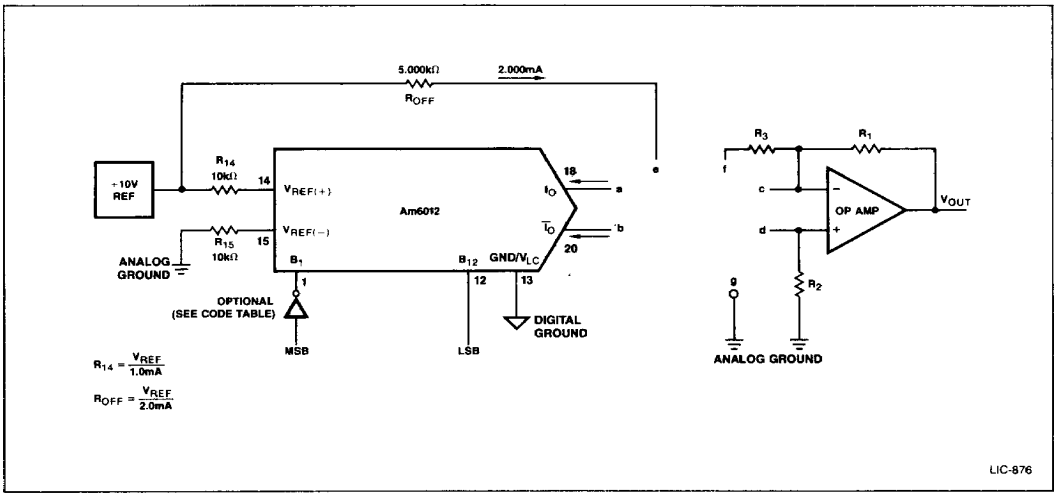


Figure 15. Voltage Output Connection

TABLE 2. INPUT CODE FORMATS

CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
UNIPOLAR	Straight binary; one polarity with true input code, true zero output.	a-c b-g R1 = R2 = 2.5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a-g b-c R1 = R2 = 2.5K	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
			Positive full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
			Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
SYM-METRICAL OFFSET	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
	1's complement; offset half scale, symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
OFFSET WITH TRUE ZERO	Offset binary; offset half scale, true zero output.	e-a-c b-g R1 = R2 = 5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			− LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000
	2's complement; offset half scale true zero output MSB complemented (need inverter at B1).	e-a-c b-g R1 = R2 = 5K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000

TWO-QUADRANT MULTIPLICATION DAC

There are two types of two-quadrant multiplication: bipolar digital, where the digital code controls the output polarity; and bipolar analog, where the analog reference input controls output polarity.

Figure 14 shows a bipolar digital two-quadrant multiplication with the output polarity controlled by an offset binary-coded input word. Two DACs are required for the bipolar analog method (Figure 16) because the Am6012 reference input cannot reverse the output polarity. A bipolar reference voltage is connected to the upper Am6012 and modulates the reference current by ±0.5mA around the quiescent current of 0.55mA. The lower Am6012 also has a reference current of 0.55mA, and both DACs have the same digital inputs. The lower Am6012 effectively subtracts out the quiescent 0.55mA of the upper Am6012 reference current at all digital input codes by differentially connecting them to an op-amp, thus the output voltage, V_{OUT}, is a product of a digital input code and a bipolar analog reference voltage.

FOUR-QUADRANT MULTIPLICATION

By combining bipolar digital and bipolar analog (two-quadrant multiplication) the output analog polarity is controlled by the analog reference input or by the offset binary digital input code. In Figure 17 two Am6012s are connected to implement a four-quadrant multiplying DAC. The circuit shows that a differential input signal can be accepted and differential output currents produced that can either be connected differentially to an op-amp to produce a voltage output or be used to drive balanced loads such as transformers, transducers and transmission lines.

USING THE Am6012 IN A/D CONVERTERS

Successive approximation is probably the method most widely used for implementing an ADC offering relatively fast conversion times with a low component count. Requiring 'n' comparisons for an 'n' bit conversion makes the technique capable of high speed.

As illustrated in Figure 18, the most significant bit is turned ON first, and the DAC output is compared with the input. The bit is switched OFF or left ON, depending upon whether the input signal is smaller or larger than the DAC output signal. The remaining bits are successively switched ON and comparisons made until all respective bits are either left ON or switched OFF. Each time one bit is tried, the DAC is required to settle to within ±½LSB. The Am2504 Successive Approximation Register (SAR) contains the necessary A/D logic, and the timing diagram (Figure 19) relates to the Am2504. Holding the start input LOW for at least one clock period initiates the conversion. The MSB is set LOW and all of the other bits are set HIGH for the first trial. Each trial takes one clock period, proceeding from the most significant to the least.

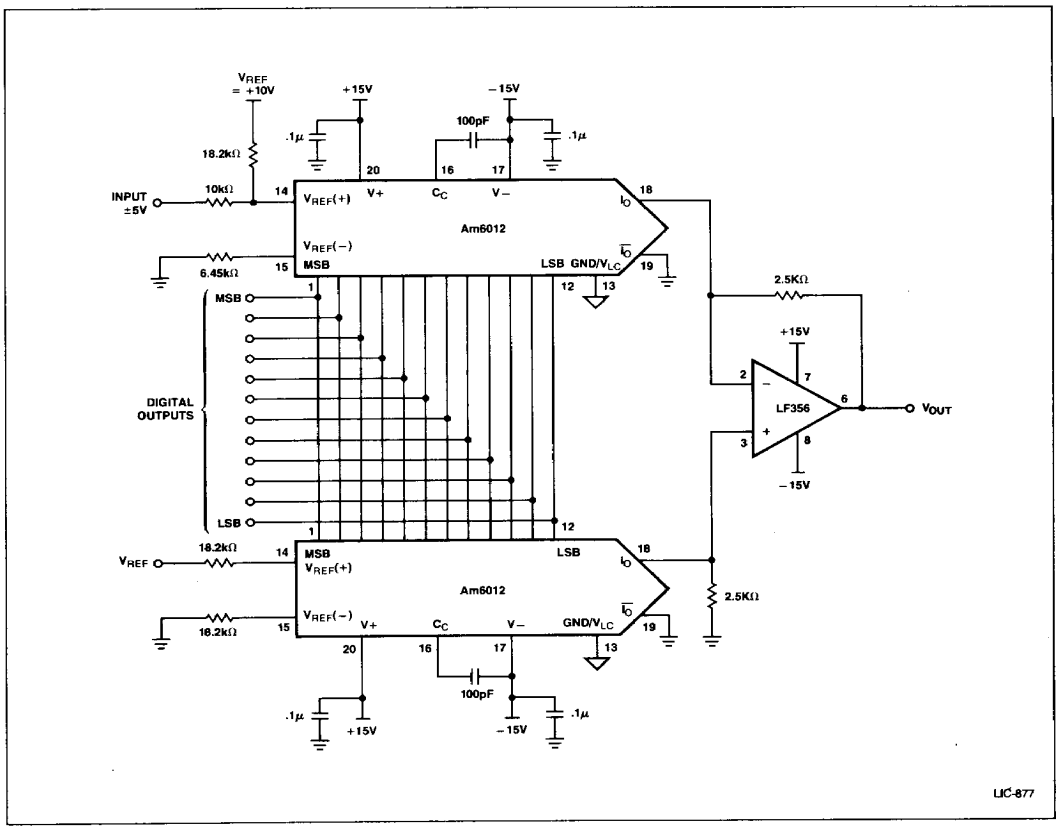


Figure 16. Bipolar Analog Two-Quadrant Multiplication

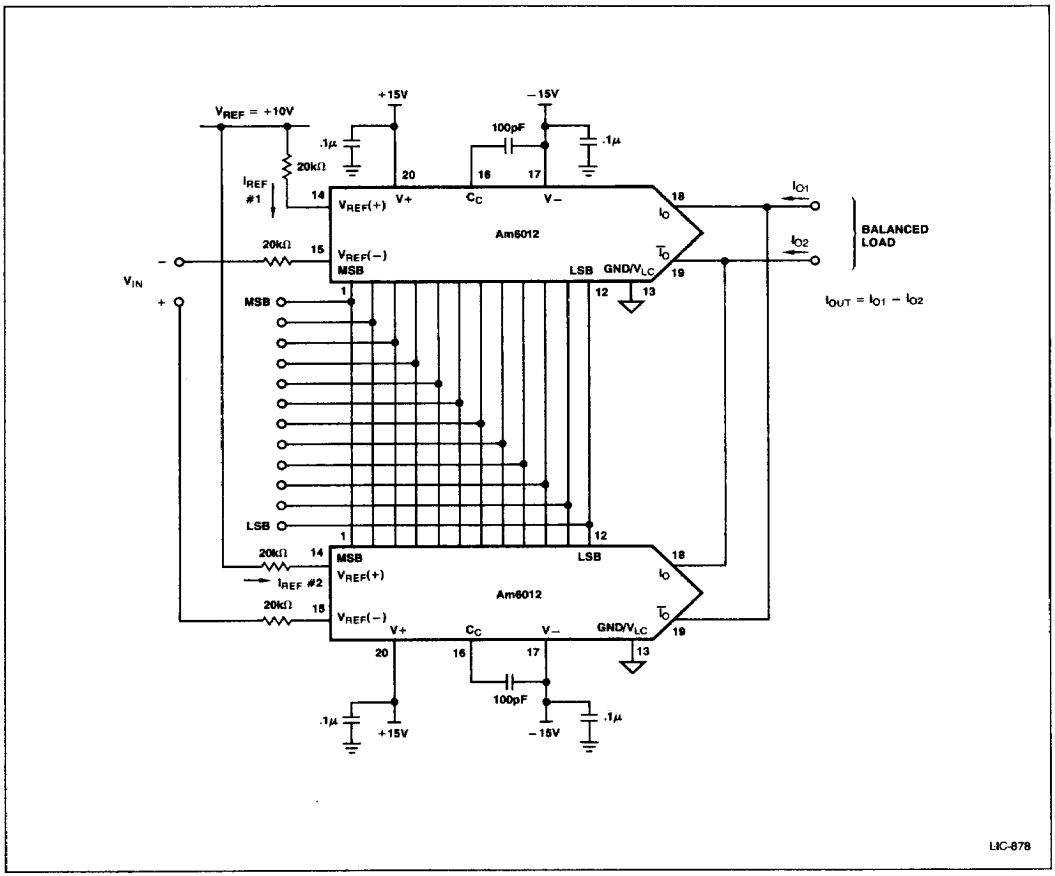


Figure 17. Four-Quadrant Multiplication with High Impedance Input

The time required to complete a 12-bit successive approximation A/D conversion is determined by adding the duration of the 12 trials, the comparator decision delays and one clock cycle. Three dynamic considerations must be taken into account: DAC output current settling time to ±½LSB, the comparator propagation delay, and the SAR propagation delay and setup requirements.

For example, with 300nsec allowed for the DAC to settle to ±½LSB, and 300nsec for the comparator response time plus 50nsec SAR logic delay a complete conversion could result in 8.5μsec.

A major factor affecting the settling time of the DAC is the RC time constant formed by the input resistor (R_{IN}) and the DAC output capacitance (C_O) plus any stray capacitance present at the summing node. The settling to within ±½LSB at 12 bits (±0.01%) requires 9.2 RC time constants. Thus the Am6012, with an output capacitance of 20pF, would influence the settling time if R_{IN} were around 300 ohms. But R_{IN} would become the dominant factor when greater than 500 ohms. Hence, if the A/D full-scale range were 10V and the DAC current was 4mA, then R_{IN} would be equal to 2.5K, resulting in a time constant of 50nsec and a settling time of approximately 500nsec. Lowering the effective resistance at the summing node is a compromise between DAC settling time and comparator overdrive because the ½LSB current is only 0.5μA and, for an equivalent resistance of 500 ohms, would only result in a DAC output voltage corresponding to ½LSB or 0.25mV, which is inadequate for most comparators. With R_{IN} of 2.5K this would result in ½LSB of 1.25mV, which is an adequate overdrive for the Am111s (Figure 18), producing a response time of 200nsec. The propagation delay of the SAR is 50nsec. Hence, the total conversion time is 11.5μsec for a full-scale signal range of 10V.

The input impedance of an ADC changes during the conversion process and can alter the performance of the input amplifier, or sample and hold amplifier if used. Because the comparison point can swing by a large amount, the input current can be modulated. The output impedance of the input amplifier is made LOW by the loop gain of the feedback amplifier. This gain reduces at high frequencies, and the output impedance rises to its open loop value, which is usually between 10 and 200 ohms.

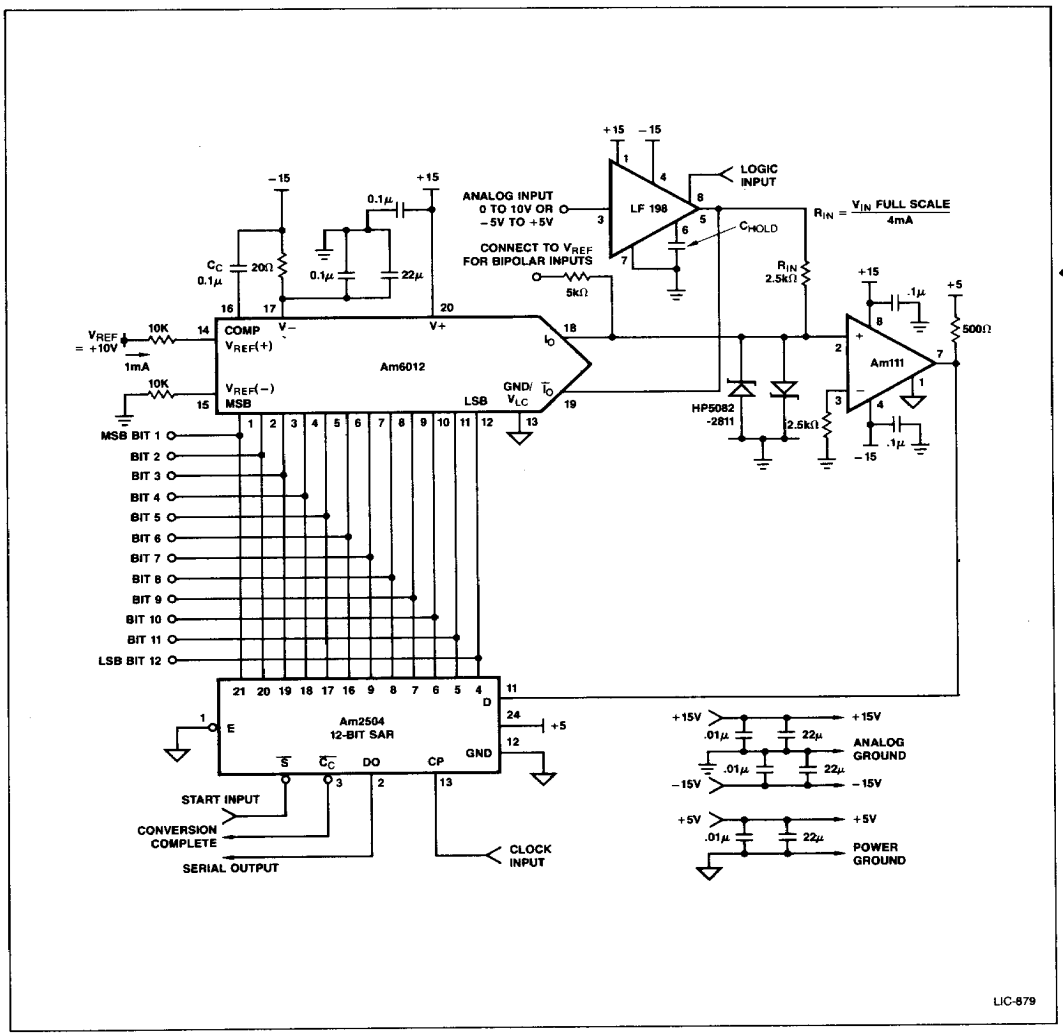


Figure 18. Fast Precision Successive Approximation A/D Converter

Errors can be introduced into the instantaneous input voltage if the bandwidth of the amplifier is not sufficient and the output of the input amplifier does not return to its normal voltage before the converter makes a comparison. The Am6012 offers dual complementary outputs that can present a constant load current to the input signal significantly reducing switching transients and increasing system throughput. Because the full-scale output current of the Am6012 is 4mA, smaller load resistors can be used. These minimize the output RC delay that usually dominates the settling time for a 12-bit ADC. In the design of high-resolution, high-speed ADCs, one must ensure that the analog wiring be kept as short as possible and be separated from the vicinity of digital lines. This precaution refers especially to the comparator output which can capacitively couple edge transients back to the input of the comparator and cause the comparator to oscillate.

Digital ground and analog ground should only meet at one point to prevent digital ground currents from creating voltage errors in the analog ground.

Ground loops should also be avoided within the analog sections since they can introduce errors. Adequately bypassing supplies is essential for high-speed and high-resolution ADCs and should include high-frequency ceramic as well as tantalum capacitors to decouple the high-frequency components of the digital switching transients.

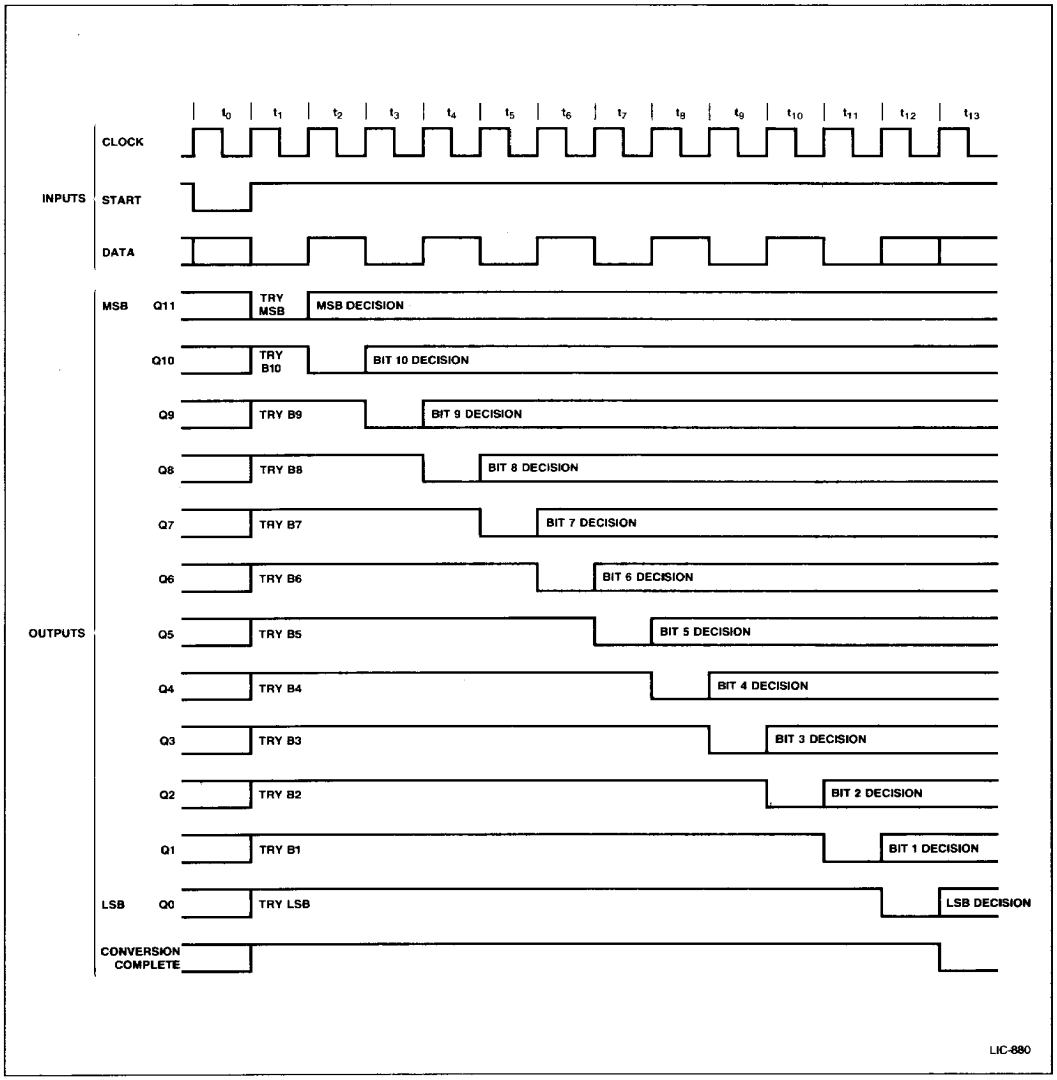


Figure 19. Typical Timing Diagram for Successive Approximation Converter

MICROPROCESSOR-BASED SYSTEM INTERFACING

The Am6012 can be interfaced to a microprocessor-based system. But microprocessors with an 8-bit bus have the problem of interfacing to the 12-bit DAC. This is solved by breaking the 12-bit word into 8- and 4-bit bytes and storing each into a memory location. Figure 20 shows a 12-bit DAC interfaced to the popular Am9080A using an Am9555 Programmable Peripheral Interface. This allows two Am6012s to be connected. For a simpler system the Am9555 could be replaced with a 12-bit latch and some control logic.

Interfacing the Am6012 to a 16-bit microprocessor such as the AmZ8001/8002 is shown in Figure 21. The DAC peripheral location is addressed by the CPU and decoded by the AmZ8136 (8-bit decoder with control storage), which contains input latches, allowing the peripheral address to be latched and decoded from the address bus. The $\overline{AS}$ (address strobe) signal from the CPU informs the decoder when the address is stable and is used as the input register latch command. Two transparent latches are used to latch the data off the address/data bus. The $\overline{DS}$ (data strobe) command produces a $\overline{CS}$ (chip select) to force the AmZ8173 octal

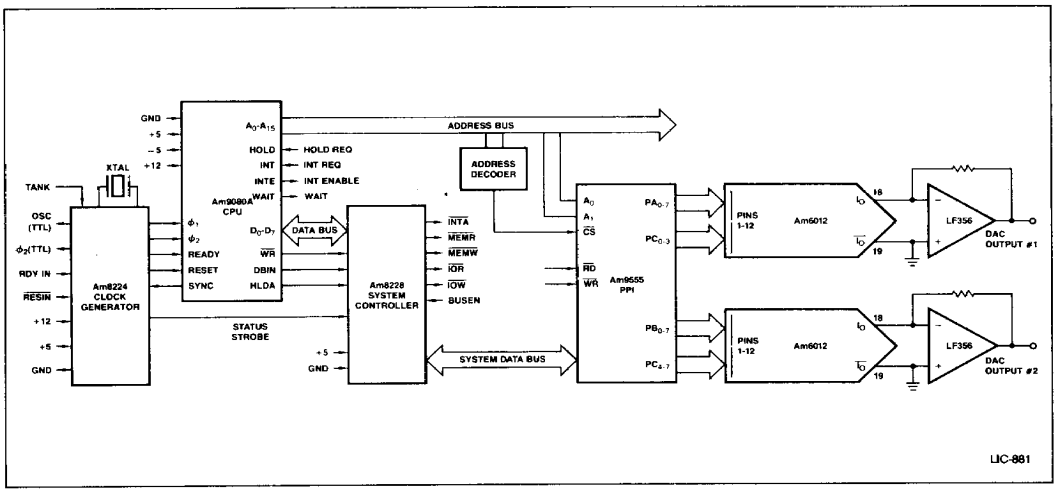


Figure 20. Two Am6012 D/A Converters Controlled by an Am9555 PPI

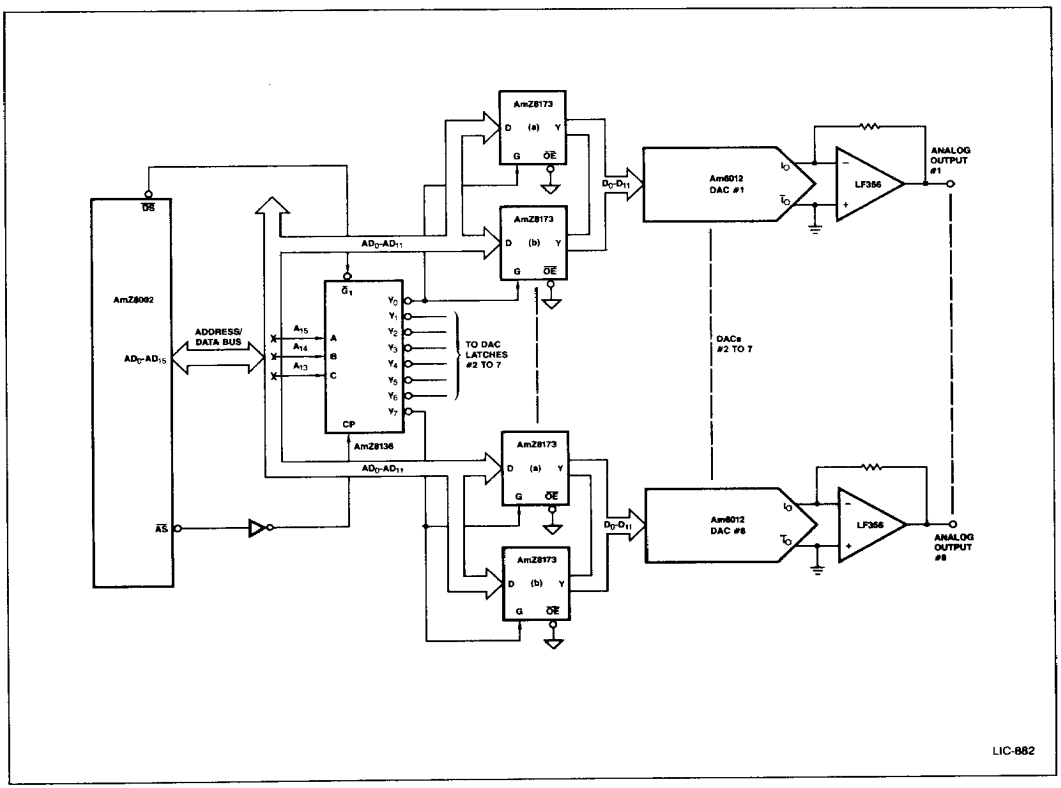


Figure 21. AmZ8000 Interface for Am6012 12-Bit DAC

latches into their transparent mode. When $\overline{DS}$ goes HIGH this causes $\overline{CS}$ to go HIGH and retains the data in the AmZ8173. This prevents erroneous data from appearing at the Am6012 inputs during CPU operations and causing the output from displaying the wrong information. The AmZ8000 has the capability of outputting not only single words of data, but also blocks of data from contiguous memory locations. The time for each data transfer is 10 clock cycles, resulting in a data update time of 2.5μsec. Additional time can be allowed for the DAC to settle by including extra WAIT states. Each wait state period is 250nsec.

When used in a successive approximation type of ADC described earlier, the Am6012 can be interfaced to an Am9080A to allow analog information into the microprocessor system (Figure 22). The ADC data conversion procedure is controlled by the Am9080A Microprocessor set (Am9080A 8-bit microprocessor, Am8224 clock generator and driver, and Am8228 system controller and bus driver). The Am26S02 is used as the START monostable circuit and is activated by ($\overline{CS}$ = 0, and $\overline{IOW}$ = 0). START ADC command sets the $\overline{S}$ input of the SAR circuit Am2504 to a logic 0. The width of the monostable pulse must be greater than the period of the DATA CLOCK signal to initialize the SAR logic. The DATA CLOCK period must be sufficiently long to allow for the worst-case settling time of the Am6012 DAC and comparator Am111 and to ensure valid data at the SAR input. After $\overline{S}$ goes LOW the first clock sets $\overline{C}_C$, changing it to logic ONE, and the sample and hold reverts back to the sample mode. The microprocessor is then allowed to resume its function by removing the logic ZERO from the RDYIN input of the Am8224 chip. Logic ONE at the SAR's $\overline{S}$ input prevents DATA CLOCK from changing the digital data outputs of the SAR after the completion of a conversion. When the microprocessor issues a READ ADC command ($\overline{CS}$ = 0, $\overline{IOR}$ = 0), the data buffer (Am9555) is enabled to transfer the data outputs of the SAR to the system data bus and into the microprocessor accumulator where on a subsequent memory write command stores the data into a memory location. The ADC must be given another START ADC command by the microprocessor before another conversion cycle can be started.

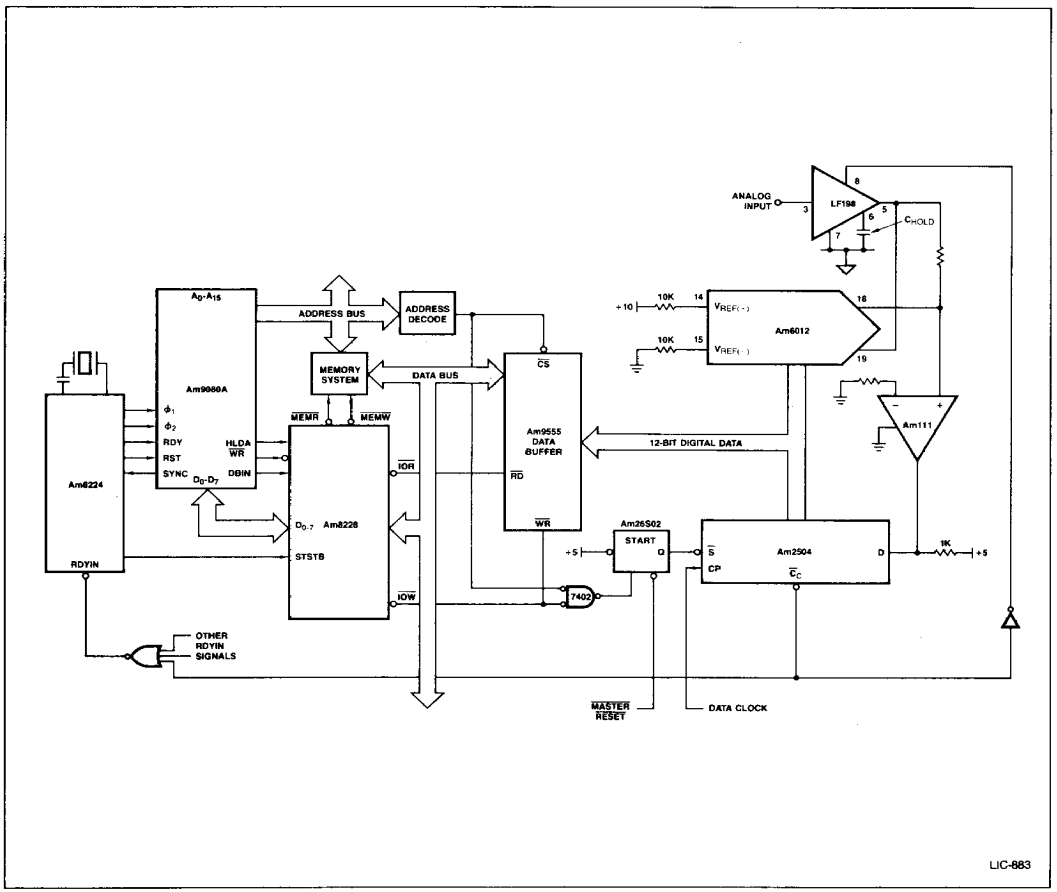


Figure 22. Microprocessor Controlled 12-Bit Analog to Digital Acquisition System