VENTURE (TM)

Technical Manual 1.0

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FOREWORD

This manual is designed for your ease in reading schematics. A description accompanies each schematic on the opposite page. This should help clarify the schematics and aid in your understanding of the technical aspects of VENTURE™.

The following Table of Contents is an outline of the information contained in the schematic descriptions. To find the particular information you are interested in, look up the schematic PAGE number as listed, and opposite the schematic is additional verbal explanation.

EXIDY VENTURE (TM)

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1. Master Oscillator (1D)

From this oscillator all dynamic operations are derived, such as the processor clock, the main element and line counters, the shift register clocks, as well as all other forms of timing signals.

2. Element (Horizontal) Counters (1C, 1E, 2E)

These components form the final stages of horizontal timing. All operations in this game requiring horizontal positioning or timing have their origin here. Note that, beginning with signal HCLK (from Clock Divide Counter 2D), there are 256 counts prior to setting signal E256 high. When this signal goes high, it indicates that the horizontal blanking period is in progress. At this time the final counter (1E) is preloaded with a higher number than previously loaded. This creates a shorter count the second time around. The shorter count measures the retrace interval. When the retrace count is finished, the counter preloads with a lower number, establishing a longer count sequence again for "real time" sweep of the electron beam across the face of the CRT.

3. Line (Vertical) Counters (4F, 5F, 6E)

These components form the entire vertical timing operation starting with a clock derived from horizontal timing. These counters count 256 times and then preload with a higher number, causing a shorter count the second time. This shorter count measures the vertical retrace interval. Note that signal L256, when high, indicates vertical blanking is in progress. After the completion of the vertical retrace count, the counters once again preload with a lower number. This way they count 256 times during the sweep of the electron beam down the face of the CRT, allowing the horizontal timers to sweep one complete horizontal line for each count of the vertical counters. Thus, the electron beam reaches the bottom of the CRT, after completing 256 horizontal line sweeps. It then begins the vertical retrace count, and the whole cycle begins anew with the beam starting again at the top of the CRT.

4. Screen RAM Addresses (7D)

During the time the screen RAM is examined by the logic for output to the monitor screen, addresses must be applied to the screen RAM to count up at a rate corresponding to the image cells conceptually arranged on the screen in a 32 x 32 matrix. The counts used here, 4 from the element counters, and 4 from the line counters, fulfill this timing requirement. The least significant element count used (E8) represents an interval exactly eight times that of one element. The least significant line count used represents an interval exactly eight times that of one horizontal line, or eight times a single line count. Dividing a 256 element line by 8 yields 32, and likewise dividing a 256 line vertical sweep by 8 yields 32. Thus the screen RAM address lines (RAM0 through RAM9) count at a rate that creates 32 horizontal counts and 32 vertical counts as the electron beam sweeps the face of the CRT. This makes 1024 conceptual "image cells" into which can then be inserted images of 8 elements by 8 lines. For more information concerning these images, refer to the text for pages 2 and 3 of the Logic Schematics.

5. Coin Input Decoding (1H)

Some models of VENTURE (TM) contain two separate coin inputs for special coinage applications. NOR gate 1H combines these separate inputs, making signal 5COINT, which sets the interrupt flip-flop (6E on page 8) when either coin input becomes active, thus forcing the microprocessor to jump to the interrupt service routine. This interrupt driven operation prevents ever missing a coin when inserted. However, this also means that when a game is first powered up, the coin input must be inactive. If for some reason the coin input switch is enabled at the time of power up, the game does not properly initialize until the switch is disabled.

6. Hardware Generated Line Positioning Proms (3E, 4E)

These PROMs are not used for VENTURE (TM).

7. Blanking and Video Clocking (5H)

Flip-flop 5H merely combines blanking and all other video.

8. Black and White Composite Video Output (1H)

This circuit is not used for VENTURE (TM). If desired, however, these components may be installed to aid troubleshooting, by acting as a "video probe".

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1. Screen Controller PROM (6D)

This PROM controls the direction of data flow into and out of the screen RAM and character generator RAM. It prevents timing errors and buss conflicts, assuring that the microprocessor can write to either the screen or character generator RAM, or read back from either.

2. Screen RAM (7B, 8B)

The screen RAM is comprised of two 1024 x 4 static RAMs, configured to act as a single 1024 x 8 RAM. This creates a screen matrix of 32 horizontal by 32 vertical positions. A single byte code is stored in each of these positions to represent a particular character. During "real time" (the time the CRT is being swept by the electron beam) these character codes address the character generator RAM.

These character codes, when used as addresses, are combined with the three least significant line counts (L1, L2, L4) to present to the character generator output shift register all the necessary data to form an 8 element wide by 8 line high character on the CRT, located within one of the 1024 positions mentioned immediately above; that is, the 32 horizontal by 32 vertical positions.

The screen, then, is a storage place for single byte codes that call up an 8 x 8 character and place it into the corresponding character cell. This character is stored in the character generator RAM, shown on page 3 of the schematic.

3. Character Image Storage

Shown on this page are two PROMs (9C, 10C). They could be used as a permanent set of characters. However, VENTURE (TM) uses RAM instead, to increase the flexibility in character manipulation. This portion of RAM appears on page 3 of the Logic schematics.

4. PROM Power and Signal Selection (10B)

This Dip Shunt configures the logic for different types of PROM devices. For VENTURE (TM), however, this Dip Shunt is unnecessary due to the fact that RAM has been used rather than PROM.

5. Character Generator Output Shift Register (12B)

Video from the character generator memory devices (RAM in the case of VENTURE (TM)) is formed by this shift register as a byte of data that displays one line at a time from left to right on the CRT. This ultimately forms an 8 line high by 8 element wide character positioned on the screen according to the time it is presented to the shift register.

Output from this shift register are all the images seen on the screen except the player image and the player missile image.

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Image Storage RAM

1. Character Generator Image Storage RAM (13C, 11C, 14C, 12C)

These four RAMs, when used in this configuration, act as a 2048 x 8 bit RAM. The images placed on the screen are stored in this RAM by the microprocessor, according to the game program. In this RAM images are established, altered, shifted slightly, and even replaced with a new set, if required by the program.

When called by the logic to do so, the RAM presents, to the character generator shift register, a single byte, representing one line of a particular image. Each image is composed of 8 lines of data, each line is one byte-wide. Thus, 256 images of 8 x 8 bits can be stored here simultaneously and "called up" by the screen RAM to be displayed on the CRT in any of the 1024 character cell positions. A single byte code, stored in the screen RAM, calls up a character. The character may change or move by replacing the single byte code in the screen RAM, or by altering the data in the character generator RAM which forms the image.

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1. The 6502 Microprocessor (2A)

For detailed information concerning this microprocessor, refer to the MOSTEK publication, 6500-10A, MCS Microcomputer Family Hardware Manual.

One feature that should be mentioned here, however, is that this microprocessor has "memory-mapped I/O". This means that all ports interfacing to peripherals of any type must be located within the normal memory map, with no duplication of addresses, since no instructions are specifically oriented toward I/O operations.

2. Power-on Reset circuit (connected to 2A pin 40)

When power is first applied to a game, a particular sequence of events must occur to set up all logic conditions. If this sequence is broken for whatever reason, the microprocessor may become confused, and the game will not start and run.

This sequence is accomplished when the reset line to the microprocessor is the last line allowed to reach a "high" logic level. The Power-on reset circuit makes sure this occurs by utilizing the charge time of an RC network as a delay.

If any kind of power interruption occurs during normal game play, the power-on reset circuit insures that the microprocessor is reset. This alleviates confusing the microprocessor, while it also recreates the original power-on sequence.

3. Processor Workspace RAM (4A, 5A)

The RAM, or workspace, consists of the lowest 1024 bytes of memory and can be divided into three separate sections due to distinctly different functions.

The lowest 256 bytes (0 to FF Hexadecimal) is reserved for special software register operations, and is called "zero page". The processor uses this area to store dynamic variables. For details of this type of operation, refer to 6502 technical literature regarding "Zero Page Addressing".

The next higher 256 bytes (100 to 1FF Hex) is reserved for the 6502 stack. The processor stores return addresses in the stack when interrupted or called to execute a subroutine. The game program may also request the processor to store other kinds of information here for later retrieval.

The next higher 512 bytes (200 to 3FF Hex) are used as a scratchpad area. Miscellaneous calculations and their results are temporarily stored here.

4. Main Address Decoding (5C, 5D, 5E)

This circuit is the first stage of the address line decoding necessary to organize the memory map; that is, it places specific functions or devices within generalized blocks of the memory map, grouped by function.

For details on the addressing scheme, see MEMORY MAP, Figure 1.

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1. Program Memory (6A through 13A)

These memory devices may be 2516, 2716 (5 volt only), or 2732 EPROMS. If 2516 or 2716 EPROMS are used, there will also be an additional memory expansion PCB in use to create more memory space. This PCB is simply an extension of the address, data and control lines present at the memory devices situated on the logic PCB.

Note that four of the lines to each memory device (PCS0 through PCS7, PAP19, PAP20, PAP21) are programmable through jumper configurations located at 4B and 11B. This allows different memory devices to be used and/or facilitates interconnection to the memory expansion PCB (if used).

2. PROM Address Selection (4B, 5B)

This is a second stage of address decoding, used to select each individual memory device when addressed. Signal ROMSEL (from page 4 Main Address Decoding) selects the Program Memory devices in general, and jumper 4B, together with decoder 5B further defines an address to a particular memory device.

3. Memory Device "Personality" Selection (11B)

The dip shunt, or jumpers block, alters control signal configuration to the program memory devices. This allows the use of alternate size EPROMS and/or those created by different manufacturers whose control signal pinouts may not be identical to one another.

1. Moving Object Horizontal Position (13F, 15F, 14F, 16F)

Counters 13F and 15F form a byte-wide counter which horizontally positions Moving Object 1 on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of the Horizontal Sync, they begin to count. The count outputs AND'ed through 15E give rise to signal M1HW, the Horizontal Position Window for Moving Object 1. Counters 14F and 16F are the equivalent circuit for Moving Object 2.

2. Moving Object Vertical Position Counters (16E, 12E, 1E, 13E)

Counters 16E and 12E form a byte-wide counter which positions Moving Object 1 vertically on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of Vertical sync, they begin counting. The four count outputs of the least significant of these two counters (M1L1, M1L2, M1L3, M1L4) are sent to the moving object image PROM to specify which line of the image is presently being displayed. The AND'ed outputs of the second counter give rise to signal M1WW, the Vertical Position Window for Moving Object 1. Counters 11E and 13E are the equivalent circuit for Moving Object 2.

3. "Write Moving Object" Decoding (6F, 16H, 5E, 3F)

Consists of two distinctly different functions. 6F and 16H form the circuit that generates the load pulses for the moving object position counters, while 5E and 3F simply prevent the counters from counting during blanking.

4. Color Interface Output (16B)

This is a 14 pin DIP socket used as the connector interface to the color selection circuitry, located on the audio PCB. The signals and their functions are listed below:

Pin #		
1	5SRLOAD	= Shift Register Load Pulse (Neg. True)
2	CBLB	= Composite Blanking
3	CSYNC	= Composite Sync
4	5CVID	= Composite Video (Neg. True)
5	5SCLK	= Shift Register CLock (Neg. True)
6	HSYNC	= Horizontal Sync
7	GND	
8	VSYNC	= Vertical Sync
9	5MO2VID	= Moving Object 2 Video (Neg. True)
10	5MO1VID	= Moving Object 1 Video (Neg. True)
11	VA9	= Character Generator Address Line 9
12	5LINES	= NOT USED ON VENTURE
13	VD7A10	= Character Generator Address Line 10
	+5V	

1. Moving Object Multiplexing (14A, 14E)

These two multiplexers pass information to the moving objects image PROM. They contain two codes: one determines which image should appear, and the other specifies which line of that image is to be displayed.

The data passed alternates between data for Moving Object 1 and Moving Object 2, depending on the state of element count E32.

The upper multiplexer (14A) passes the "which image" code, and the lower multiplexer (14E) passes the "which line of that image" code.

2. Moving Objects Image PROM (11D)

This EPROM accepts as an address the image and line codes of moving objects 1 and 2 (see "Moving Object Multiplexing" above). It then presents the appropriate data for one line of the image to the output shift registers.

The timing of the logic insures that the correct pair of shift registers are loaded with the data, then shifted out at the correct time to become, one line at a time, the 16 lines of video for that character (Moving Object 1 or 2).

3. Moving Object Video Output Shift Registers (12D, 13D, 14D, 15D)

Shift registers 12D and 13D together form a 16 bit shift register whose task is to accept, as data, 16 bits (2 bytes) representing a single line of the image for Moving Object 1, then shift these 16 parallel bits out serially to become video. This operation is repeated for 16 consecutive lines, resulting in a video image that is 16 bits wide by 16 lines high on the monitor screen.

Shift registers 14D and 15D together form this same type of circuit, identical in function, for Moving Object 2.

4. Moving Objects Shift Register Load Logic (2F, 16H)

This circuit sends properly timed load signals to the Moving Object Video Shift Registers. These load signals are needed to load the image data into the shift registers at locations 12D, 13D, 14D, and 15D.

5. Moving Object Shift Register Control Logic (15H, 14H)

The input signals to the upper two gates (15H) represent horizontal and vertical position "windows" for the two moving objects (for example, M1HW = Moving Object 1 Horizontal Window, M2VW = Moving Object 2 Vertical Window). These windows allow the Moving Object shift registers to shift only at the right time. This insures the image is generated at the correct position on the screen.

The lower 2 gates of 15H are, in VENTURE, used for later decoding in the color selection circuitry, located on the audio PCB.

6. Memory Device Personality Configuration (10D)

This is another Dip Shunt which reconfigures the PC board in order to use an EPROM (11D) of another type or manufacturer.

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1. Interrupt Status Latch (8E)

This latch is set when a coin is dropped or vertical sync occurs. When the latch is set, the CPU is interrupted; that is, signal $\overline{IRQ}$ goes low. This forces the CPU to jump to the interrupt service routine. The interrupt service routine instructs the CPU to check for a coin input, and then run a debounce routine on the coin bits of ports 9E or 15A, depending on which coin input bit was set at 8E.

If the CPU finds no coin input bit set at latch 8E, it will assume the Interrupt condition was caused by vertical sync. This tells the CPU that it should now jump to the routine that services the normal game play, and that the screen can now be updated with new data. The screen can only be updated during the vertical retrace interval.

Note that this latch also has two signals labeled LNG0 and LNG1 which both show PC etched jumpers. These two bits are the select bits for one of four languages, English, French, German, and Spanish. You may select a language by cutting the appropriate jumper, allowing it to be pulled to a logic high. For English, no cutting is necessary. See the Operator's Manual for proper configuration of other languages.

Also on this latch is the signal named TABLE. This signal, tied to a pullup resistor and switch, determines whether the program operates as a table model or in the upright game configuration. Please check with the Exidy Marketing Department and the Operator's Manual for more details, since table models may or may not be available.

2. Option Switch Port (15A)

This port provides input from the option dipswitch, at location 16A. Data from the dipswitch is gated onto the data buss and read by the CPU at game start. This allows such options as number of turns, coins per game, additional game versus extra turn, etc.

Note that one input of this port (labeled COIN 2) does not come from the switch. Instead, it comes from Coin Input 2, and is used for debouncing the auxiliary coin input switch.

3. Control Inputs Port (9E)

This port provides input from the controls located on the control panel, such as the joystick, fire button, one player start, and two player start. Data from these controls are gated onto the data buss for examination by the CPU during the regular service routine (which is synchronized to the vertical interval).

Note that one of these inputs is from the COIN1 input (labeled 5COIN1) rather than a game control input. The COIN1 input to this port is used for debouncing the standard coin input.

4. Moving Image Latch

Only the CPU can write to the moving image latch. This latch contains the code that specifies which image or images are presently being displayed by the hardware moving object circuitry.

5. Audio Board Port

This latch is written to and read by the CPU, and transmits instructions to the audio board when any sounds are enabled, disabled, or the game is initialized. In addition, this port passes data sent to select colors for screen images. For the functions of these instructions, see the audio board schematic and/or description of operation.

6. Control Port Latch (9D)

This latch, used only in table versions, is written to only by the CPU and keeps track of which player is "up", in order to select which controls are active, that is, player one or player two.

7. I/O Decoding (7E)

The upper half of this decoder generates the chip selects for those I/O devices written to by the CPU, and the lower half generates the chip selects for those I/O devices which are read by the CPU. See the detailed memory map for more precise information.

Figure 1: MEMORY MAP

Hex Address	Function or Device
FFFA-FFFF	Interrupt and Reset Vectors
8000-FFF9	Program memory space
52XX	Audio board communications
5103	Interrupt Condition Latch (read)
5101	Control Inputs Port (read)
5101	Output Control Latch (write) (Not used in VENTURE (TM) upright)
5100	Moving Objects Image Latch (write)
5100	Option Dipswitch Port (read)
50C0	Moving Object 2 Vertical Position Latch (write)
5080	Moving Object 2 Horizontal Position Latch (write)
5040	Moving Object 1 Vertical Position Latch (write)
5000	Moving Object 1 Horizontal Position Latch (write)
4800-4FFF	Character Generator RAM
4000-43FF	Screen RAM
0200-03FF	Scratchpad RAM
0100-01FF	Stack RAM
0000-00FF	Zero Page RAM

AUDIO/COLOR PCB-GENERAL DESCRIPTION

The Audio/Color PCB is so named because it contains not only the circuitry required to generate all sounds, but also the color selection decoding circuitry and video output connector.

This PCB contains a dedicated 6502 microprocessor and circuitry to support the simultaneous generation of many types of sound, including three channel music. The Logic PCB simply sends commands to the Audio/Color PCB via a bi-directional communications port and the Audio/Color PCB takes it from there. In some cases this PCB even aids the Logic PCB in some of it's calculations when there is not enough processing time available on the Logic PCB.

As a result of this structure, the actual program to generate sounds or music resides on the Audio/Color PCB. There is also a handshake required between the two PCB's in order for the system to power up correctly, and of course, there is no video output without the Audio/Color PCB connected.

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1. Logic and Power Interface (P5, J2, J3)

Connector P5 provides the audio/color PCB with all the power it requires to operate. Also fed through this connector are the two speaker output leads. P5 interfaces only to the power supply module and the speaker, through the main harness.

Connectors J2 and J3 are the most significant path of communication between the Logic and Audio/Color PCB's. Address lines, Bi-directional Data lines, processor control lines, and the Audio/Color PCB Select line are all passed through these two connectors.

2. Communications and Address Decoding (9B, 13D)

Peripheral Interface Adapter (PIA) 9B, in concert with 8B (another PIA, shown on page two) serves as a bi-directional communications path between the Logic PCB and the Audio/Color PCB. During information transfer between the two PCB's, both PIA's are in use. Information from the Logic PCB microprocessor passes through the PIA at 9B to the PIA at 8B, then to the microprocessor on the Audio/Color PCB. When information is passed the other direction, the path is the same, but the direction is reversed.

During the time that no information transfer is occurring between the two PCB's, both microprocessors can continue to operate independently.

Also shown on page one is 13D, a 3-line to 8-line decoder, used to generate the write signals for the Color Data Latches. These Latches will be covered in the text for page five of the Audio/Color PCB.

1. 6502 Microprocessor (3B)

This microprocessor is the same as that used on the Logic PCB, but is exclusively dedicated to the generation of sound. It can communicate with the Logic PCB microprocessor, and receives it's instructions thereby. Once it has received it's instructions, however, it asserts complete control over all Audio/Color PCB circuitry and ignores the Logic PCB microprocessor until such time as it is informed that another command is ready. Some commands are of a type that must be processed immediately, irregardless of other operations in progress, and some commands can wait until the operations in progress are completed. The program on the Audio/-Color PCB handles all these eventualities appropriately.

2. Peripheral Interface Adapters (8B, 7B)

The PIA at 8B, as mentioned in the text for page one, is used in bi-directional communications between the microprocessors on the Logic PCB and the Audio/Color PCB.

The PIA at 7B is used for two fundamental purposes on this PCB. The first, and most important, is that it contains the RAM that the microprocessor uses for zero page and stack operations. The PIA only contains 128 bytes of RAM, which under normal circumstances would not be sufficient for both zero page and stack. In this case, however, the memory map on this PCB has been altered, so that when the microprocessor thinks it is putting the stack at address 01FFH it is actually putting it at address 007FH.

The second use of this device is that of a programmable interval timer, used for various purposes unique to the specific sounds being generated on this game. The ability of this device to generate interrupts at time out is utilized here.

3. Address Decoding (4B)

Keyboard Encoder (4B) is used here to generate the chip selects of all devices located in the memory map of the Audio/Color PCB.

4. Music Generator (2B)

Another Programmable Counter/Timer device is used here to generate music (and sometimes other special effects) in up to three channels (or voices) simultaneously. The music is created by a special software operating system, and all but the counter/timer chip is therefore invisible.

5. Master Oscillator (A1,B1)

This oscillator is the source of all timing on the Audio/Color PCB. If this clock stops running, so does everything else on the Audio/Color PCB. It is, however, completely independent of the clock and other timing signals generated by the Master Oscillator located on the Logic PCB.

6. Program Memory (3A, 4A, 5A, 6A, 7A)

The memory devices used here are 2716 (2048 x 8) EPROMS. The DIP shunt located at 8A is used to reconfigure the control and power supply lines, if necessary, for equivalent devices from different manufacturers, whose pinouts may not be the same.

7. Output Filter Latch (1C)

This latch is used simply to switch different output filter capacitors in or out of the circuit to soften or shade the sound, according to program requirements.

1. Clock Manipulation and Noise Generation Circuit (3D,4D,6D,5E)

The timers inside Programmable Timer Module 3D can be incremented or decremented either internally by the Phase Two clock input, or externally from the "C" inputs (C1,C2,C3). Both options are used by the program. When the counters are being controlled by the Phase Two clock, the "C" inputs have no effect, and the noise generation circuit is therefore inoperative. In order to generate sounds that are classified as noise, or contain some kind of noise within them, the counters are programmed to decrement in accordance with the input on the "C" inputs. While in this mode, the combination of 6D (Dual "D" Flip-Flop) and 5E (128 Bit Shift Register), are used to "randomize" the clock inputs to the Programmable Timer Module (3D). The "randomizer" can be clocked with either the Phase Two clock or counter output Q1.

2. Amplitude Modulation Control (2D, 7D, 8D, 9D)

Counter (3D) outputs Q1,Q2, and Q3 are already highly complex sounds, but in order to create much more specialized audio they must be modulated in amplitude. Each channel is separately controllable in amplitude by associated Digital-to-Analog converters comprised of analog multiplexers and a resistive ladder network. Three control bits on each multiplexer select a voltage to output, according to which input pin is addressed (since each input pin is tied to a different point, and therefore voltage, in the resistive ladder).

The voltage thus selected is applied to one of the two inputs to each segment of 2D (another triple analog switch). The other input is tied to ground. Note that the control bit to each analog switch segment is one of the previously mentioned count outputs (Q1,Q2,Q3). In this manner, each output can be controlled for frequency and amplitude individually.

Note also that the count output from Q1, unlike Q2 and Q3, first passes through yet another analog switch whose function is to turn off the count output of Q1 prior to reaching the Digital-to-Analog conversion stage. This is done because the Q1 output is the one used for selective clock frequency generation, and would therefore interfere with other sounds if not disabled at the appropriate time.

3. Output Summation and Special Effects Volume Control (2E)

The three segments of Operational Amplifier 2E are configured as voltage followers (for impedance considerations), and their outputs are summed together at the top of a 10K POT, R31. The output volume, therefore is determined by the voltage applied at each input and the adjustment of the POT. Note that the resistors used to sum these three outputs together are large in value, so that each channel will have minimal effect on the others when conflicting signals arrive simultaneously (except, of course, that their sum will appear at the output).

This summed output is then again summed with all other sounds generated by this PCB at the input to the final Power Amplifier.

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1. Summing Amplifier and Master Volume Control (3F, R46)

One segment of Operational Amplifier 3F is used here as a point at which all the various sounds generated on this PCB are brought together. Note that the output goes immediately to a 10K POT (R46) which has ground on the other end. The wiper, therefore, varies the final output volume of all sounds together.

2. Integrator and Audio Power Amplifier (3F,10F)

Another segment of Operational Amplifier 3F is used here as an integrator; that is, it is used to "roll off" the higher frequency sounds in order to prevent the power amplifier from going into unwanted oscillation.

The Audio Power Amplifier (10F) is a Dual Audio Amplifier IC configured as a "Bridge Amplifier" and may be either a LM377 or LM378 for Revision A, Audio/Color PCB. Revision letters are locted at position 11C. In later versions of Venture it may possibly use a LM379 with a reconfigured DIP shunt. Information regarding this is available in the operators manual for this game, or contact the Exidy Customer Service Department for assistance if you must use an alternate device.

Volume Controls

Master Volume R46, see the fourth page of Audio/Color PCB schematics.

Music Volume R9, see the fourth page of Audio/Color PCB schematics.

Special Effects Volume R3, see the fourth page of Audio/Color PCB schematics.

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1. Pattern Character Color Division (10A, 9A)

The two segments of Flip-Flop 10A, using the upper two address lines from the character generator circuit, divide the character generator RAM space into four (4) conceptual groups (or quadrants) according to address. This is done in order to assign different colors to different characters.

Using this method, any character stored in a particular quadrant will be the same color as any other character stored in that same quadrant. If the same character is stored in a different quadrant, it will be displayed with a different color. The output of 9A (Two-line to Four-line decoder) applies the separated video lines of these quadrants to priority encoder 10B, whose task is to determine which image is to take visual preference when two or more coincide on the TV screen; that is, which image is to appear to be in the "foreground", and which is to appear to be in the "background".

2. Priority Encoder (10B)

All the video signals generated by the logic PCB are applied to the priority encoder. The signals assigned the higher priority are shown at the top, and the lower priority are shown on the bottom. The output of this device is a 3 Bit code representing the highest priority video line active at that instant. This output code is then sent to the color multiplexers as an address which will select the appropriate color for the imagery generated on that video line. Note that the lowest priority input to the encoder is tied permanently low (active). This insures that when no other video is being generated, there is a background color present, unless of course, the program has selected a background color of black at that time.

3. Color Data Latches (11C, 12C, 13C)

These latches are addressed directly by the Logic PCB microprocessor. Here the microprocessor stores the data that determines which character is what color. This data is then passed to the color selection multiplexers.

4. Color Selection Multiplexers (11B, 12B, 13B)

Each of the three multiplexers controls the video output to a different color gun in the CRT. One turns the red gun on or off, one turns the green gun on or off, and the third does the same for the blue gun. The output combination of the three multiplexers provides for one of eight possible colors to be displayed at any given instant. The color displayed is determined by two things: what type of video is present (e.g. which character), and what color the microprocessor has currently assigned to that type of video. As mentioned above, the color assignations are stored in the color data latches. The priority encoder (10B) issues the code representing the type of video currently displayed. Using these two pieces of information, the multiplexers look at the appropriate bits in the color latches and send the data directly to the TV to turn the color guns on or off.

5. Video and Sync Signal Polarity Selection (11A, 12A)

Before being reclocked one last time, all video outputs are passed through an Exclusive-Or gate (11A), so that one input of each segment can be used to invert the video (make it 180 degrees out of phase with respect to the input to the gate). This feature insures compatibility with TV monitors made by several different manufacturers.

The TV Sync signals are also routed through Exclusive-Or gate segments (12A) for the same purpose.

6. Final Video Output Re-synchronization (13A)

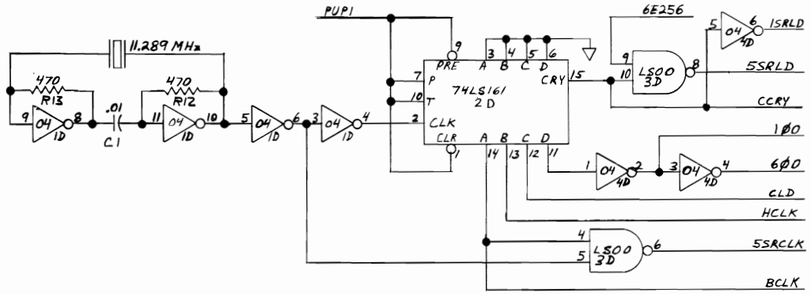
To insure that all video signals and sync signals are accurately synchronized in time, they are all re-clocked one last time together by a HEX "D" Flip-Flop. It "cleans up" any spurious irregularities or propagation delays that may have crept into any of the video or sync signals.

PAGE 1 OF 1: MEMORY EXPANSION PCB

For information on the Memory Expansion PCB, refer to PAGE 5 OF 8, GAME LOGIC PCB. See section 1. Program Memory (6A through 13A)

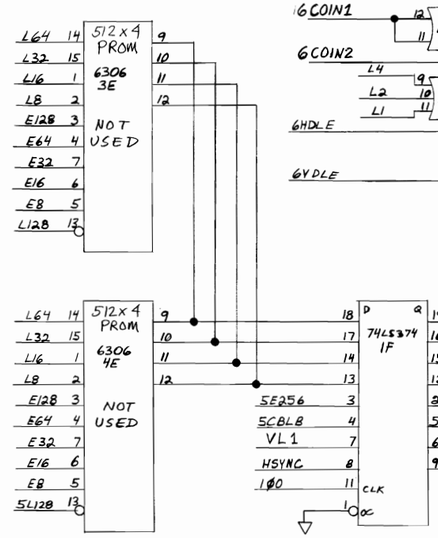
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	E		6-12-81	

MASTER OSCILLATOR

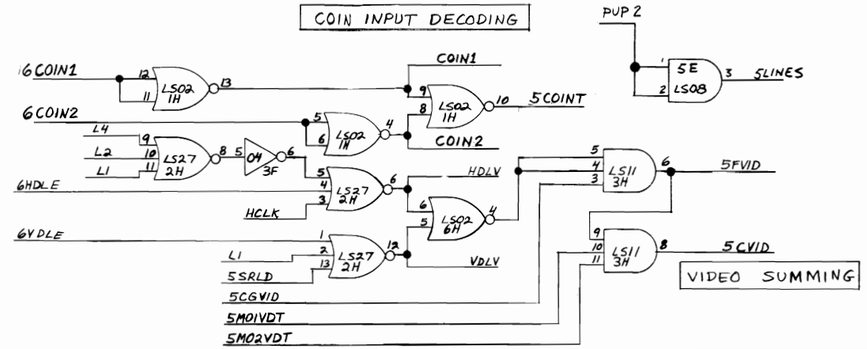


CLOCK DIVIDE

HARDWARE GENERATED LINE POSITIONING PROMS

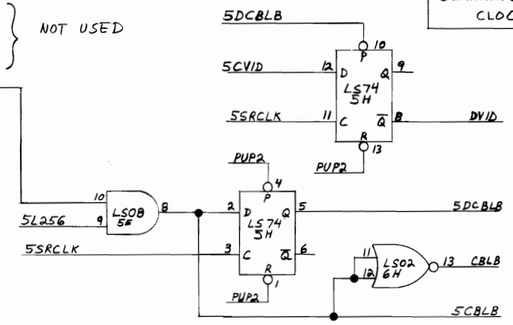


COIN INPUT DECODING

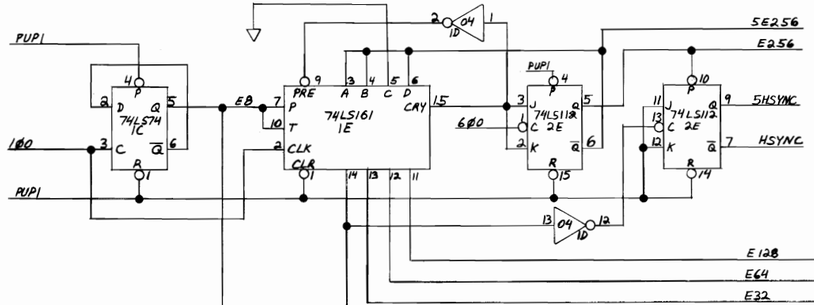


VIDEO SUMMING

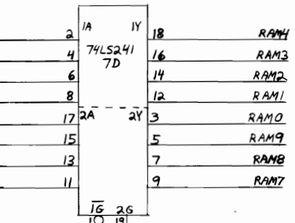
BLANKING & VIDEO CLOCKING



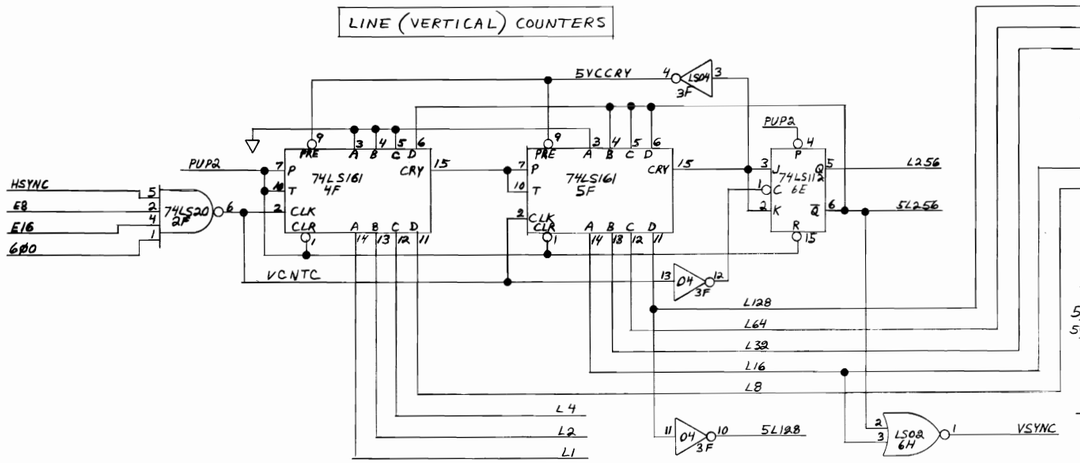
ELEMENT (HORIZONTAL) COUNTERS



SCREEN RAM ADDRESSES

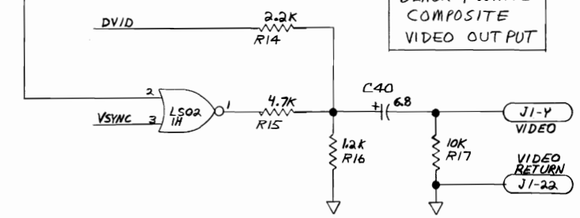


LINE (VERTICAL) COUNTERS



BLACK & WHITE COMPOSITE VIDEO OUTPUT

NOT USED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USE

APPLICATION | DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN OKS	6-12-81
CHECKED	

6502 GAME LOGIC PCB

SYNC AND VIDEO GENERATION

SIZE	CODE IDENT NO.	DRAWING NO.
D		77-3374-11 REV E

SCALE | SHEET / OF 8

BISHOP GRAPHICS, INC. REORDER NO. 20509

SCREEN CHIP SELECT and BUSS DIRECTION DECODING PROM

1Ø0 14 VSEL 13 A11 12 VD7A10 11 R/W 10 — 6331 OR 82S123 GD — PROG # HRL 6D-1 — 15

9 CSSR
7 CSCG1
6 CSCG2
5 SESBD
4 SECGBD
3 DBDIR
2 SWR 13
1 ESBD

220 R311 — C300 330 pf

CLD 12 — LSØØ 3D — 11 GSWR

11 — 04 4D — 10 ECGBD

SCREEN RAM(S) (CHAR. CODE STORAGE)

VD7A10

A9 2 A8 4 A7 6 A6 8 A5 17 A4 15 A3 13 A2 11 5ESBD 1 ESBD 19 — LS241 6B — 18 16 14 12 3 5 7 9

RAM 9 15 RAM 8 16 RAM 7 17 RAM 6 1 RAM 5 2 RAM 4 3 RAM 3 4 RAM 2 5 RAM 1 6 RAM 0 7 CSSR 8 GSWR 10 — 2114 7B — A9 11 12 13 14 — AØ CS W

A1 17 A0 15 ESBD 19 5ESBD — LS241 1A — 2A 2Y 3 5

15 16 17 1 2 3 4 5 6 7 — 2114 8B — A9 11 12 13 14 — AØ CS W

CSSR 8 GSWR 10

D7 2 D6 3 D5 4 D4 5 D3 6 D2 7 D1 8 DØ 9 5ESBD 19 DBDIR 1 — LS245 6C — A B — 18 17 16 15 14 13 12 11 — ENA DIR — O→I

18 17 14 13 3 4 7 8 — LS374 7C — /SRLD 11 ECGBD 1 — CLK ØC — 19 16 15 12 2 5 6 9

L4 2 L2 4 L1 6 — LS241 9B — 1A 1Y 18 16 14 — ECGBD 1 — 1G

A10 2 A9 4 A8 6 A7 8 A6 17 A5 15 A4 13 A3 11 5ECGBD 1 ECGBD 19 — LS241 8C — 1A 1Y 18 16 14 12 3 5 7 9 — 1G 2G

A2 17 A1 15 A0 13 — LS241 9B — 2A 2Y 3 5 7 — ECGBD 19 — 2G

VA9 22 VA8 23 VA7 1 VA6 2 VA5 3 VA4 4 VA3 5 VA2 6 VA1 7 VA0 8 CSCG1 18 VRP21 21 VRP20 20 VRP19 19 — PROM 9C — CS — NOT USED — See Page 3

22 23 1 2 3 4 5 6 7 8 CSCG2 18 VRP21 21 VRP20 20 VRP19 19 — PROM 10C — CS — NOT USED — See Page 3

17 16 15 14 13 11 10 9

VD7 14 VD6 12 VD5 11 VD4 10 VD3 5 VD2 4 VD1 3 VD0 2 5SRLD 15 5CBLB 9 6 5SCLK 7 — LS166 12B — SI S/L CLR CI CLK

13 — 04 11F — 12 SCGVID

CHARACTER GENERATOR VIDEO OUTPUT SHIFT REGISTER

CHARACTER IMAGE STORAGE

See Page 3 for Alternate: RAM used for PROGRAM generated changeable imagery.

PROM POWER & SIGNAL SELECTION

NO SHUNT USED THIS GAME

10B

-5 1 +5. 2 GSWR 3 4 A10 5 6 +12 7 VD7A10 8 — 16 VRP21 15 14 13 VRP20 12 11 VRP19 10 9

DIP SHUNT NOT USED THIS GAME

6502 GAME LOGIC PCB

SCALE:	APPROVED BY: JKG	DRAWN BY
DATE: 6-12-81		REVISED E

VIDEO RAM CHARACTER GENERATOR AND SHIFT REGISTER

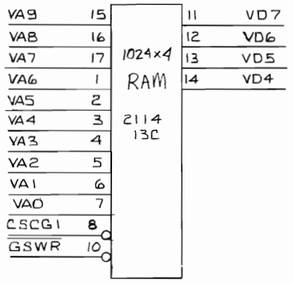
2 OF 8

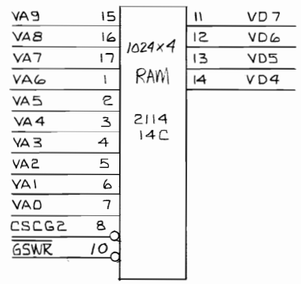
DRAWING NUMBER 77-3374-11

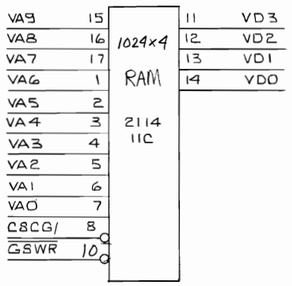
23234 PRINTED ON NO. 1000H CLEARPRINT

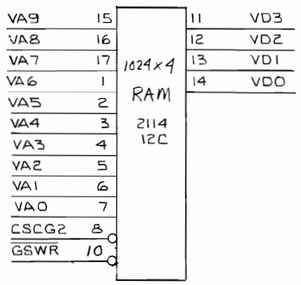
CHARACTER GENERATOR
IMAGE STORAGE RAMS

For use with PROGRAM
generated changeable imagery.









6502 GAME LOGIC PCB

SCALE:	APPROVED BY: AKJ	DRAWN BY
DATE: 6-12-81		REVISED E
IMAGE STORAGE RAM		
3 OF 8		DRAWING NUMBER 77-3374-11

22234 PRINTED ON NO. 1000H CLEARPRINT

CPU

BUSS DRIVERS

PAGE ZERO, ONE & SCRATCHPAD RAM

JØ

IRQ 4 — 4 IRQ

+5V 1.8K 2 — 2 RDY

+5V 1.8K 6 — 6 NMI

+5V 1.8K 38 — 38 SO

CPU CONTROL INPUTS

Inactive This game

CPU MASTER CLOCK → 1Ø0 37 — 37 ØO

+5V

POWER-UP RESET

R5 1.8K

+ 33 C42

R8 1.8K

R9 1.8K

07 2C

40 RESET

ANTI-SLAM

J1-L

R6 2.7K

R11 2.7K

+ 33 C43

+5V

STATIC ANTENNA INPUT

J1-A

.1 C7

R7 1.8K

R10 2.7K

07 2C

JØ 40 RESET

6502 2A

JØ

A15 25 — 25 — 2 A — Y 18 — A15

A14 24 — 24 — 4 — 16 — A14

A13 23 — 23 — 6 — 14 — A13

A12 22 — 22 — 8 — 12 — A12

A11 20 — 20 — 11 LS241 3B — 9 — A11

A10 19 — 19 — 13 — 7 — A10

A9 18 — 18 — 15 — 5 — A9

A8 17 — 17 — 17 — 3 — A8

1 1G

PUP 19 2G

A7 16 — 16 — 2 A — Y 18 — A7

A6 15 — 15 — 4 — 16 — A6

A5 14 — 14 — 6 — 14 — A5

A4 13 — 13 — 8 — 12 — A4

A3 12 — 12 — 11 LS241 3A — 9 — A3

A2 11 — 11 — 13 — 7 — A2

A1 10 — 10 — 15 — 5 — A1

A0 9 — 9 — 17 — 3 — AØ

1 1G

PUP 19 2G

ADDRESS BUSS

SYNC 7 — 7 — 2 IA — IY 18 — SYNC

Ø1 3 — 3 — 4 — 16 — Ø1

Ø2 39 — 39 — 6 LS241 1A — 14 — Ø2

R/W 34 — 34 — 8 — 12 — R/W

1 1G

BUSS CONTROL & CPU GENERATED CLOCKS

D7 26 — 26 — 2 A — B 18 — D7

D6 27 — 27 — 3 — 17 — D6

D5 28 — 28 — 4 — 16 — D5

D4 29 — 29 — 5 — 15 — D4

D3 30 — 30 — 6 LS245 3C — 14 — D3

D2 31 — 31 — 7 — 13 — D2

D1 32 — 32 — 8 — 12 — D1

DØ 33 — 33 — 9 — 11 — DØ

19 ENA

SR/W 1 DIR

0

1

DATA BUSS

VSS VSS VCC

1 21 8

JØ 8 1 21 +5V

R/W 9 — 04 4D — 8 — SR/W

SR/W 1

Ø2 2 — LS00 3D — 3 — WRITE

A9 15 — 1024 x 4 RAM 2114 4A — 11 — RD7 — 2 A — B 18 — D7

A8 16 — 12 — RD6 — 3 — 17 — D6

A7 17 — 13 — RD5 — 4 — 16 — D5

A6 1 — 14 — RD4 — 5 — 15 — D4

A5 2 — RD3 — 6 — 14 — D3

A4 3 — RD2 — 7 — 13 — D2

A3 4 — RD1 — 8 — 12 — D1

A2 7 — RDO — 9 — 11 — DO

A1 6 — BBSEL 19 — ENA

A0 5 — R/W 1 — DIR

RAMSEL 8 — 0

WRITE 10 — 1

74LS245 4C

A9 15 — 1024 x 4 RAM 2114 5A — 11

A8 16 — 12

A7 17 — 13

A6 1 — 14

A5 2

A4 3

A3 4

A2 7

A1 6

A0 5

RAMSEL 8

WRITE 10

MAIN ADDRESS DECODING

AI5 15 — A7 D3 — 9 — 3 — C — 7 — 7

AI4 1 — 10 — 2 — B — 6 — 9

AI3 2 — 11 — 1 — A — 5 — 10 — ABSEL

AI2 3 — PROM 6301 OR 74S287 5C — 12 — 6 — LS138 5D — G1 — 4 — 11 — IOSEL

AI1 4 — 5 — G2 — 3 — 12 — MISEL

AI0 7 — 4 — G3 — 2 — 13 — VSEL

A9 6 — 1 — 14 — RONSEL 13

A8 5 — A0 — 14 — G1 — 0 — 15 — RAMSEL 12

13 G1

LS08 5E — 11 — BBSEL

PROG. # VEL 5C-1

NOTE: Connector JØ used for test & analysis purposes only. Contains all CPU connections.

6502 GAME LOGIC PCB

SCALE: — APPROVED BY: AKJ — DRAWN BY

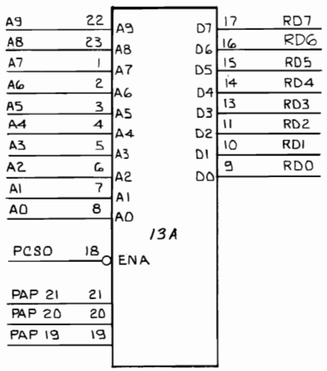
DATE 6-12-81 — REVISED E

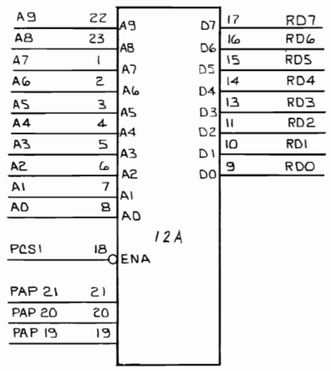
RESET: CPU: PROGRAM RAM BUS ARCHITECTURE

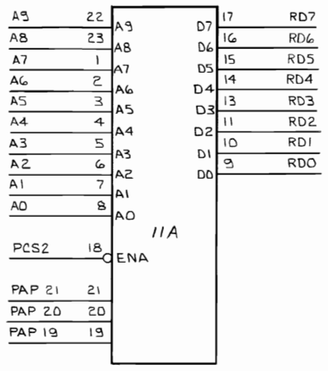
4 OF 8 — DRAWING NUMBER 77-3374-11

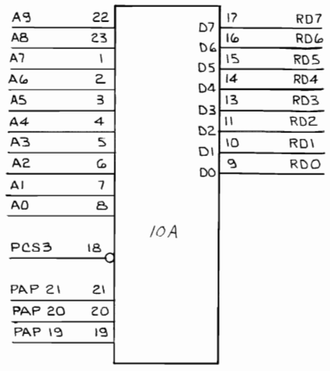
22X34 PRINTED ON NO. 1000H CLEARPRINT

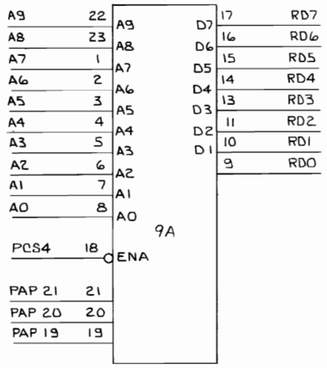
PROGRAM MEMORY

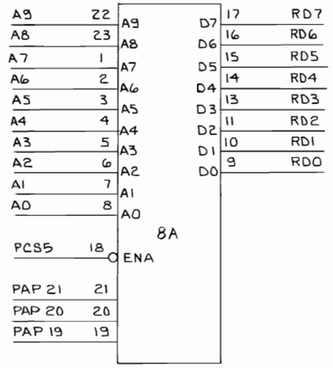


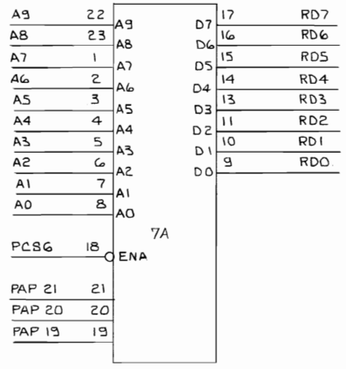


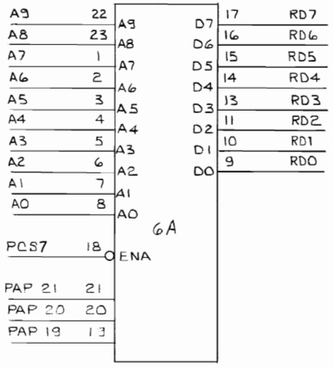






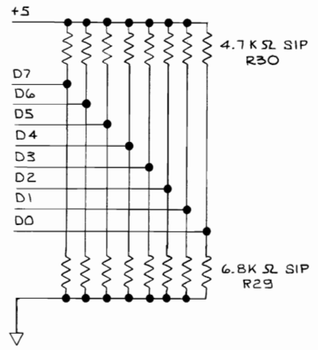


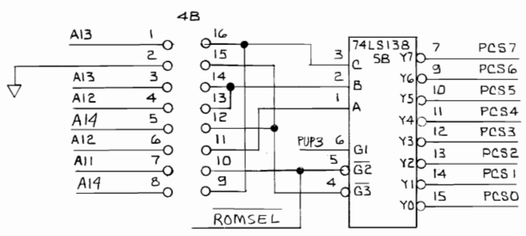




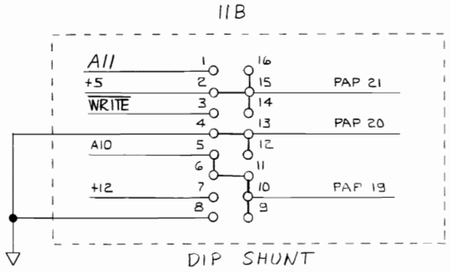
DATA BUSS TERMINATION

Ringing Suppression





PROM ADDRESS SELECTION

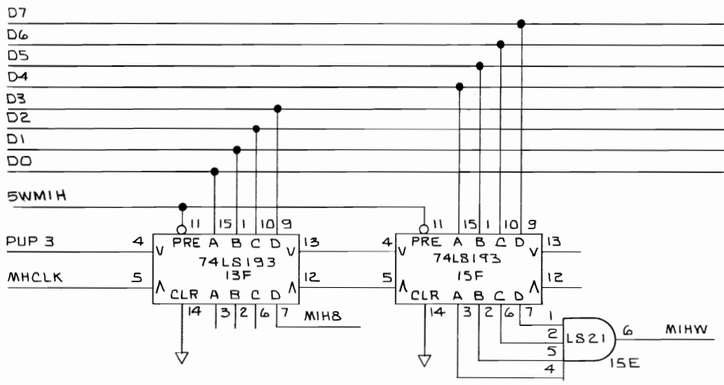


MEMORY DEVICE PERSONALITY SELECTION

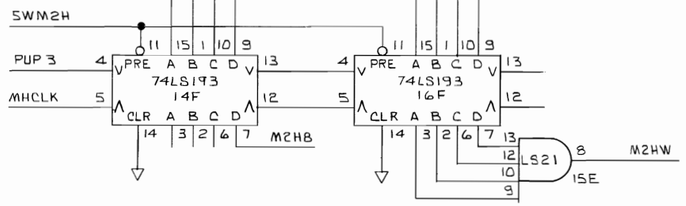
EXIDY INC.		
SCALE:	APPROVED BY: GKA	DRAWN BY
DATE: 6-12-81		REVISED E
6502 GAME LOGIC PCB CPU ROM		
5 OF 8		DRAWING NUMBER 77-3374-11

22X34 PRINTED ON NO. 1000H CLEARPRINT

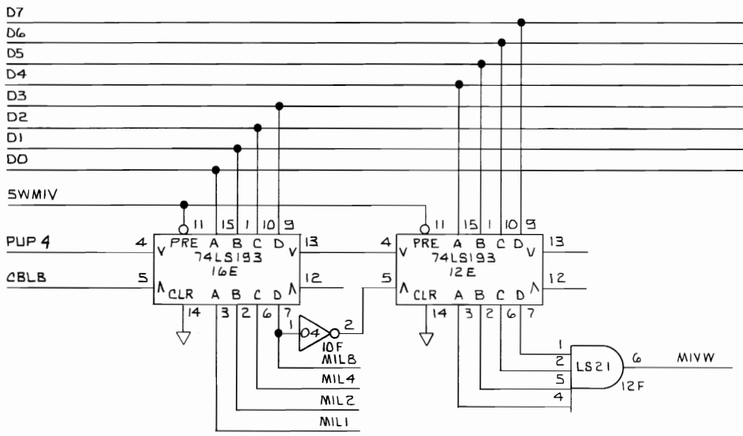
MOVING OBJECT 1
HORZ. COUNTERS



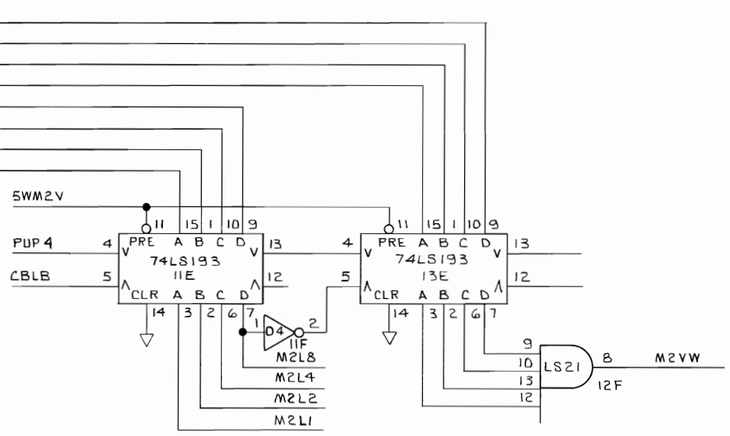
MOVING OBJECT 2
HORZ. COUNTERS

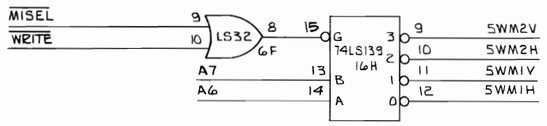


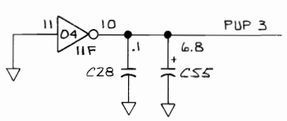
MOVING OBJECT 1
VERTICAL COUNTERS

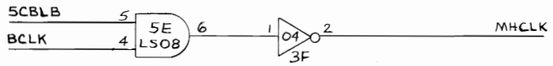


MOVING OBJECT 2
VERTICAL COUNTERS

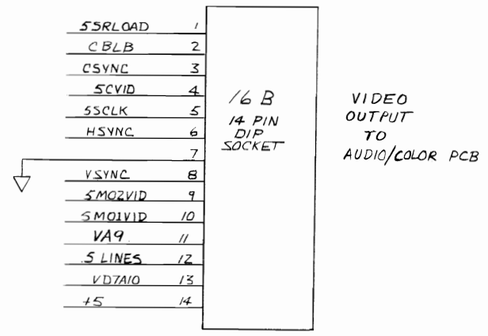








'WRITE MOVING OBJECT' DECODING



6502 GAME LOGIC PCB

SCALE:	APPROVED BY: AKG	DRAWN BY
DATE 6-12-81		REVISED E

COLOR INTERFACE OUTPUT AND
MOVING OBJECT POSITION COUNTERS

6 OF 8

DRAWING NUMBER 77-3374-11

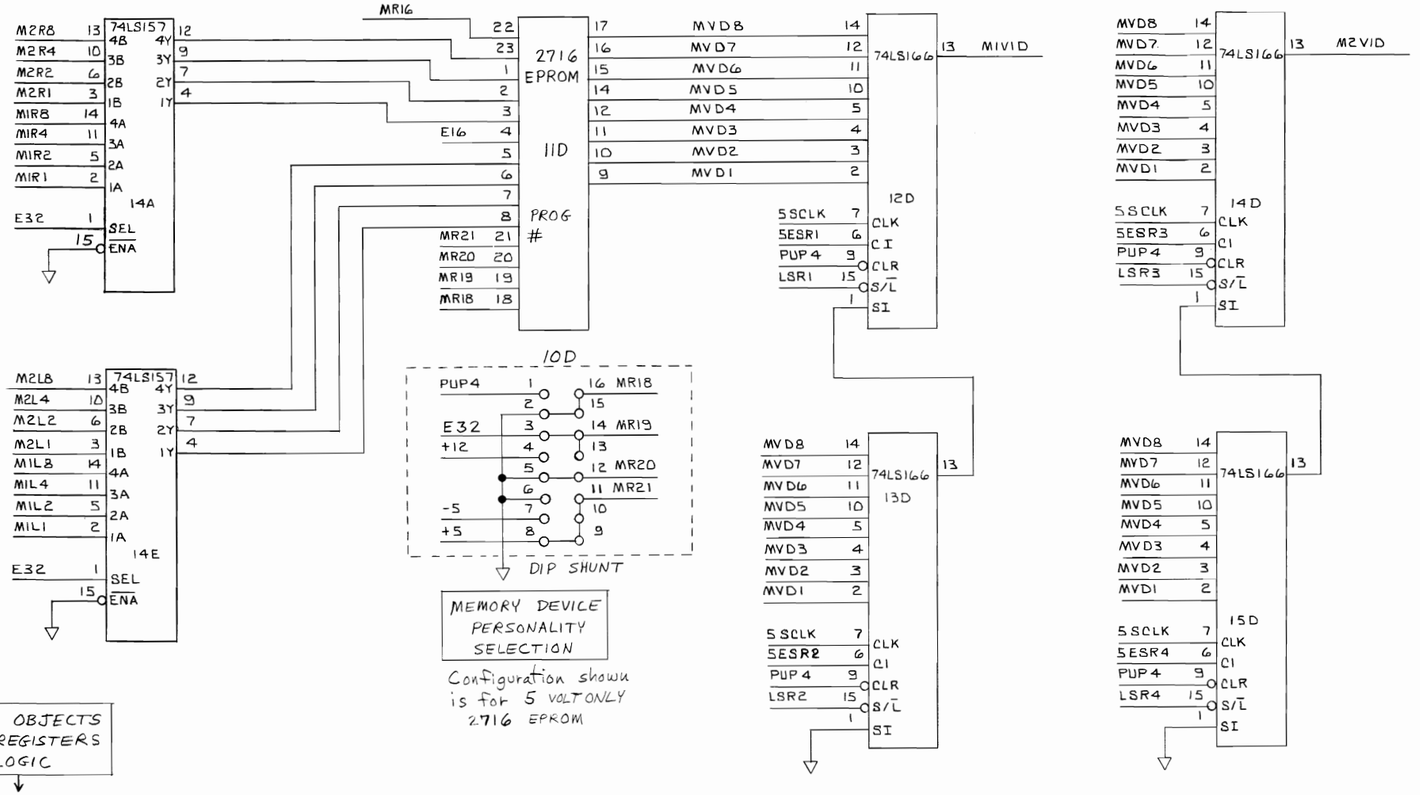
33334 PRINTED ON NO. 1000H CLEARPRINT

MOVING OBJECTS MULTIPLEXING

MOVING OBJECTS IMAGE STORAGE

MOVING OBJECT 1 VIDEO OUTPUT SHIFT REGISTER

MOVING OBJECT 2 VIDEO OUTPUT SHIFT REGISTER



MOVING OBJECTS SHIFT REGISTERS LOAD LOGIC

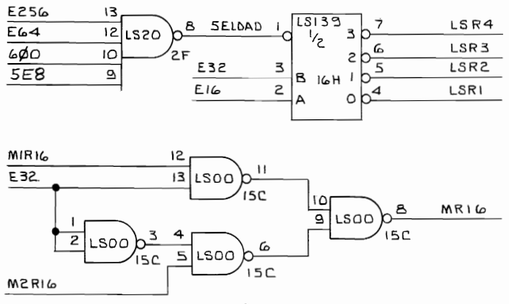
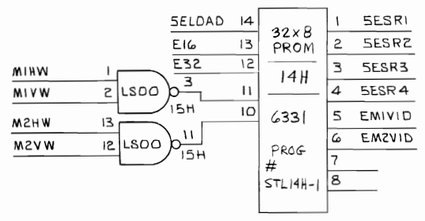
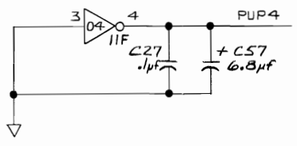


IMAGE SELECTION LOGIC
(Which Moving Object?)



MOVING OBJECTS SHIFT REGISTER CONTROL LOGIC



6502 GAME LOGIC PCB

SCALE:	APPROVED BY: AKJ	DRAWN BY
DATE: 6-12-81		REVISED E

MOVING OBJECT VIDEO GENERATION

7 OF 8

DRAWING NUMBER 77-3374-11

88884 PRINTED ON NO. 1000H CLEARPRINT

A/D CONVERSION

Not used

A/D CONVERTER LATCH

LS374 (8D)

L128	18	D	Q	19
L64	17			16
L32	14			15
L16	13	NOT USED		12
L8	3			2
L4	4			5
L2	7			6
L1	8			9
SEAD	1	OC		
	11	CLK		

S1 SELECTABLE OPTIONS DIPSWITCH

16A

+5V, 2.2K (SIP)

TABLE

OPTION SWITCH PORT

74LS241 (15A)

	11	A	Y	9
	13			7
	15			5
	17			3
	8			12
	6			14
	4			16
COIN2	2			18
5EDIP	1	$\overline{1G}$		
	19	2G		

13 — 04 — 12 (10F)

MOVING OBJECT IMAGE LATCH

LS374 (14B)

	18	D	Q	19	M2R8
	17			16	M2R4
	14			15	M2R2
	13			12	M2R1
	3			2	M1R8
	4			5	M1R4
	7			6	M1R2
	8			9	M1R1
SWMOL	11	CLK			
	1	$\overline{OC}$			

MIADO / M2ADO

MIADO = 1 · ADSEL = 2 · LS00 (13H) = 3

M2ADO = 13 · 12 · LS00 (13H) = 11

MIADO · M2ADO = 10 · 9 · LS00 (13H) = 8

3 · 5 · LS00 (13H) = 6 → L128

NOT USED

R19 10K · R20 910K · C58 .01 · C59 .02 · R26 1M

J1-Z · VSYNC · CR3 IN4454 · R23 1K · +5V · 680K R22

LM3900 (12H) → MIADO

R24 100K · R28 910K · C60 .01 · C61 .02 · R27 1MEG

J1-22 · VSYNC · CR4 IN4454 · R25 1K · +5V · 680K R21

LM3900 (12H) → M2ADO

+5V 220Ω SIP R18 (18Ω ×8)

R300 · R301 · R302 · R303 · R304 · R305 · R306 · R307

J1-E · J1-S · J1-F · J1-6 · J1-H · J1-7 · J1-J · J1-8

CR1 · 1µF (8) C45 · C52 · 5ESR

CR2 IN4002 (2)

CONTROL INPUT PORT

74LS241 (9E)

5COIN1	2	A	Y	18
DOWN	4			16
UP	6			14
FIRE	8			12
LEFT	17			3
RIGHT	15			5
2START	13			7
1START	11			9
CR1	1	$\overline{1G}$		
	19	2G		

5 — 04 — 6 (10F)

AUDIO BOARD PORT

LS245 (15B)

	2	A	B	18	ABD7	J3-1
	3			17	ABD6	J3-2
	4			16	ABD5	J3-3
	5			15	ABD4	J3-4
	6			14	ABD3	J3-5
	7			13	ABD2	J3-6
	7			12	ABD1	J3-7
	9			11	ABD0	J3-8
ABSEL	19	$\overline{ENA}$				
S R/W	1	DIR				

D7 · D6 · D5 · D4 · D3 · D2 · D1 · D0 — DATA BUSS

I/O DECODING

LS139 (7E) · LS32 (6F)

IOSEL 13 · WRITE 12 → LS32 (6F) 11 → 15 → LS139 (7E) G ½

A1 13 · A0 14 → B, A

9		
10		
11	5WCPL	
12	5WMOL	

IOSEL 2 · S R/$\overline{W}$ 1 → LS32 (6F) 3 → LS139 (7E) G ½

A1 3 · A0 2 → B, A

7	5EIR	
6	5EAD	
5	5ESR	
4	5EDIP	

+5V · CR200 IN4002 · R200 220 · 18Ω R308 · J1-Y · C200 .1

AUXILIARY COIN INPUT

50 Pence etc.

5COIN2

INTERRUPT DECODING

CBLB · 5MOIVDT · 5FVID · 5M02VDT · 5MOVID · L256 · 5VCCRY · VCNTC

LS02 (8F) · LS27 (7F) · LS32 (6F)

1VL1 · VL1

INTERRUPT CONDITION LATCH

+5V · R309 · R310 2.2K (×2) · LANGUAGE JUMPERS (SEE TEXT)

5COINT

74LS112 (8E): J · PRE · CLK · K · CLR · Q

BCLK 13 · SEIR

LS374 (8E)

SL256	18	D	Q	19
COIN1	17			16
COIN2	14			15
VDLV	13			12
TABLE	3			2
5MOIVID	4			5
LNG1	7			6
LNGØ	8			9
	11	CLK		
	1	$\overline{OC}$		

5WCPL

LS374 (9D)

	18	D	Q	19	ADSEL	
	17			16	M1R16	
	14			15	M2R16	
	13			12		
	3			2		J1-4
	4			5		J1-D
	7			6		J1-3
	8			9		J1-C
	11	CLK				J1-2
	1	$\overline{OC}$				

PERIPHERAL CONTROL LATCH

+5V · R4 1.2K · IRQ

5 — 07 — 6 (2C)

SIGNALS

A0	J2-5
A1	J2-4
A2	J2-3
A3	J2-2
Ø2	J2-10
WRITE	J3-9
ABSEL	J3-10
A4	J3-1
R/$\overline{W}$	J2-9
+5V	J2-6
$\overline{RESET}$	J2-8
	J2-7

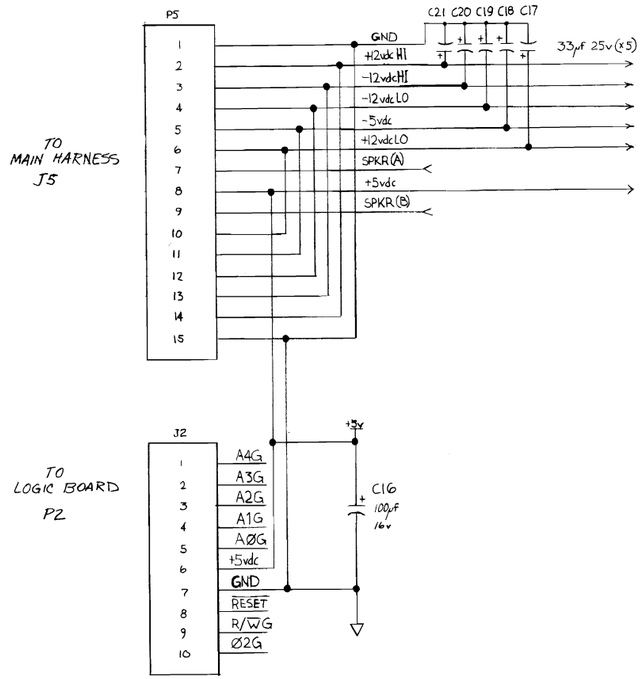
J1-R thru J1-V · J1-10 thru J1-21 · C44 470 · C23 .1 · +5V

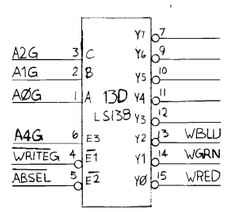
-5V — J1-N

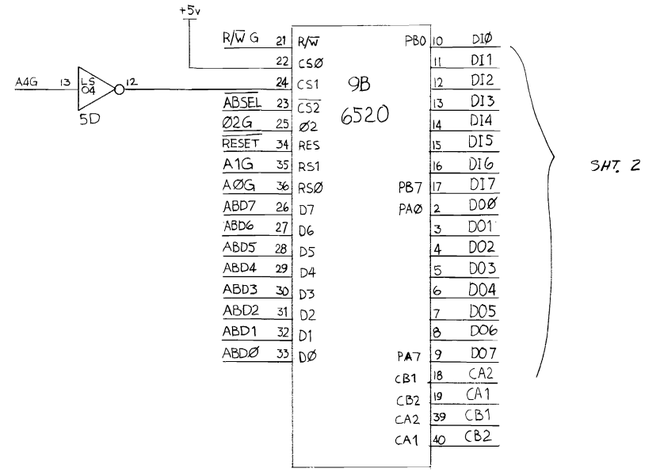
+12V — J1-M

SCALE:	APPROVED BY:	DRAWN BY	
DATE: 6-12-81		REVISED E	
6502 GAME LOGIC PCB I/O PORTS			
8OF8		DRAWING NUMBER 77-3374-11	

22X34 PRINTED ON NO. 1000H CLEARPRINT







NOTE:
ALL RESISTORS ARE ¼ WATT, 5%.
ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

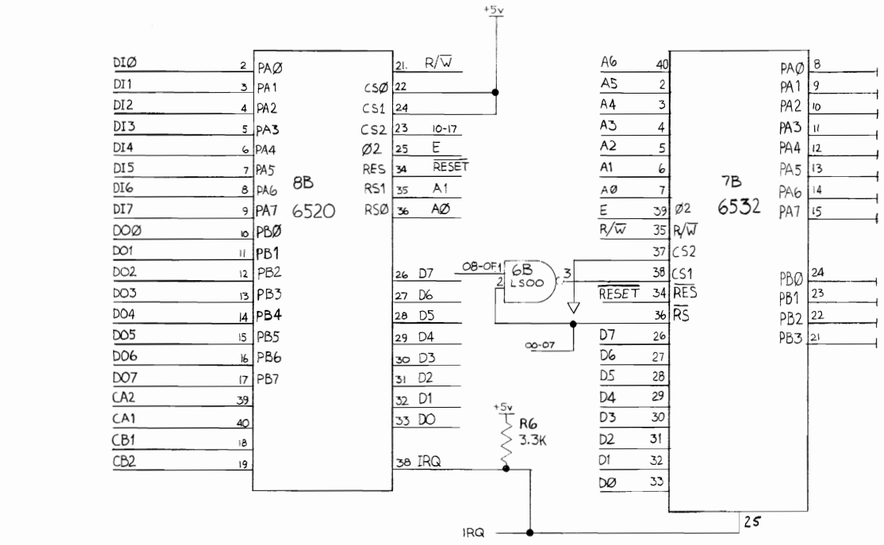
BYPASS .1µf FOR EVERY OTHER I.C.

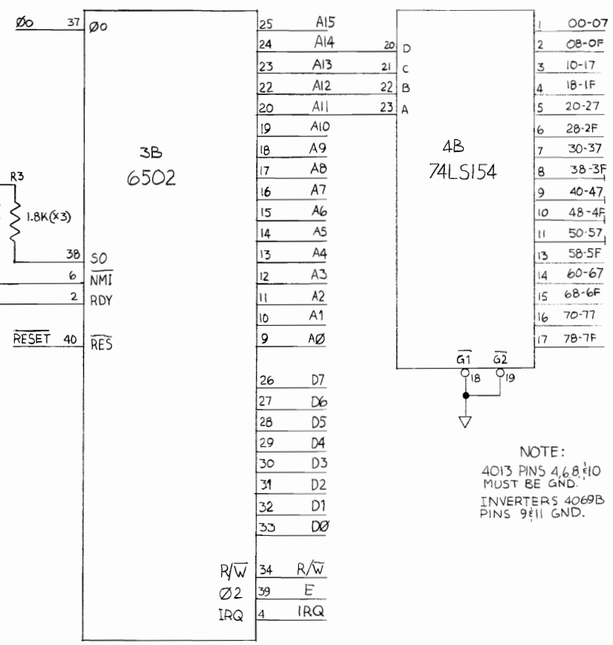
THIS TABLE REFERS TO POWER & GND PINS NOT SCHEMATICALLY REPRESENTED.

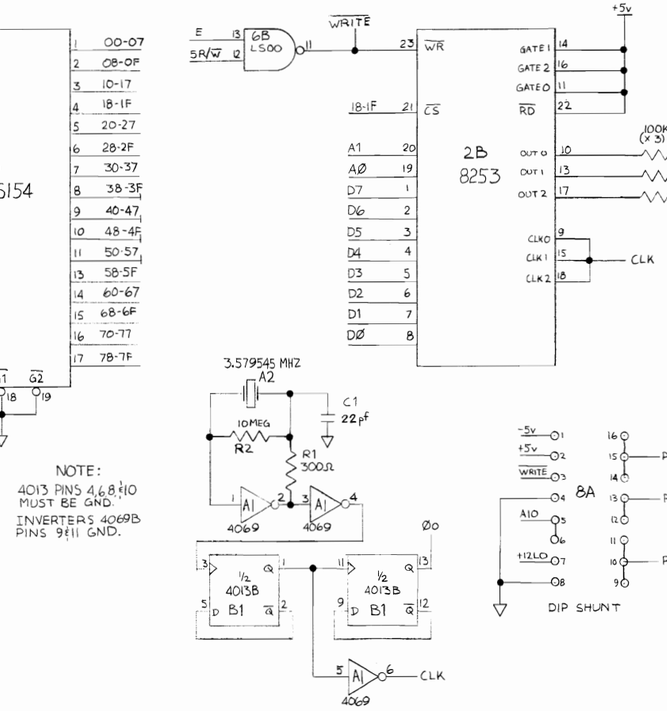
DEVICE TYPE	+5v	GND
6520	20	1
4069	14	7
4013	14	7
6502	8	1,21
6532	20	1
LS154	24	12
8253	24	12
LS00	14	7
LS374	20	10
LS138	16	8
LS86	14	7
LS139	16	8
4175	16	8
4053	16	8
LS74	14	7
LS04	14	7
7406	14	7
4175	16	8
4051	16	8
4562	14	7
74151	16	8
74148	16	8
LS174	16	8

NOTES UNLESS OTHERWISE SPECIFIED: 13

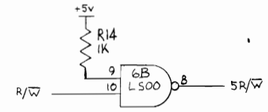
PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING: DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY: NEAL R. ZOOK	DATE: 6-8-81	ENGINEER: MARK VON STRIVER	DATE: 6-8-81	SCALE: DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS	FINISH / DECIMALS / ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	TITLES/DESCRIPTION: AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 1 OF 5	CODE	DRAWING NO.: 77-3387-11	REV.: A
		CHECKED: MARK VON STRIVER	DATE: 6-8-81	PROJECT ENGINEER	DATE												

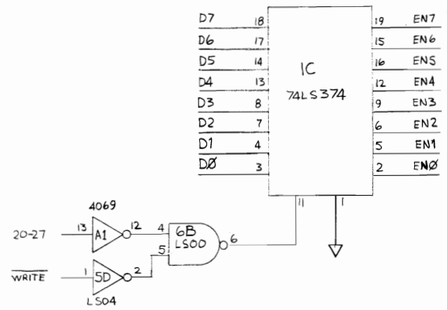


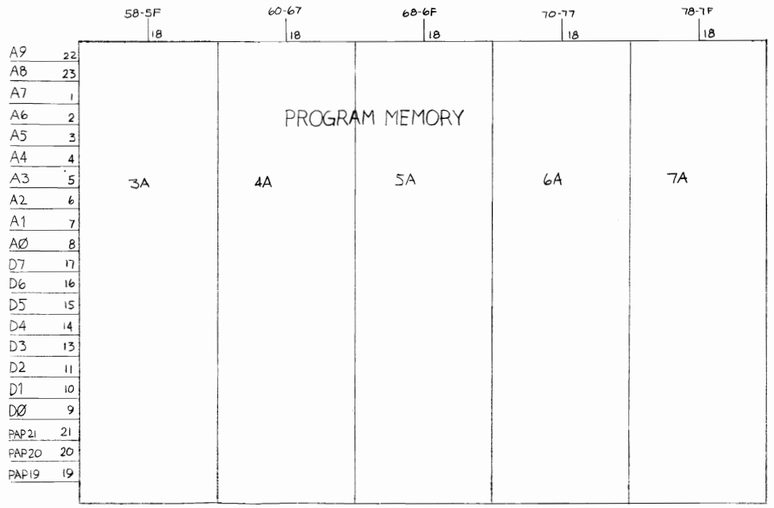




NOTE:
4013 PINS 4,6,8,10 MUST BE GND.
INVERTERS 4069B PINS 9&11 GND.

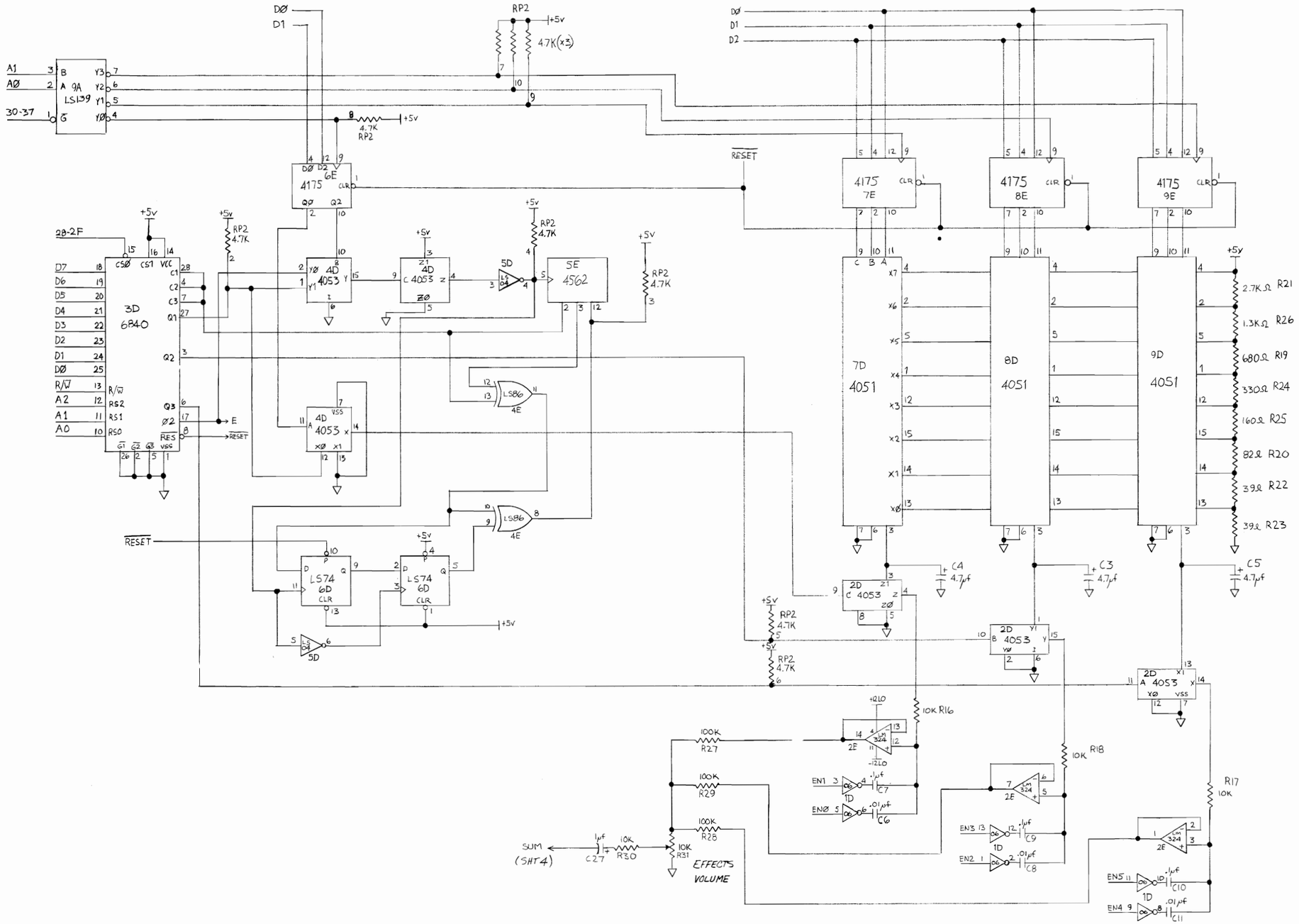






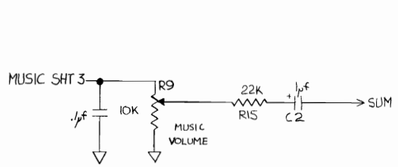
NOTES UNLESS OTHERWISE SPECIFIED: 12

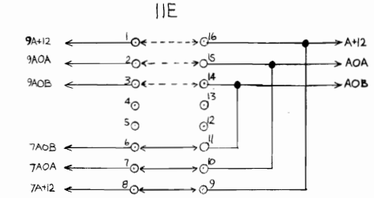
PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING: DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY: NEAL R. ZOOK	DATE: 6-5-81	ENGINEER: MARK VON STRIVER	DATE: 6-6-81	SCALE: DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS: ±	FINISH / DECIMALS: .XX ± .XXX ± / ANGLES: ± °	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	TITLES/DESCRIPTION: AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 2 OF 5	CODE	DRAWING NO.: 77-3387-11	REV.: A
		CHECKED: MARK VON STRIVER	DATE: 6-6-81	PROJECT ENGINEER	DATE										



PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	**DESIGN DRAWING** DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY NEAL R. ZOOK	DATE 6-9-81	ENGINEER MARK VON STRIVER	DATE 6-9-81	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS	FINISH / DECIMALS / ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLES/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 3 OF 5	CODE	DRAWING NO. 77-3387-11	REV. A
		CHECKED MARK VON STRIVER	DATE 6-9-81	PROJECT ENGINEER	DATE														

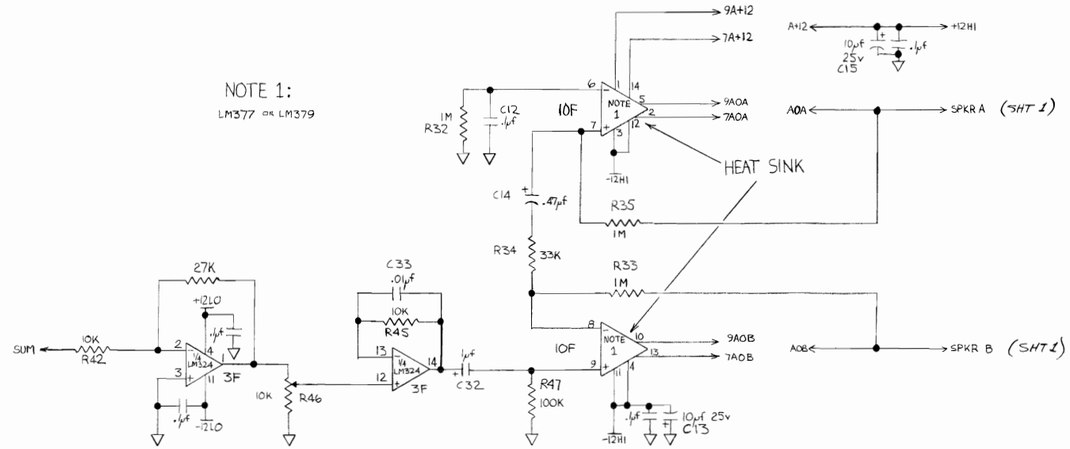
NOTES UNLESS OTHERWISE SPECIFIED:





DIP SHUNT CONFIGURATION
DOTTED LINE FOR LM379
SOLID LINE FOR LM377

NOTE 1:
LM377 OR LM379



PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	**DESIGN DRAWING** DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY NEAL R. ZOOK	DATE 6-9-81	ENGINEER MARK VON STRIVER	DATE 6-9-81	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS	FINISH / DECIMALS .xx± .xxx± / ANGLES ± °	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLES/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 4 OF 5	CODE	DRAWING NO. 77-3387-11	REV. A
		CHECKED MARK VON-STRIVER	DATE 6-9-81	PROJECT ENGINEER	DATE														

NOTES UNLESS OTHERWISE SPECIFIED:

J20

14 PIN DIP SOCKET CONNECTOR

FROM LOGIC PCB J4

1	5$RLD
2	CBLB
3	5CSYNC
4	5CVID
5	5$CLK
6	HSYNC
7	GND
8	VSYNC
9	5M02VID
10	5M01VID
11	VA9
12	5LINES
13	VD7A10
14	+5VDC

PATTERN CHARACTER COLOR DIVISION

BLUE DATA LATCH

GREEN DATA LATCH

RED DATA LATCH

ABD0
ABD1
ABD2
ABD3
ABD4
ABD5
ABD6
ABD7
WBLU
WGRN
WRED

L$ 374 11C

COLOR SELECTION

11B 151
12B 151
13B 151

BLU
GRN
RED

VIDEO POLARITY
"VID"
CUT FOR LOW=TRUE
+5V
330 R7

11A L$ 86
BLUA
GRNA
REDA

SYNC POLARITY
"SYNC"
CUT FOR LOW=TRUE
330 R8

12A L$ 86
5CSYNC
HSYNC
VSYNC
CSYNCA
HSYNCA
VSYNCA

PRIORITY ENCODER

9A L$ 139

10B 148

5M01VID
5M02VID
5LINES
CSPACE3
CSPACE2
CSPACE1
CSPACE0
BACKGND
PRI2
PRI1
PRI0

VD7A10
VA9
5$RLD
5CVID

L$ 74 10A

P21

10 PIN WAFER HEADER

REDA	3	2	RED OUT
GRNA	4	5	GRN OUT
BLUA	6	7	BLU OUT
CSYNCA	11	10	CSYNC OUT
HSYNCA	13	12	HSYNC OUT
VSYNCA	14	15	VSYNC OUT

13A L$ 174

5$CLK

OUTPUT TO TV MONITOR (THRU MAIN HARNESS)

PROPRIETARY	DRAWN BY	DATE	ENGINEER	DATE	SHEET OF	NEXT ASSEMBLY	USED ON
THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	AKH	6-7-81	AKH	6-7-81	5 5		
	CHECKED	DATE	PROJECT ENGINEER	DATE			
	AKH	6-22-81	AKH	6-7-81			

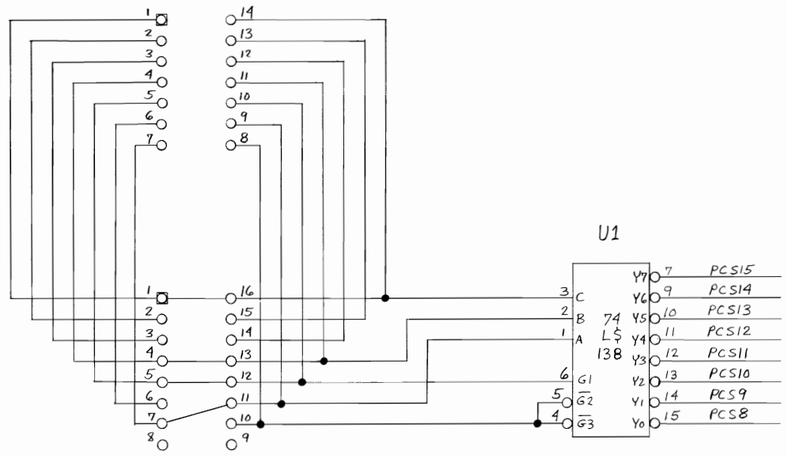
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE	TITLE/DESCRIPTION	SHEET OF	CODE	DRAWING NO.	REV
D	AUDIO/COLOR PCB SCHEMATIC DIAGRAM	5 OF 5		77-3387-11	A

NOTES:
1. For EPROMS +5V (VCC) = PIN 24
   GND = PIN 12
2. 10 EA. BYPASS CAPS NOT SHOWN,
   Between +5VDC and GND. VALUE = .1µf 10V(MIN)
   (Ceramic OK)

J1

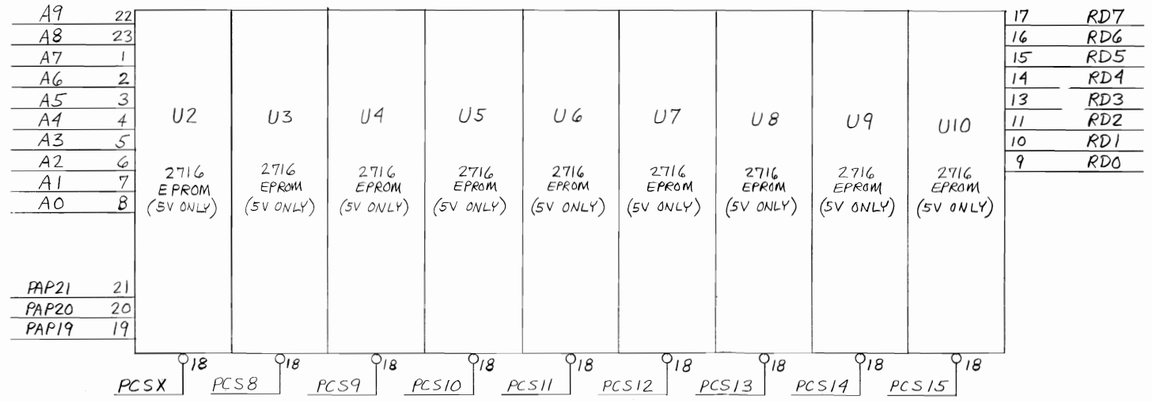
14 PIN DIP SOCKET
(FROM LOGIC PCB POSITION 4B)



JPR1

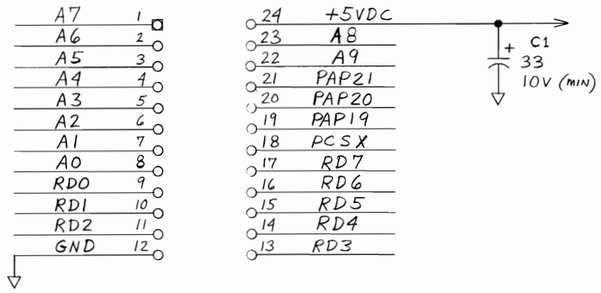
16 PIN DIP PATTERN
w/JPRS included as shown
(May double as 16 PIN input socket)

All lines BUSSED TOGETHER except CHIP SELECTS (PCS0, PCS8–PCS15)



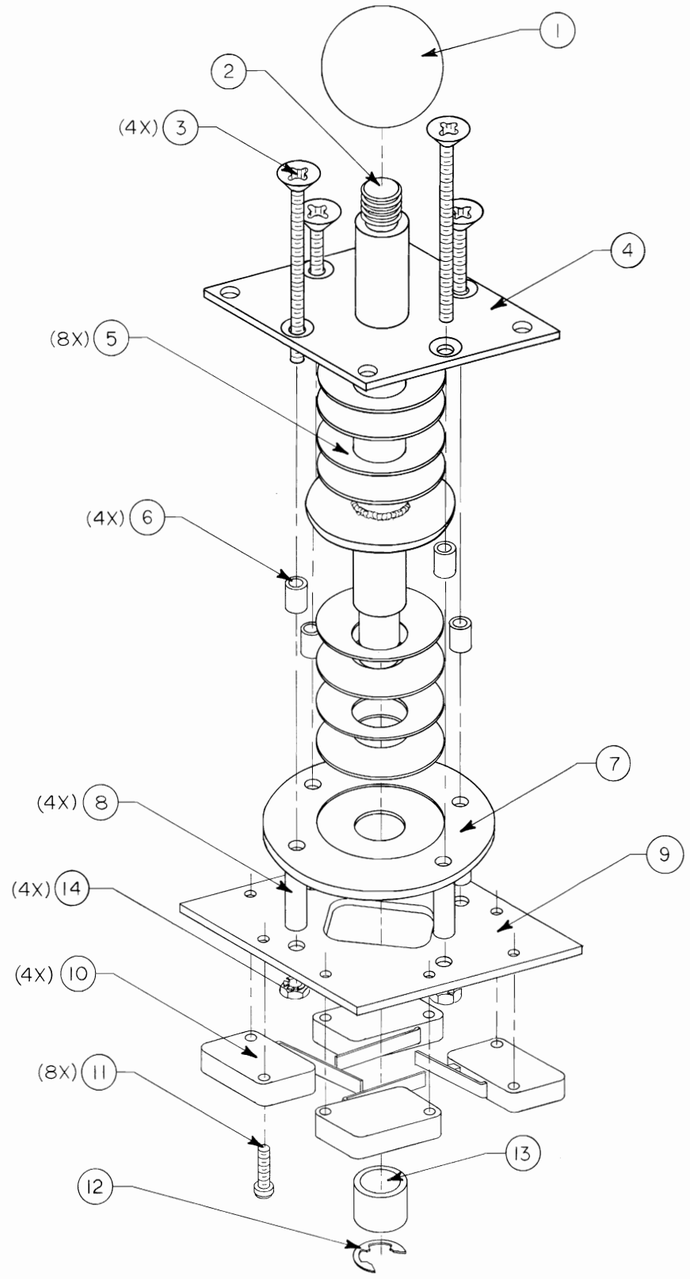
J2

24 PIN DIP SOCKET
(FROM LOGIC PCB POSITION 13A)



14

PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DRAWN BY: AKY	DATE: 6-11-81	ENGINEER: AKY	DATE: 6-11-81	SHEET 1 OF 1	NEXT ASSEMBLY: 77-3374-14 REV E	USED ON: 6502 LOGIC PCB FOR EXPANDED MEMORY	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	TITLE/DESCRIPTION: MEMORY EXPANSION PCB (77-3389-14) SCHEMATIC	CODE	DRAWING NO.: 77-3389-11	REV: A
	CHECKED: AKY	DATE: 6-11-81	PROJECT ENGINEER: AKY	DATE: 6-11-81									



ITEM NO.	QTY	DRAWING NO.	DESCRIPTION
14	4	74-6506	NUT, KEP
13	1	74-5466	BUSHING
12	1	74-5467	RING RETAINING
11	8	74-5189	SCREW, PAN HD.
10	4	72-3063	SWITCH
9	1	68-0127-10	PLATE, SWITCH
8	4	74-5212	SPACER
7	1	68-2031-10	DISC, LOWER
6	4	74-5248	SPACER
5	8	73-9081	WASHER, BELLEVILLE
4	1	68-0030-10	PLATE, UPPER
3	4	74-6525	SCREW, FL.HD.
2	1	97-1022-10	SHAFT
1	1	92-1021-10	KNOB

LIST OF MATERIAL

NOTES UNLESS OTHERWISE SPECIFIED:

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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

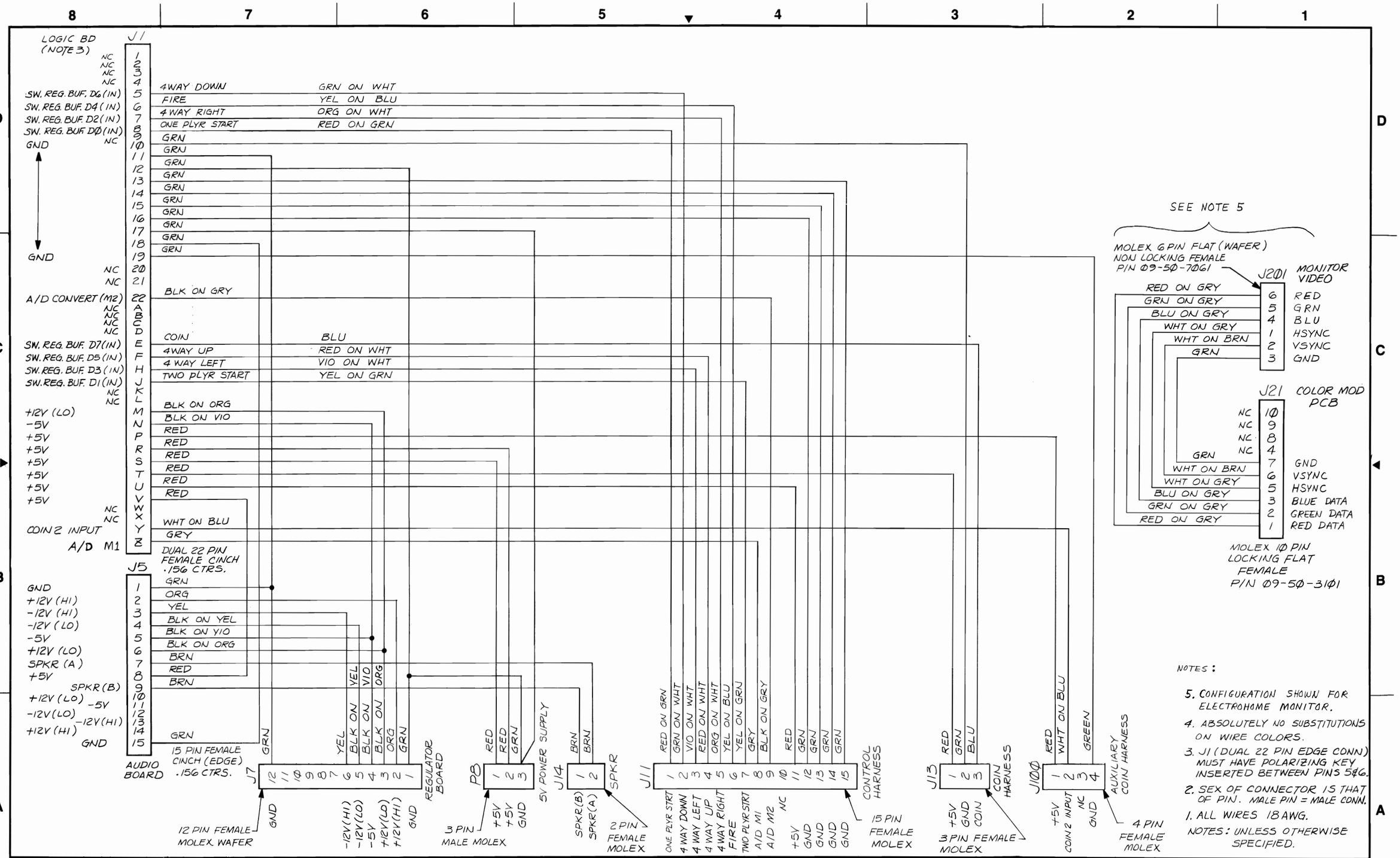
DRAWN BY NP — DATE 4/25/81
CHECKED — DATE
ENGINEER — DATE
PROJECT ENGINEER — DATE
SCALE DO NOT SCALE DRAWING
DATE OF ISSUE
MATERIAL — FINISH
TOLERANCES — FRACTIONS ± — DECIMALS .XX ± .XXX ± — ANGLES ±°

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE D

TITLE/DESCRIPTION: VENTURE TM JOY STICK-8 POSITION

SHEET 1 OF 1 — CODE — DRAWING NO. 38-5119-10 — REV. A



PROPRIETARY
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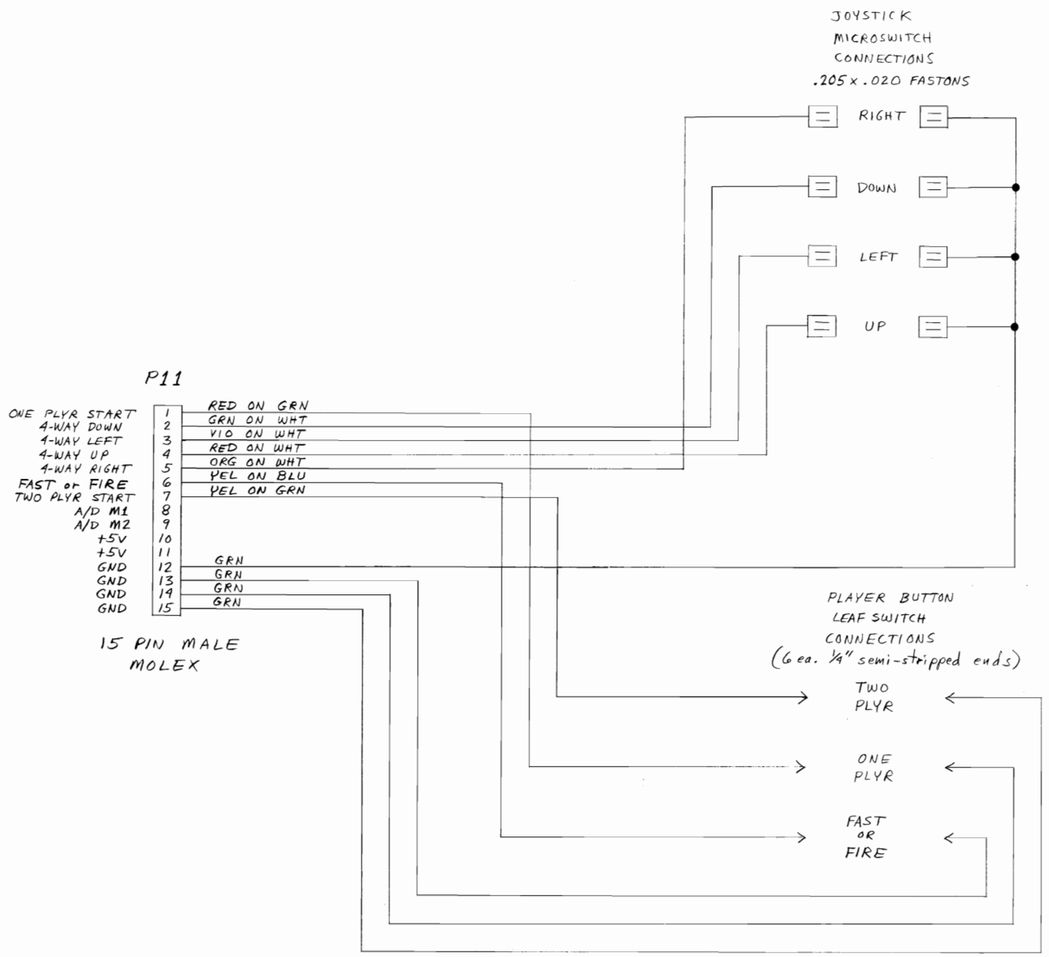
DRAWN BY	DATE	ENGINEER	DATE	SHEET	OF	NEXT ASSEMBLY	USED ON
MA Thompson	6/84			1	1		VENTURE™
CHECKED	DATE	PROJECT ENGINEER	DATE				

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE	TITLE/DESCRIPTION	CODE	DRAWING NO.	REV
D	6502 MAIN HARNESS COLOR	HR	71-2413-11	

CONTROL PANEL HARNESS SCHEMATIC

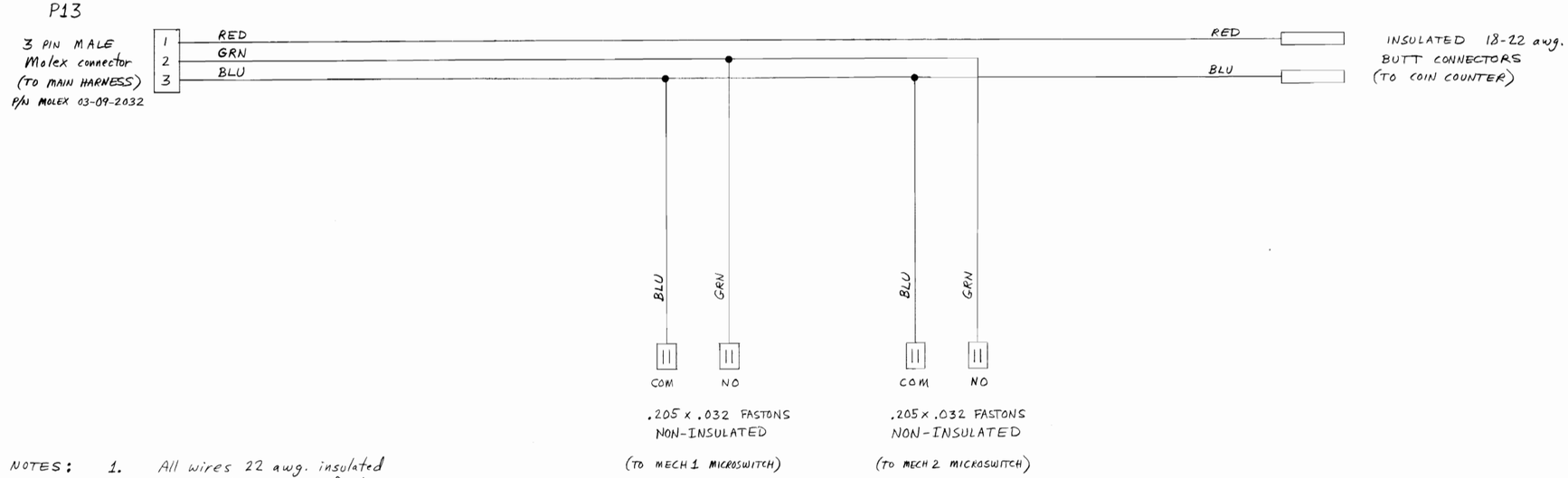


NOTES:
1. All wires 22 awg. insulated unless otherwise specified.
2. ABSOLUTELY NO SUBSTITUTIONS ON SPECIFIED WIRE COLORS

11-6-79

390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE	TITLE/DESCRIPTION	CODE	DRAWING NO.	RF#
	D	CONTROL PANEL HARNESS VENTURE™		30-3188	

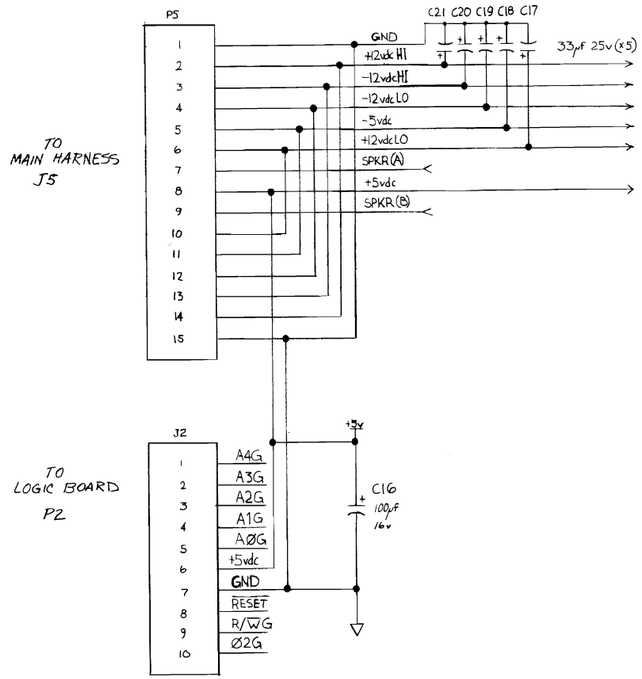
COIN HARNESS SCHEMATIC
(UNIVERSAL COIN HARNESS)

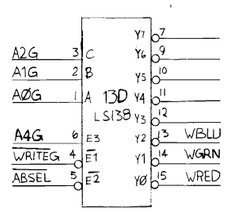


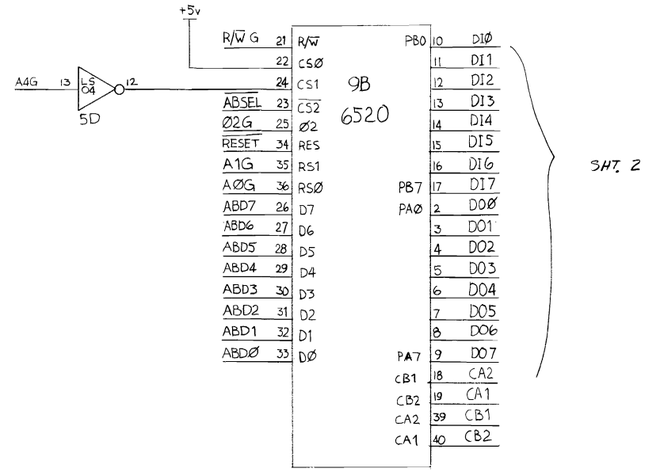
NOTES:

1. All wires 22 awg. insulated unless otherwise specified.
2. ABSOLUTELY NO SUBSTITUTIONS ON SPECIFIED WIRE COLORS

390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLE/DESCRIPTION UNIVERSAL COIN HARNESS VENTURE™	CODE	DRAWING NO. 30-3189	REV







NOTE:
ALL RESISTORS ARE ¼ WATT, 5%.
ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

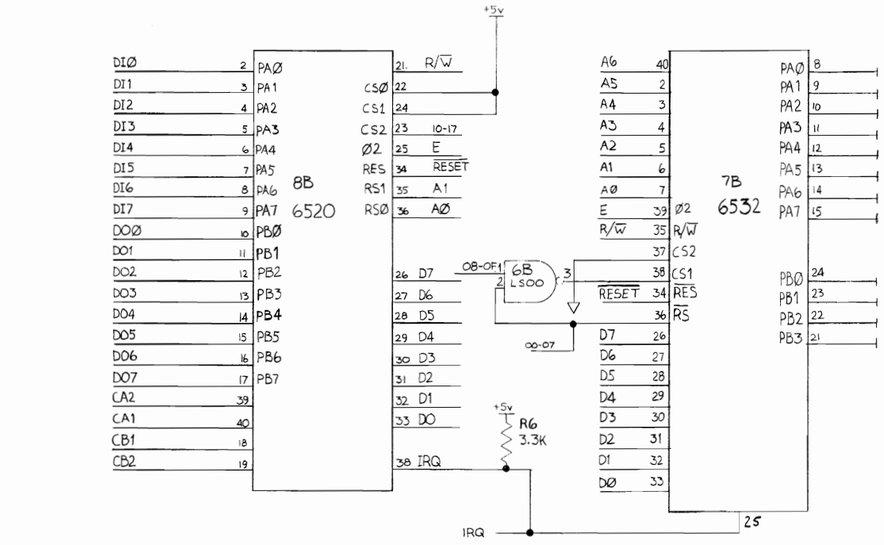
BYPASS .1µf FOR EVERY OTHER I.C.

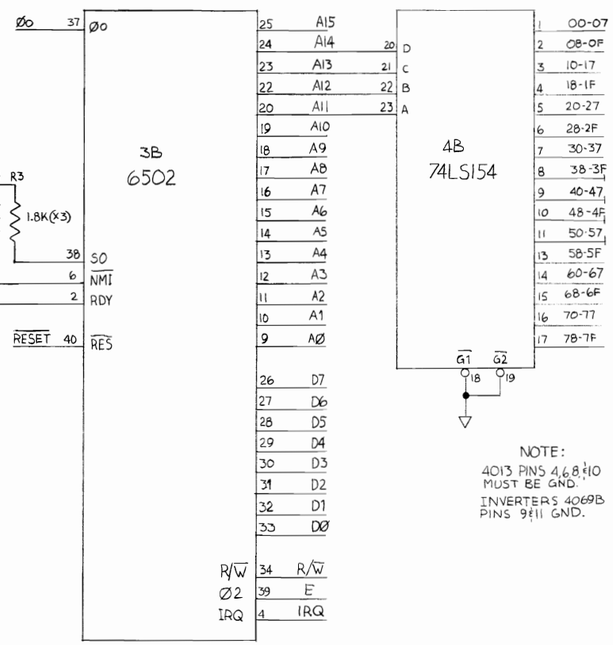
THIS TABLE REFERS TO POWER & GND PINS NOT SCHEMATICALLY REPRESENTED.

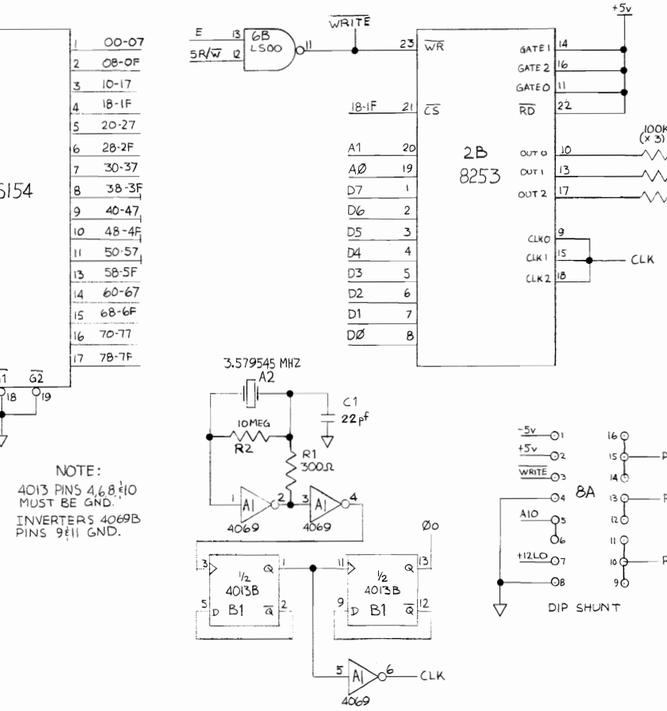
DEVICE TYPE	+5v	GND
6520	20	1
4069	14	7
4013	14	7
6502	8	1,21
6532	20	1
LS154	24	12
8253	24	12
LS00	14	7
LS374	20	10
LS138	16	8
LS86	14	7
LS139	16	8
4175	16	8
4053	16	8
LS74	14	7
LS04	14	7
7406	14	7
4175	16	8
4051	16	8
4562	14	7
74151	16	8
74148	16	8
LS174	16	8

NOTES UNLESS OTHERWISE SPECIFIED: 13

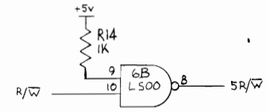
PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING: DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY: NEAL R. ZOOK	DATE: 6-8-81	ENGINEER: MARK VON STRIVER	DATE: 6-8-81	SCALE: DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS	FINISH / DECIMALS / ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	TITLES/DESCRIPTION: AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 1 OF 5	CODE	DRAWING NO.: 77-3387-11	REV.: A
		CHECKED: MARK VON STRIVER	DATE: 6-8-81	PROJECT ENGINEER	DATE												

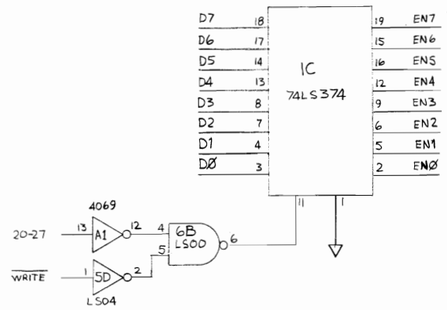


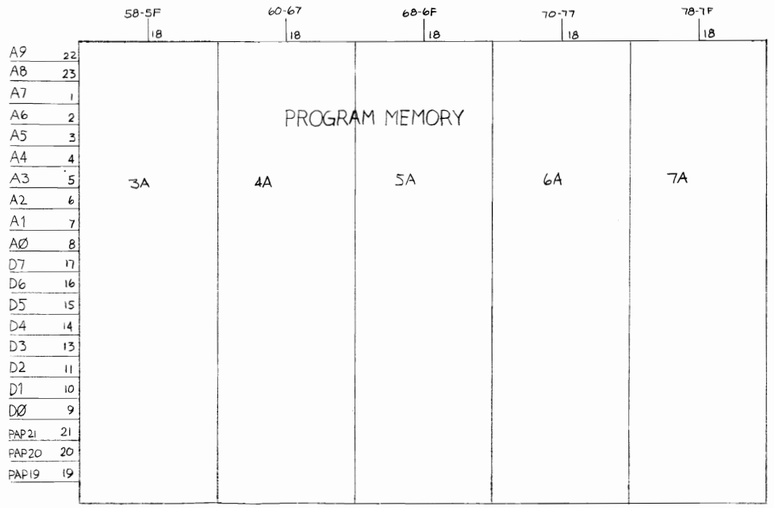




NOTE:
4013 PINS 4,6,8,10 MUST BE GND.
INVERTERS 4069B PINS 9&11 GND.

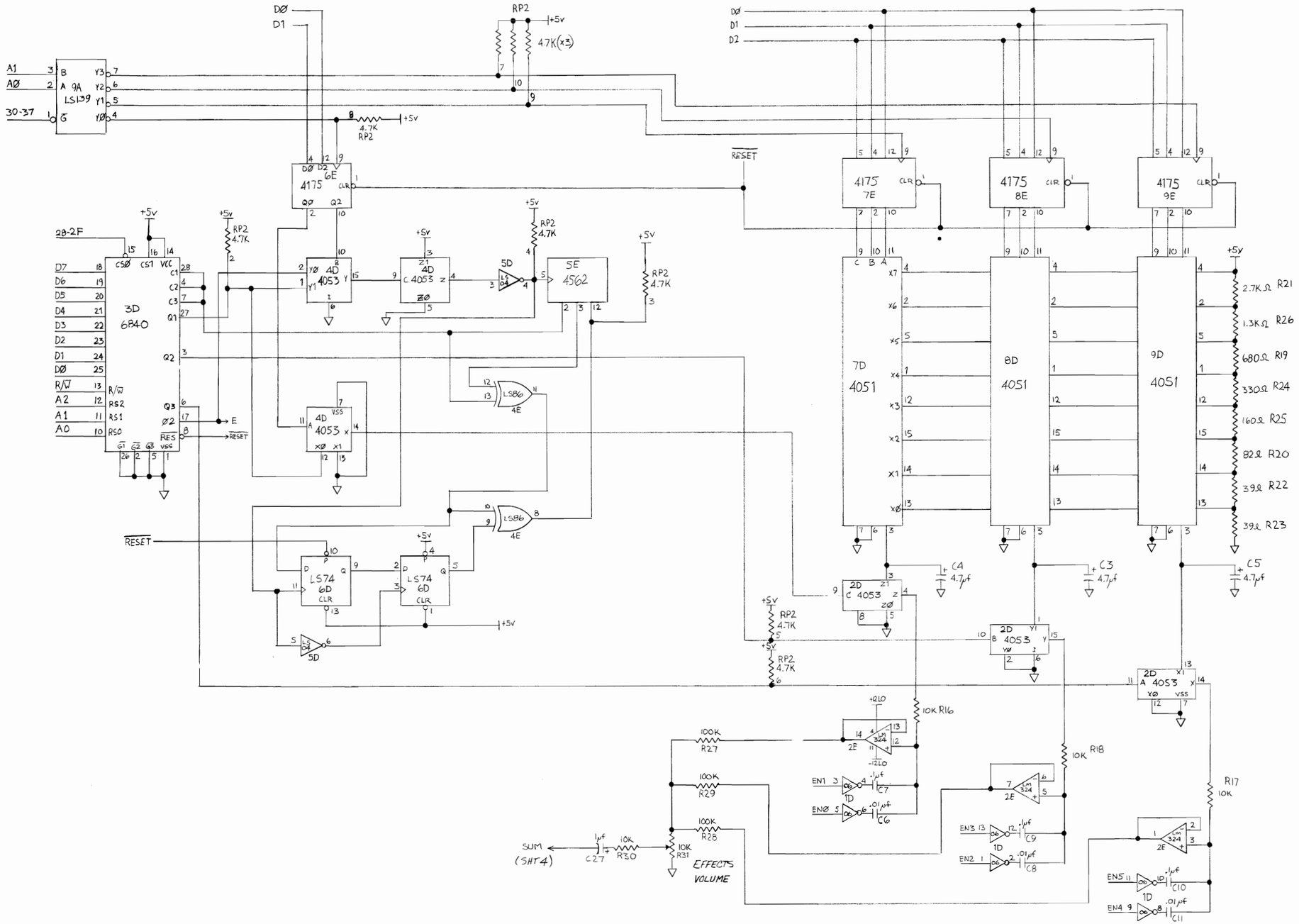






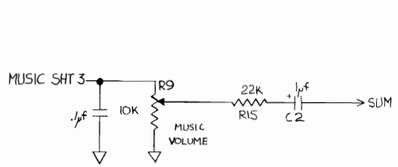
NOTES UNLESS OTHERWISE SPECIFIED: 12

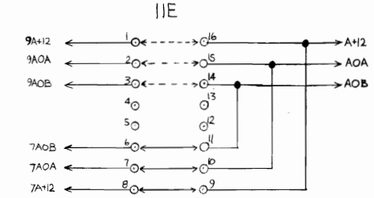
PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING: DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY: NEAL R. ZOOK	DATE: 6-5-81	ENGINEER: MARK VON STRIVER	DATE: 6-6-81	SCALE: DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS: ±	FINISH / DECIMALS: .XX ± .XXX ± / ANGLES: ± °	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	TITLES/DESCRIPTION: AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 2 OF 5	CODE	DRAWING NO.: 77-3387-11	REV.: A
		CHECKED: MARK VON STRIVER	DATE: 6-6-81	PROJECT ENGINEER	DATE										



PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	**DESIGN DRAWING** DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY NEAL R. ZOOK	DATE 6-9-81	ENGINEER MARK VON STRIVER	DATE 6-9-81	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS	FINISH / DECIMALS / ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLES/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 3 OF 5	CODE	DRAWING NO. 77-3387-11	REV. A
		CHECKED MARK VON STRIVER	DATE 6-9-81	PROJECT ENGINEER	DATE														

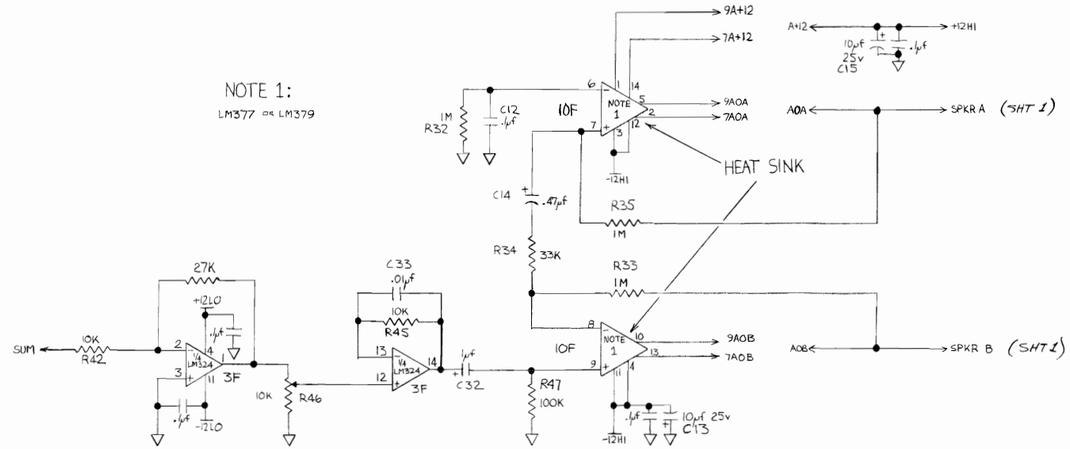
NOTES UNLESS OTHERWISE SPECIFIED:





DIP SHUNT CONFIGURATION
DOTTED LINE FOR LM379
SOLID LINE FOR LM377

NOTE 1:
LM377 OR LM379



PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	**DESIGN DRAWING** DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY NEAL R. ZOOK	DATE 6-9-81	ENGINEER MARK VON STRIVER	DATE 6-9-81	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES / FRACTIONS	FINISH / DECIMALS .xx± .xxx± / ANGLES ± °	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLES/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 4 OF 5	CODE	DRAWING NO. 77-3387-11	REV. A
		CHECKED MARK VON-STRIVER	DATE 6-9-81	PROJECT ENGINEER	DATE														

NOTES UNLESS OTHERWISE SPECIFIED:

J20

14 PIN DIP SOCKET CONNECTOR

FROM LOGIC PCB J4

1	5$RLD
2	CBLB
3	5CSYNC
4	5CVID
5	5$CLK
6	HSYNC
7	GND
8	VSYNC
9	5M02VID
10	5M01VID
11	VA9
12	5LINES
13	VD7A10
14	+5VDC

PATTERN CHARACTER COLOR DIVISION

BLUE DATA LATCH

GREEN DATA LATCH

RED DATA LATCH

ABD0
ABD1
ABD2
ABD3
ABD4
ABD5
ABD6
ABD7
WBLU
WGRN
WRED

L$ 374 11C

COLOR SELECTION

11B 151
12B 151
13B 151

BLU
GRN
RED

VIDEO POLARITY
"VID"
CUT FOR LOW=TRUE
+5V
330 R7

11A L$ 86
BLUA
GRNA
REDA

SYNC POLARITY
"SYNC"
CUT FOR LOW=TRUE
330 R8

12A L$ 86
5CSYNC
HSYNC
VSYNC
CSYNCA
HSYNCA
VSYNCA

PRIORITY ENCODER

9A L$ 139

10B 148

5M01VID
5M02VID
5LINES
CSPACE3
CSPACE2
CSPACE1
CSPACE0
BACKGND
PRI2
PRI1
PRI0

VD7A10
VA9
5$RLD
5CVID

L$ 74 10A

P21

10 PIN WAFER HEADER

REDA	3	2	RED OUT
GRNA	4	5	GRN OUT
BLUA	6	7	BLU OUT
CSYNCA	11	10	CSYNC OUT
HSYNCA	13	12	HSYNC OUT
VSYNCA	14	15	VSYNC OUT

13A L$ 174

5$CLK

OUTPUT TO TV MONITOR (THRU MAIN HARNESS)

PROPRIETARY	DRAWN BY	DATE	ENGINEER	DATE	SHEET OF	NEXT ASSEMBLY	USED ON
THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	AKH	6-7-81	AKH	6-7-81	5 5		
	CHECKED	DATE	PROJECT ENGINEER	DATE			
	AKH	6-22-81	AKH	6-7-81			

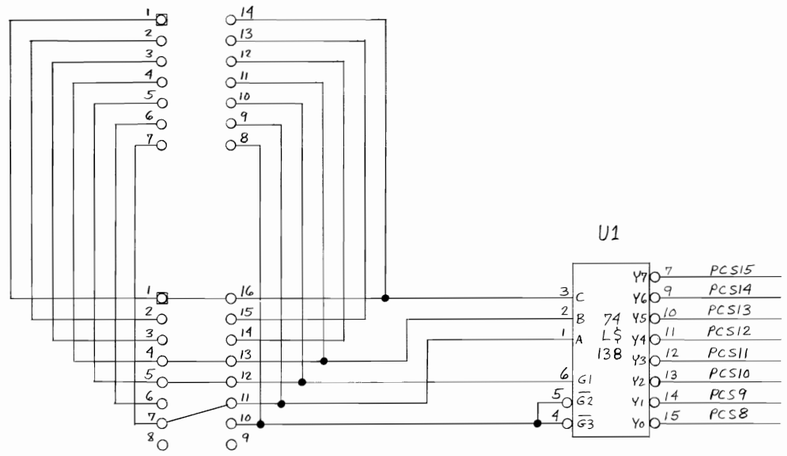
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE	TITLE/DESCRIPTION	SHEET OF	CODE	DRAWING NO.	REV
D	AUDIO/COLOR PCB SCHEMATIC DIAGRAM	5 OF 5		77-3387-11	A

NOTES:
1. For EPROMS +5V (VCC) = PIN 24
   GND = PIN 12
2. 10 EA. BYPASS CAPS NOT SHOWN,
   Between +5VDC and GND. VALUE = .1µf 10V(MIN)
   (Ceramic OK)

J1

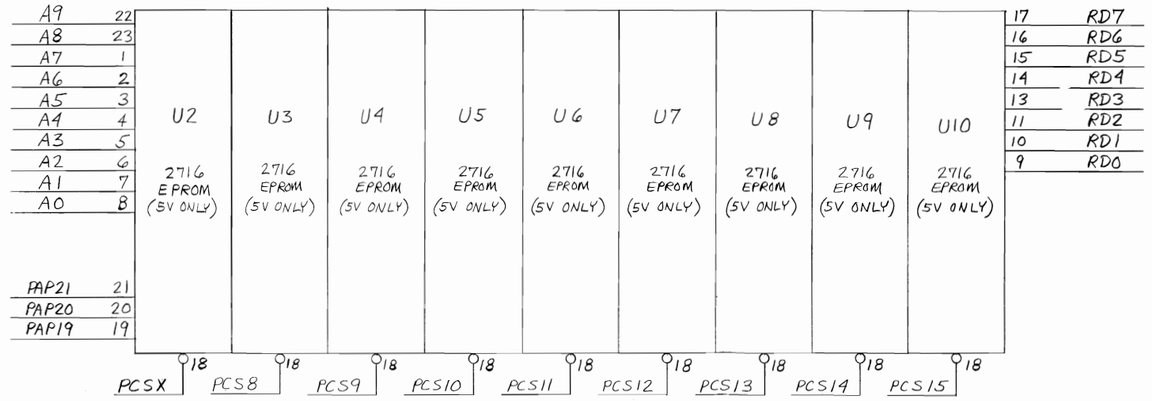
14 PIN DIP SOCKET
(FROM LOGIC PCB POSITION 4B)



JPR1

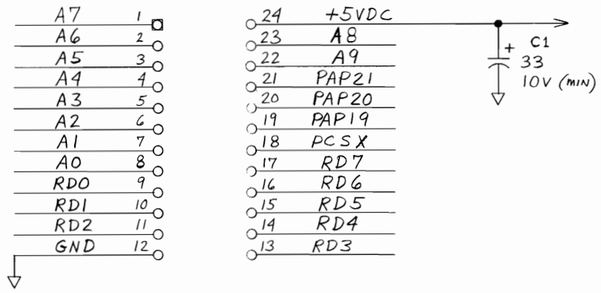
16 PIN DIP PATTERN
w/JPRS included as shown
(May double as 16 PIN input socket)

All lines BUSSED TOGETHER except CHIP SELECTS (PCS0, PCS8–PCS15)



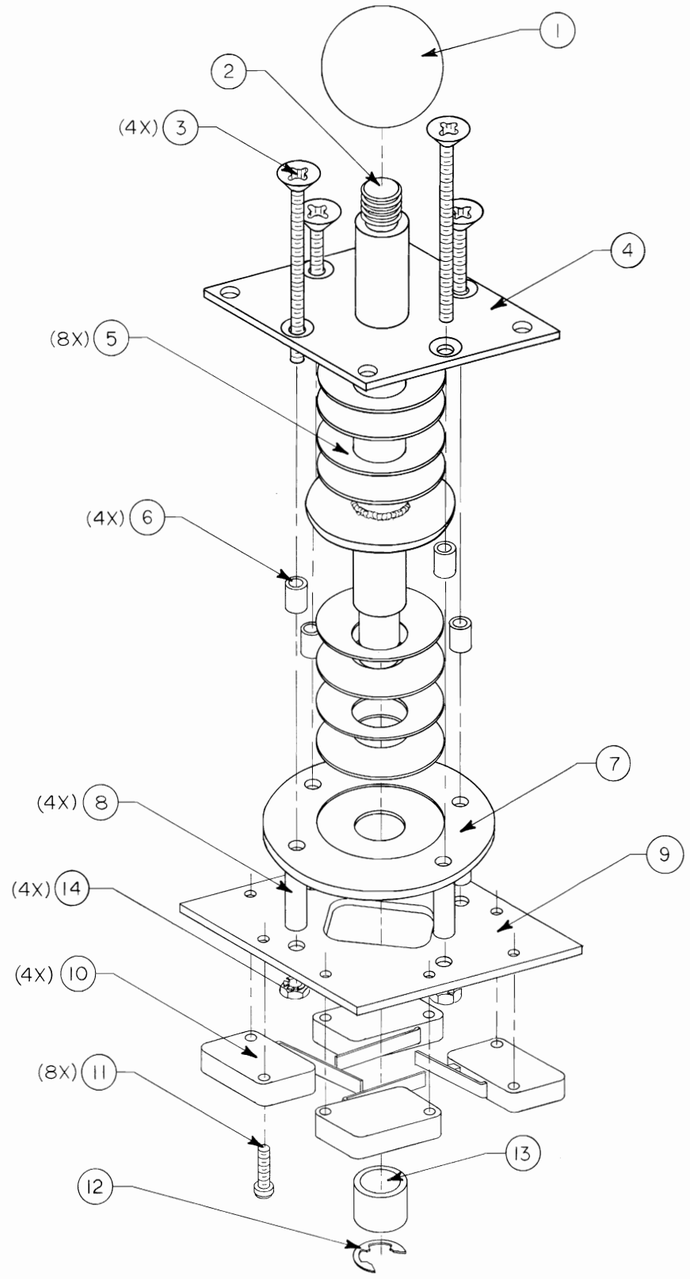
J2

24 PIN DIP SOCKET
(FROM LOGIC PCB POSITION 13A)



14

PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DRAWN BY: AKY	DATE: 6-11-81	ENGINEER: AKY	DATE: 6-11-81	SHEET 1 OF 1	NEXT ASSEMBLY: 77-3374-14 REV E	USED ON: 6502 LOGIC PCB FOR EXPANDED MEMORY	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	TITLE/DESCRIPTION: MEMORY EXPANSION PCB (77-3389-14) SCHEMATIC	CODE	DRAWING NO.: 77-3389-11	REV: A
	CHECKED: AKY	DATE: 6-11-81	PROJECT ENGINEER: AKY	DATE: 6-11-81									



ITEM NO.	QTY	DRAWING NO.	DESCRIPTION
14	4	74-6506	NUT, KEP
13	1	74-5466	BUSHING
12	1	74-5467	RING RETAINING
11	8	74-5189	SCREW, PAN HD.
10	4	72-3063	SWITCH
9	1	68-0127-10	PLATE, SWITCH
8	4	74-5212	SPACER
7	1	68-2031-10	DISC, LOWER
6	4	74-5248	SPACER
5	8	73-9081	WASHER, BELLEVILLE
4	1	68-0030-10	PLATE, UPPER
3	4	74-6525	SCREW, FL.HD.
2	1	97-1022-10	SHAFT
1	1	92-1021-10	KNOB

LIST OF MATERIAL

NOTES UNLESS OTHERWISE SPECIFIED:

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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

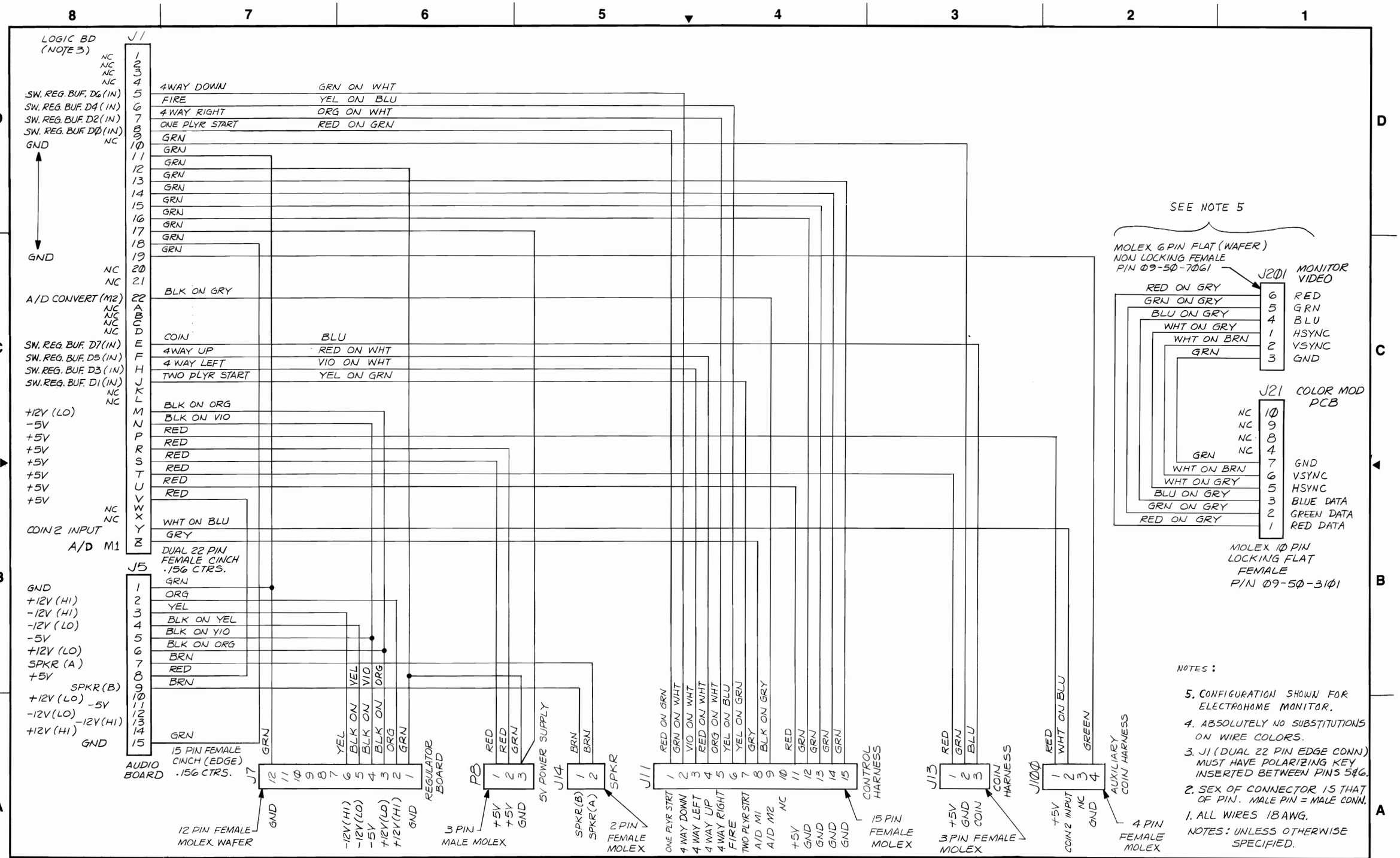
DRAWN BY NP — DATE 4/25/81
CHECKED — DATE
ENGINEER — DATE
PROJECT ENGINEER — DATE
SCALE DO NOT SCALE DRAWING
DATE OF ISSUE
MATERIAL — FINISH
TOLERANCES — FRACTIONS ± — DECIMALS .XX ± .XXX ± — ANGLES ±°

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE D

TITLE/DESCRIPTION: VENTURE TM JOY STICK-8 POSITION

SHEET 1 OF 1 — CODE — DRAWING NO. 38-5119-10 — REV. A



PROPRIETARY
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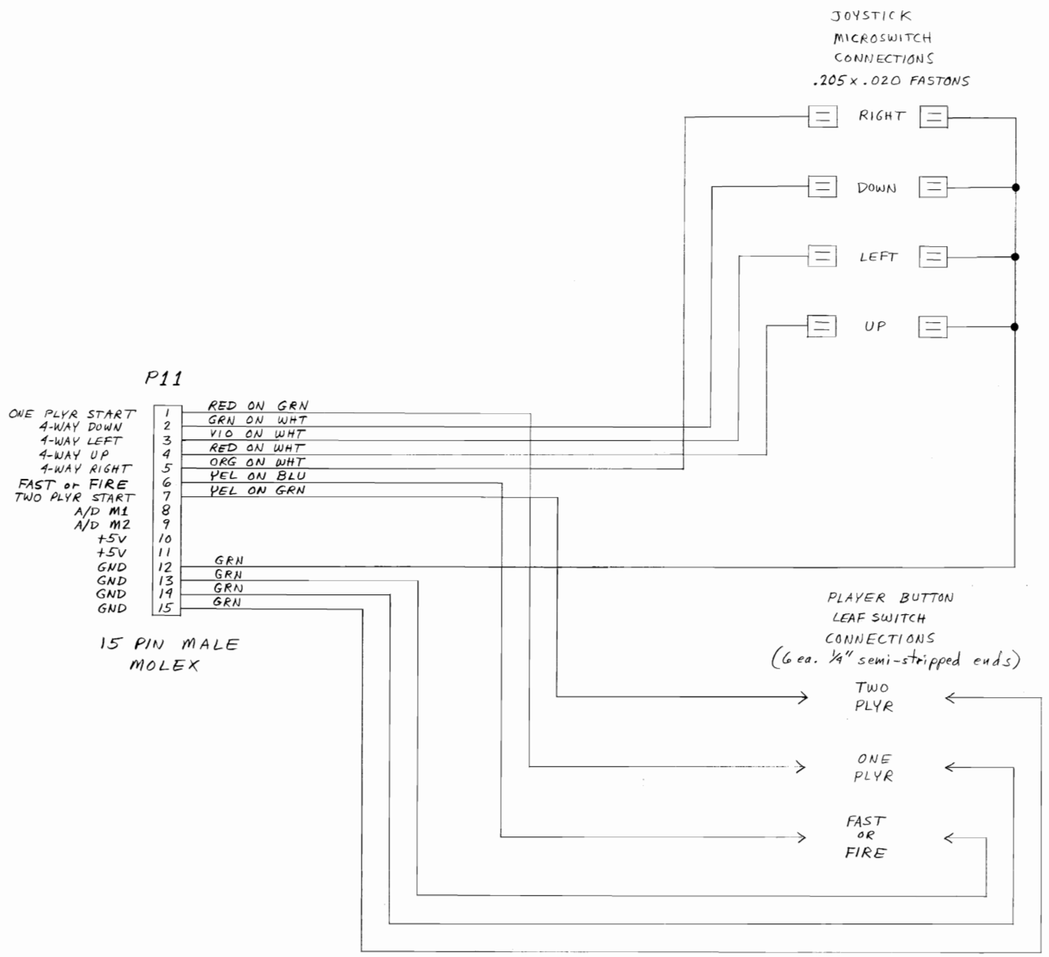
DRAWN BY	DATE	ENGINEER	DATE	SHEET	OF	NEXT ASSEMBLY	USED ON
MA Thompson	6/84			1	1		VENTURE™
CHECKED	DATE	PROJECT ENGINEER	DATE				

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE	TITLE/DESCRIPTION	CODE	DRAWING NO.	REV
D	6502 MAIN HARNESS COLOR	HR	71-2413-11	

CONTROL PANEL HARNESS SCHEMATIC

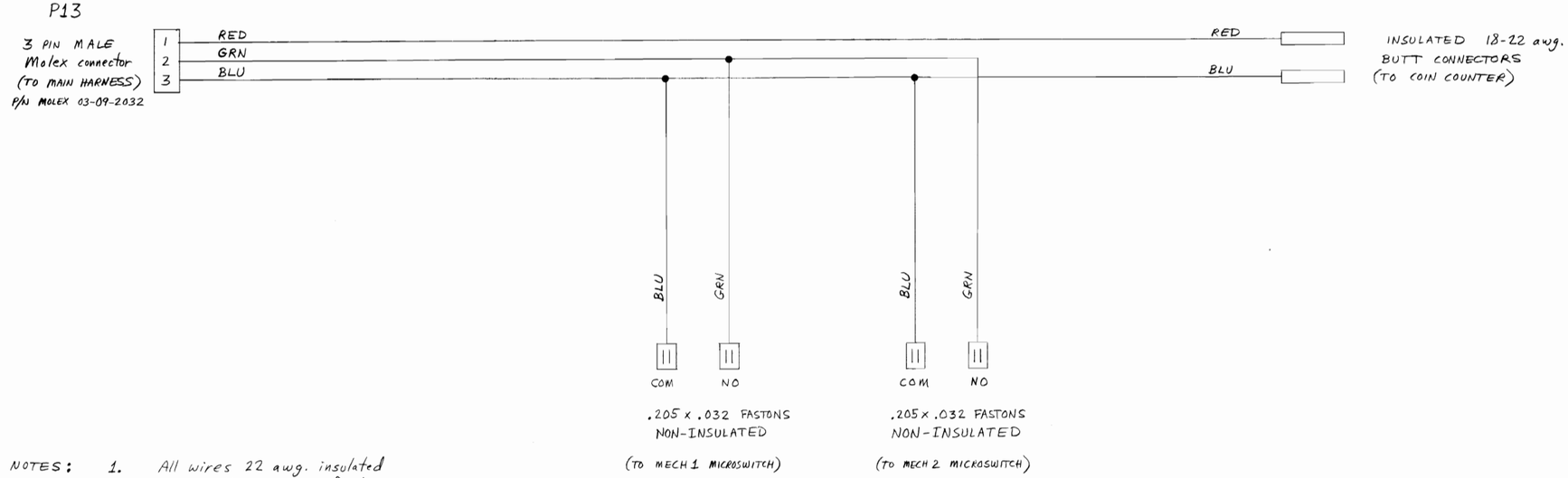


NOTES:
1. All wires 22 awg. insulated unless otherwise specified.
2. ABSOLUTELY NO SUBSTITUTIONS ON SPECIFIED WIRE COLORS

11-6-79

390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE	TITLE/DESCRIPTION	CODE	DRAWING NO.	RF#
	D	CONTROL PANEL HARNESS VENTURE™		30-3188	

COIN HARNESS SCHEMATIC
(UNIVERSAL COIN HARNESS)

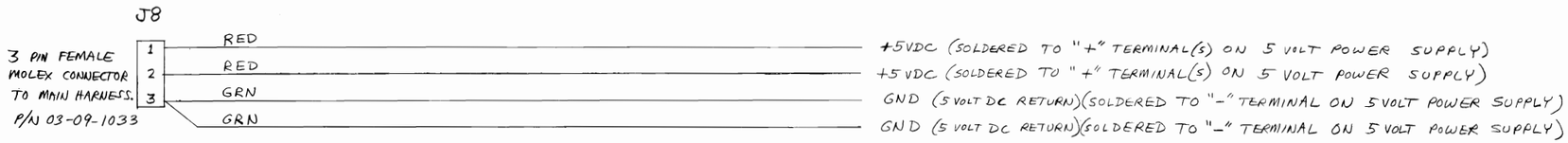


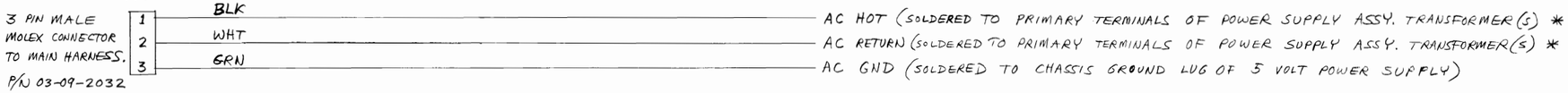
NOTES:

1. All wires 22 awg. insulated unless otherwise specified.
2. ABSOLUTELY NO SUBSTITUTIONS ON SPECIFIED WIRE COLORS

390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLE/DESCRIPTION UNIVERSAL COIN HARNESS VENTURE™	CODE	DRAWING NO. 30-3189	REV

UNIVERSAL POWER SUPPLY ASSEMBLY
HARNESS SCHEMATIC



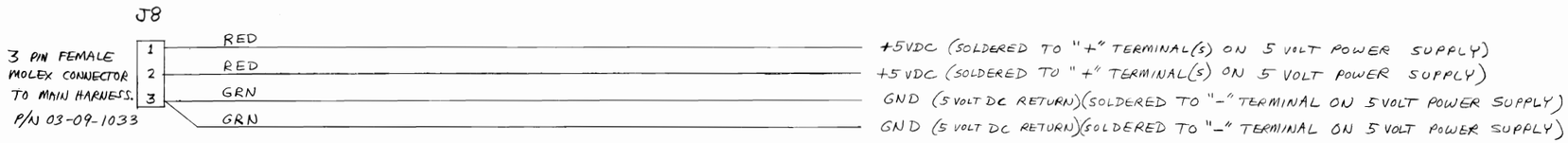


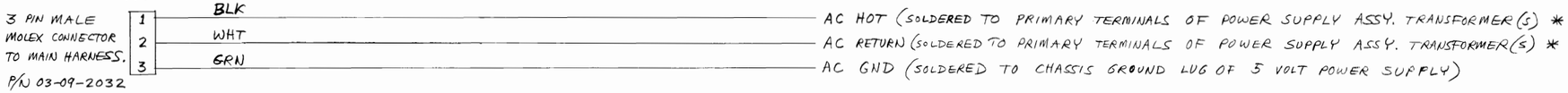
* Which transformer leads or terminals used varies with manufacturer and input AC voltage requirements

NOTES:
1. All wires 18 awg insulated unless otherwise specified
2. ABSOLUTELY NO SUBSTITUTIONS on specified wire colors

390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLE/DESCRIPTION UNIVERSAL POWER SUPPLY ASSEMBLY HARNESS VENTURE™	CODE	DRAWING NO. 30-3190	REV

UNIVERSAL POWER SUPPLY ASSEMBLY
HARNESS SCHEMATIC





* Which transformer leads or terminals used varies with manufacturer and input AC voltage requirements

NOTES:
1. All wires 18 awg insulated unless otherwise specified
2. ABSOLUTELY NO SUBSTITUTIONS on specified wire colors

390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLE/DESCRIPTION UNIVERSAL POWER SUPPLY ASSEMBLY HARNESS VENTURE™	CODE	DRAWING NO. 30-3190	REV

PROPRIETARY
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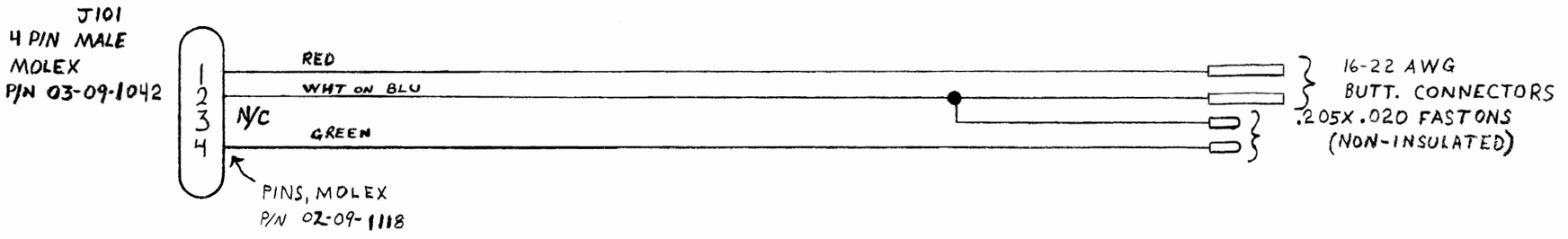
DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST



J101
1. RED
2. WHT ON BLU
3. N/C
4. GREEN

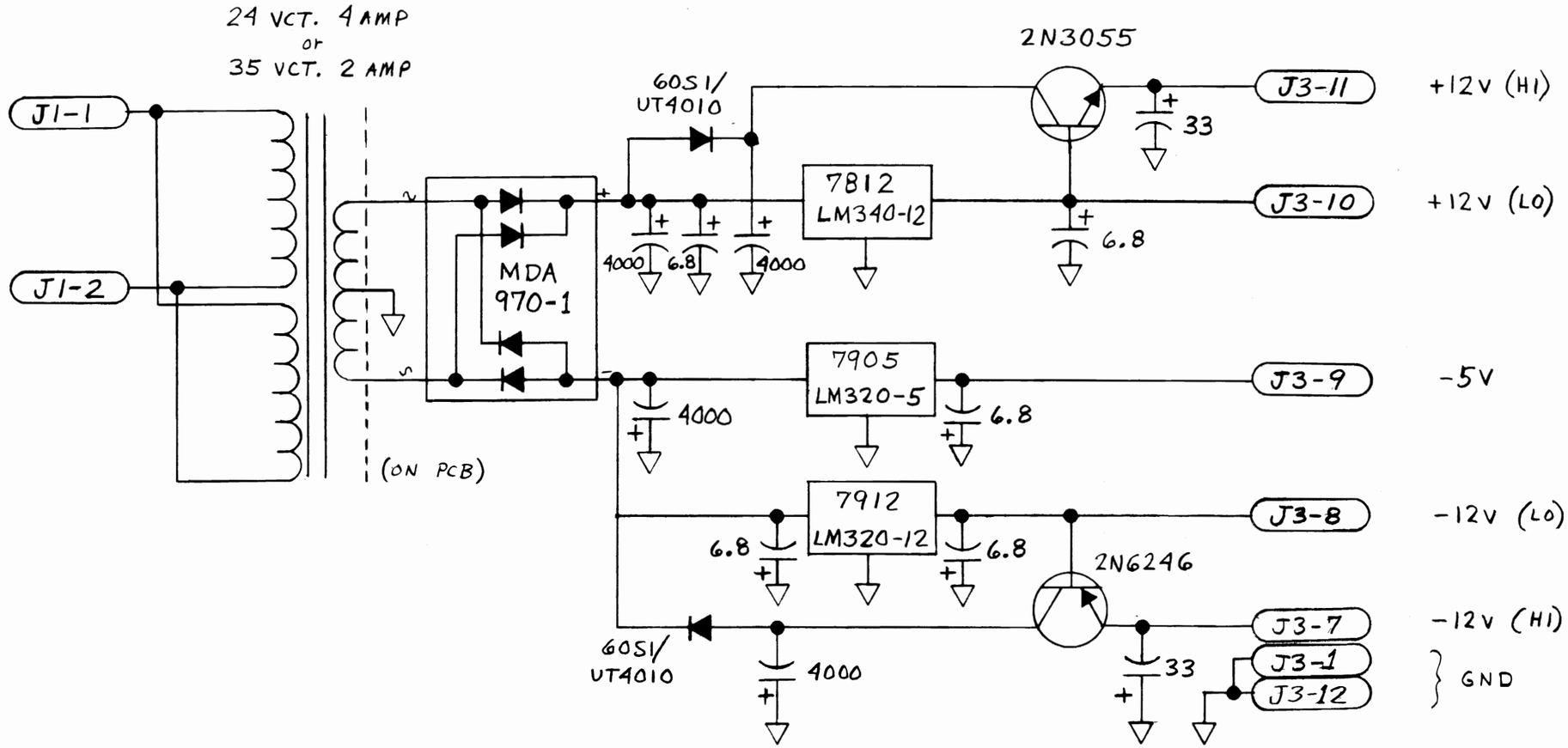
NOTES:
1. NO CHANGES IN SPECIFIED WIRE COLORS.
2. ALL WIRES 22 AWG.
3. EQUIVALENT PINS AND HOUSING MAYBE USED.

NOTES UNLESS OTHERWISE SPECIFIED:

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

TOLERANCES	MATERIAL SEE NOTE	DRAWN	RAW	DATES 5-5-80	SIZE B	TITLE/DESCRIPTION VENTURE™ AUXILIARY COIN DOOR HARNESS SCHEMATIC	SHEET OF
FRACTIONS ± N/A	FINISH N/A	CHECKED	RAW	5-5-80			
DECIMALS .xx± N/A .xxx± N/A	SCALE N/A	ENGINEER	RAW	5-5-80	CODE HR	DRAWING NO. 71-2417-11	REV A
ANGLES ± N/A°	DO NOT SCALE DRAWING	PROJECT ENGINEER	RAW	5-5-80			

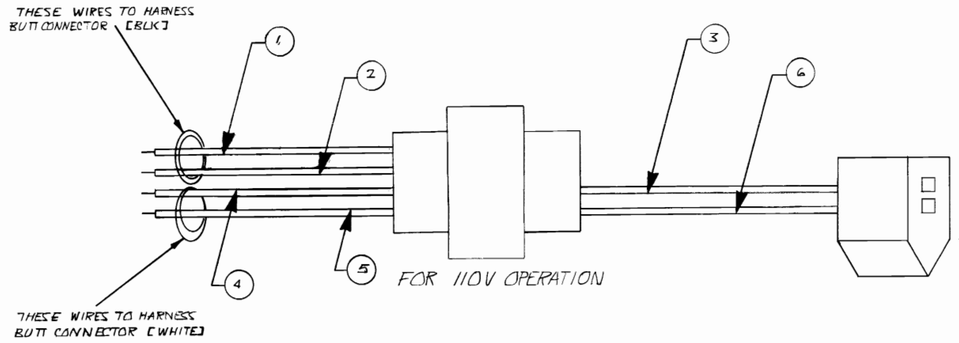
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



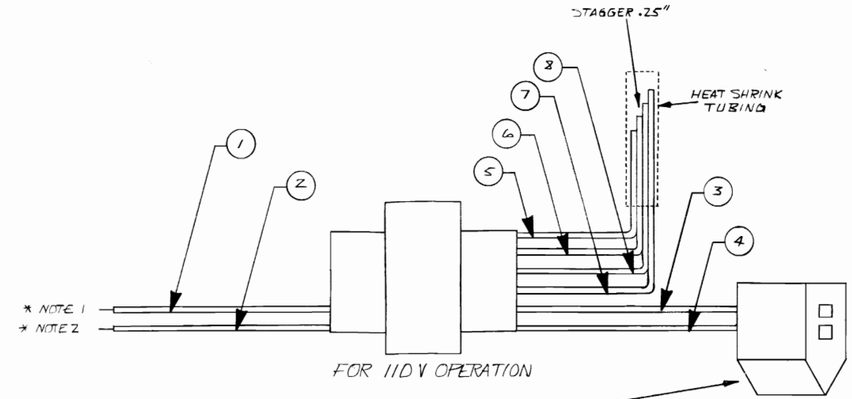
NOTES: 1. All capacitance values shown in microfarads (μf).

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±	CONTRACT NO.	SCHEMATIC
			APPROVALS / DATE	
			DRAWN OMK 26/11/78	UNIVERSAL POWER SUPPLY VENTURE™
		MATERIAL	CHECKED	
		FINISH		SIZE B / CODE IDENT NO. / DRAWING NO. 77-3365-11
NEXT ASSY	USED ON			SCALE / SHEET 1 OF 1
APPLICATION		DO NOT SCALE DRAWING		

BISHOP GRAPHICS, INC. REORDER NO. 20503

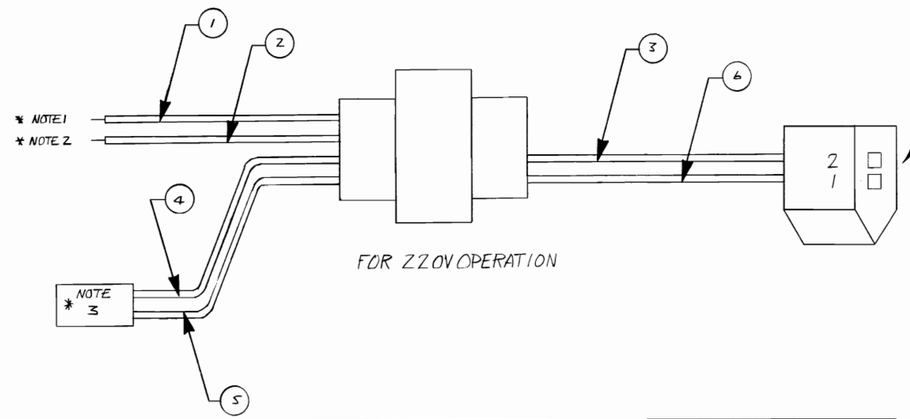


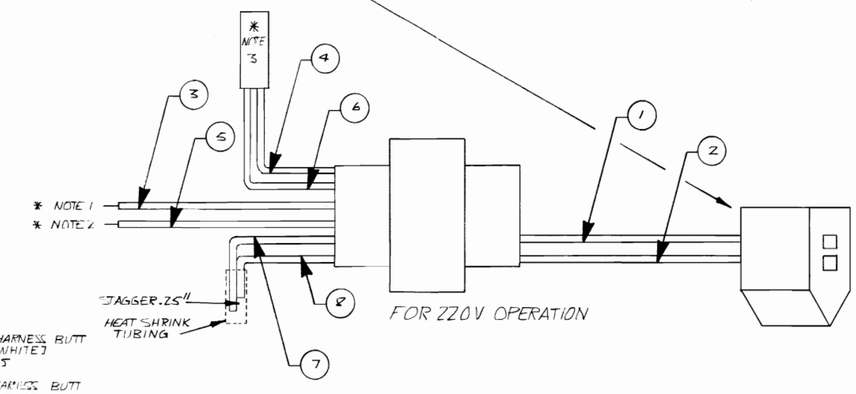
MIDWEST 773P7
EXIDY P/N 63-4029



MOTOROLA 25D25 Z39B20
EXIDY P/N 63-4033

2 PIN MOLEX CONNECTOR
P/N 03-09-1023
EXIDY P/N 61-8057
PINS ARE MOLEX 02-09-1118
EXIDY 61-8055





* NOTE 1:
WIRES GO TO HARNESS BUTT CONNECTOR [WHITE]
STRIP .25"

* NOTE 2:
WIRES GO TO HARNESS BUTT CONNECTOR [BLK]
STRIP .25"

* NOTE 3:
BUTT SPLICE CONNECTOR
THERE IS A CONNECTION AT THESE POINTS

110 VOLTS		
WIRE NUMBER	COLOR	GUAGE
1	RED/YEL	18 GA.
2	RED	
3	YEL	
4	BLK	
5	BLK/YEL	
6	YEL	18 GA.

220 VOLTS		
WIRE NUMBER	COLOR	GUAGE
1	RED	18 GA.
2	BLK/YEL	
3	YEL	
4	RED/YEL	
5	BLK	
6	YEL	18 GA.

110 VOLTS		
WIRE NUMBER	COLOR	GUAGE
1	GRY	18GA.
2	GRY/RED	
3	YEL	
4	BLK/YEL	
5	RED	
6	RED/GRN	
7	GRN	
8	WHT/BLK	18 GA.

220 VOLTS		
WIRE NUMBER	COLOR	GUAGE
1	GRY	18 GA.
2	GRY/RED	
3	YEL	
4	YEL/BLK	
5	RED	
6	RED/GRN	
7	GRN	
8	WHT/BLK	18 GA.

PROPRIETARY
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DRAWN BY	DATE	ENGINEER	DATE	SHEET	OF	NEXT ASSEMBLY	USED ON	SIZE	TITLE/DESCRIPTION	CODE	DRAWING NO.	REV
RICK/MARK	4-17-80			1	1		VENTURE™	D	MONITOR ISOLATION TRANSFORMER ASS'Y.		96-0134-15	A0
CHECKED: RICK	DATE	PROJECT ENGINEER	DATE									

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

EXIDY VENTURE™

APPENDIX A: PARTS LIST

VENTURE(TM) FINAL ASSEMBLY

Part Number	Description
38-5118-10	cabinet assy
38-5122-10	control panel assy
79-2311-10	19" monitor
38-5059	power supply assy
96-0134	monitor isolation xfmr assy
38-5057-10	American Standard dbl coin door assy (w/penny stop)
or	
38-5057-20	British/Australian coin door assy
or	
38-5057-30	French coin door assy
or	
38-5057-40	German coin door assy
or	
38-5057-50	Spanish coin door assy
38-5034	power cord assy
38-5061-10	speaker assy
67-5000	lock and key assy
71-2413	main harness assy
71-2330	cable, PCB ribbon
38-5117-10	fluorescent light assy
77-3377-15	logic board PCB assy
77-3387-15	audio color board PCB assy
75-5183-10	pressure sensitive side art right
75-5184-10	pressure sensitive side art left
72-3000	interlock switch
68-7010	interlock bracket
88-4026	locktite
92-1021-10	8-way joystick knob (black)
68-0035	6 x 9 speaker grill
68-6050-10	universal coin box
68-6050-20	universal coin box lid
68-0126-10	coin box hasp
68-0124	logo plex mounting bracket
68-0125	monitor stop brkt
89-1008	label, serial no. aluminum-black letters
83-0009	3 amp fuse label
87-9003	packing list envelope
75-5185	ambient solar-control plastic shield
75-5186	display plastic panel, silkscreened
75-5187-10	logo plastic panel, silkscreened
89-1009-10	FCC warning label (small)
89-1010-10	FCC warning label (large)
71-3388-10	isolation xfmr extension harness
74-5165-10	washer 3/16 i.d.x. 1 1/4 o.d. fender
74-6513-10	10-32 kep nut
74-4710	#8x 1/2 pan hd. phil wood screw
74-5246	10-24 x 1 1/2 hex full thread bolt

FINAL ASSEMBLY, continued

74-6402	#10 American plain washer
74-6506	10-24 kep nut
74-4603	#8 x 3/4 pan hd. phil wood screw
74-8532-10	10-32 x 1" pan hd. allen drive mach screw black
74-6524-10	10-24 x 1 1/2 carriage bolt black
74-8533-10	1/4 20 x 3/4 full thread hex bolt
74-5163-10	1/4 i.d. x 5/8 o.d. amer plain washer
88-4002	small tie wrap
88-4001	large tie wrap
74-5464	#8 x 1/2 pan hd. square drive blk ox wood screw

CONTROL PANEL ASSEMBLY

Part Number	Description
68-0123	control panel fab
38-5119-10	8-way joystick assy
38-5044	wico pushbutton assy
72-3022	switch, pushbutton w/ nut and washer
75-5188	control panel polycarb overlay, silkscreened
74-5247	10-24 x 5/8 carriage bolt black
74-6506	10-24 kep nut
71-2391	control panel harness

PUSH BUTTON ASSEMBLY

Part Number	Description
72-3061	Switch assy, Wico
72-3062	push button
74-0203	pal nut

MONITOR ISOLATION TRANSFORMER ASSY

Part Number	Description	Reference
FR 63-4029	isolation transformer midwest 773P7	
61-8058	molex connector 03-09-2032	AC input P22
61-8054	male molex pins 02-09-2118	P22
61-8057	molex connector 03-09-1023	AC monitor J23
61-8055	female molex pins 02-09-1118	J23
76-1212-50	transformer mounting board	
71-2001-14	transformer harness	
61-8072	butt splice blue	
74-6402	washer, #10 plain	
74-6506	kepnut 10-24	
74-5463-01	screw, 10-24 x 1" ph phil. mach	
74-5165	fender washer 1/4 id 1 1/4 od	
88-4002	tie wrap small	
61-8313	butt splice red	

AMERICAN STANDARD DOUBLE COIN DOOR

Part Number	Description
66-4003	std double coindoor, Vendall w/penny stop
66-4007	25 cent American coin door acceptor
supp w/ item	coin door key
71-2390	universal coin door harness
64-2000	coin meter
88-4002	tie wrap, small
61-8313	butt splice, red
74-3502	6-32 kepnut

6502 GAME LOGIC PCB ASSEMBLY

Part Number	Description	Reference Location
48-2000	IC 7400	3D, 15H
48-2005	IC 7402	1H, 6H
48-2010	IC 7404	1D, 3F, 4D, 10F, 11F
48-2015	IC 7407	2C
48-2020	IC 7408	5E
48-2332	IC 74LS11	3H
48-2035	IC 7420	2F
48-2316	IC 74LS21	12F, 15E
48-2045	IC 7427	7F, 2H
48-2055	IC 7432	6F
48-2067	IC 7474	1C
48-2071	IC 74LS112	2E, 6E
48-2307	IC 74LS138	5B, 5D
48-2321	IC 74LS139	7E, 16H
48-2090	IC 74157	14A, 14E
48-2095	IC 74161	1E,2D,4F,5F
48-2100	IC 74166	12B, 12D, 13D, 14D, 15D
48-2115	IC 74193	10E, 12E, 13F, 15F 14F, 16F, 11E,13E
48-2328	IC, 74LS241	8C, 1A, 3A 3B, 4H, 6B, 7D, 9B, 9E, 15A

6502 GAME LOGIC PCB ASSEMBLY (continued)

Part Number	Description	Reference Location
48-2350	IC 74LS245	3C, 4C, 6C 15B, 13B
48-2314	IC 74LS374	1F, 14B, 7C, 8E
48-6502	microprocessor 6502	2A
48-2334	2114 (1K x4) RAM	4A, 5A, 7B, 8B, 11C, 12C 13C, 14C
48-9220	2176 (VEL 11D-1)	11D
48-9099-01	6331 PROM (.32 X 8)	6D
48-9099-02	6331 PROM (.32 X 8)	14H
48-9219	6301 PROM (256 X 4) VEL5C-1	5C
46-3025	IN4002 diodes	8E, 9E, 2H
59-5135	res. 470 omega 1/4 w 5%	1D, 2H
59-5120	res., 1.2K 1/4w 5%	2C
59-5115	res., 1.8K 1/4w 5%	1C, 2C
59-5110	res., 2.2K 1/4w 5%	7E, 2A
59-5105	res., 2.7K 1/4W 5%	1C, 2C
51-0003	res., 220 omega 1/4w 5% 10 pin sip	9E
51-0002	res., 2.2K 1/4w 5% 10 pin sip	16A
51-0001	res., 4.7K 1/4w 5% 10 pin sip	15A
51-0004	res., 6.8K 1/4w 5% 10 pin sip	14A
23-4033	cap, .01 uf ceramic disc	1D
23-4035	cap, .1 uf ceramic disc	A/R per assy drawing
21-4015	cap, 6.8 uf 25v tant. dip	1C, 6E, 15D, 13F
20-4014	cap, 33 uf 25v electrolytic	IC 2C
20-4005	cap, 470 uf 10v electrolytic	10H
72-3025	dip shunt jumper paks 16 pin	4B, 10D, 11B
72-3042	dip switch 8 pos.	16A
45-3036	crystal, 11.289	1D
61-8041	connector 10 pin molex	16C, 16E
61-8062	dip sockets 16 pin low profile	5C, 6D, 14H
77-3374	print. circuit board	
61-8045	dip socket 24 pin low profile	11D,6A,7A,8A 9A, 10A, 11A
61-8035	dip socket 40 pin low profile	2A
61-8060	dip socket 14 pin low profile	16B
61-8157	dip socket 18 pin low profile	4A 5A 7B 8B 11C 12C 13C 14C

6502 Game Logic PCB Assembly (continued)

Part Number	Description	Reference Location
21-4021	cap, 1 uf 25V dip tant	C45, C52
59-5138	res, 220 v 1/4 w 5%	R200, R311 at 5D
59-5179	res, 18ohm 1/4w 5%	R300-R308
23-4067	cap, 330 pf cer. disk	5D
48-2300	74LS00 I.C.	15C
48-2301	74LS02 I.C.	8F

See addendum for part numbers of 2716 eprom programmed.

AUDIO-COLOR PCB ASSEMBLY

Part Number	Description
48-2307	74LS138
48-6520	6520
48-9209	6532
48-6502	6502
48-9210	6840
48-9211	74LS154
48-9212	8253
48-9213	4069
48-9069	4013
48-2302	74LS04
48-2300	74LS00
48-2314	74LS374
48-9214	4053
48-9215	4175
48-9216	4562
48-2305	74LS74
48-2342	LM324
48-2013	7406
48-2341	74LS86
48-9217	4051
48-2321	74LS139
48-9112	LM377
48-2072	74148
47-2080	74151
48-2333	74LS174
23-4034	cap .1 uf cer 16v
20-4014	cap 33 uf 25v Electrolytic
20-4006	cap 100 uf 16v Electrolytic
59-5115	res 1.8K 1/4w 5%
59-5100	res 3.3K 1/4w 5%
59-5125	res 1K 1/4w 5%
45-3048	3.579545 mHz (series)
59-5016	res. 10 m 1/4w 5%
23-4070	cap 22 pf cer 16v
59-5182	res 300K 1/4w 5%
59-5045	res 100 K 1/4w 5%

AUDIO-COLOR PCB ASSEMBLY (continued)

Part Number	Description
52-0009	res 4.7K sip (10 pin)
61-8062	16 pin dip socket
72-3025	16 pin dip shunt
61-8045	socket 24 pin dip
61-8103	socket 28 pin dip
23-4033	cap .01 uf cer 16v
59-5070	res 22K 1/4 w 5%
59-5063	res 27K 1/4w 5%
59-5025	res 1m 1/4w 5%
59-5065	res 33K 1/4 5%
22-4032	cap 10 uf 25v dip tant
59-5105	res 2.7K 1/4w 5%
59-5119	res 1.3K 1/4w 5%
59-5130	res 680 omega 1/4w 5%
59-5136	res 330 omega 1/4w 5%
59-5184	res 160 omega 1/4w 5%
59-5185	res 82 omega 1/4w 5%
59-5080	res 10K 1/4w 5%
54-5019	10K pot
20-4009	cap 4.7 uf 16v Electrolytic
20-4022	cap. 1 uf 16v Electrolytic
61-8035	40 pin dip socket
74-5065	standoff 6-32 x 5/8" nylon

UNIVERSAL POWER SUPPLY ASSEMBLY

Part Number	Description
78-3001	+5 vdc power supply 6 amp
63-4028	aux. transformer T911 or 63-4035 Mfg. pin 773 pg.
OR	
63-4025	aux. transformer T893
77-3365-15	power supply pcb assy
71-2389-10	power supply harness
76-1211-10	power supply mounting board
74-3503	screw, #6 x 1/2 l phillips pan head self tap
74-5198	screw, #6-32 x 3/4 pan hd phil machine
74-3502	kepnut 6-32
74-3500	washer #6 amer std plain
74-4604	hex nut 8-32 nylon
61-8072	butt splice blue
61-8056	plug, 2 pin molex
61-8054	pins, male molex
88-4002	tie wrap, small
88-4001	tie wrap, large
88-4028	wire, 22 ga. buss-uncoarted
88-4008	solder SN60.03 dia 58 core
88-4011	flex mask and mold seal

AC LINE CORD HARNESS ASSEMBLY

Part Number	Description	Reference
71-2070	AC line cord	PL1
60-6020	fuse holder	F1
60-6001	fuse 3 amp slow bin	F1
61-8039	3 pin molex recept	J1
61-8055	individual femal pins	J1
88-4002	small tie wrap	
61-8051-01	fast on push on terminals .1875	E1
61-8051-02	fast on push on terminals .1875	E2
61-8072	TFB butt splice	E3
88-4012	shrink tubing 3/8	

VENTURE (TM) SPEAKER ASSY

Part Number	Description	Reference
62-7061	6" X 9" oval speaker	cab. interior
61-8056	conn. 2 pin male molex 03-09-2002	P4
61-8054	pins, male molex 02-09-2118	

ISOLATION TRANSFORMER HARNESS

Part Number	Description
61-8058	molex 3 pin plug
61-8039	molex 3 pin recept
61-8054	molex pin (male)
61-8055	molex pin (female)
88-4022	panduit tie wrap 4 in.
61-8313	butt splice (red) black wire 18-22 ga. white wire 18-22 ga. green wire 18-22 ga.

UNIVERSAL COIN DOOR HARNESS

Part Number	Description
61-8058	molex 3 pin plug 03-09-2032
61-8312	panduit terminal D18-188
61-8054	molex pin (male)
61-8313	butt splice (red)
88-4002	panduit tie wrap
N/A	red wire 18-22 ga.
N/A	green wire 18-22 ga.
N/A	blue wire 18-22 ga.

POWER SUPPLY HARNESS

Part Number	Description
61-8058	molex 3 pin plug
61-8039	molex 3 pin recept
61-8054	molex pin (male)
61-8055	molex pin (female)
88-4022	panduit tie wrap 4 in.
	black wire 18 ga.
	white wire 18 ga.
	green wire 18 ga.

CONTROL PANEL HARNESS

Part Number	Description
61-8095	molex 15 pin plug
61-8312	panduit terminal D18-188
	violet on white wire 18-22 ga.
	green on white wire 18-22 ga.
	red on green wire 18-22 ga.
	green on blue wire 18-22 ga.
	orange on white wire 18-22 ga.
	red on white wire 18-22 ga.
	yellow on green wire 18-22 ga.
	green wire 18 ga.
88-4002	panduit tie wrap
61-8054	molex pin (male)
61-8312	.205 x .02 fast-ons

MAIN HARNESS

Part Number	Description	Reference
61-8043	molex 6 pin flat wafer conn.	
61-8089	molex 4 pin plug	
61-8039	molex 3 pin receptacle	61-8039
61-8207	molex 15 pin receptacle	
61-8113	molex 10 pin flat conn.	09-50-3101
61-8057	molex 2 pin receptacle	
61-8058	molex 3 pin plug	
61-8208	molex 12 pin flat wafer conn.	
61-8308	15 pin cinch edge conn.	
61-8309	dual 22 pin cinch edge conn.	
	black wire 18 ga.	
	brown wire 18-22 ga.	
	red wire 18 ga.	
	orange wire 18 ga.	
	yellow wire 18 ga.	
	green wire 18 ga.	
	blue wire 18-22 ga.	
	violet wire 18 ga.	
	grey wire 18-22 ga.	
	white wire 18 ga.	
	blue on black wire 18-22 ga.	
	blue on green wire 18-22 ga.	
	black on yellow wire 18 ga.	
	black on orange wire 18 ga.	
	black on violet wire 18 ga.	
	red on green wire 18-22 ga.	
	yellow on green wire 18-22 ga.	
	black on grey wire 18-22 ga.	
	red on white wire 18-22 ga.	
	green on white wire 18-22 ga.	
	violet on white wire 18-22 ga.	
	orange on white wire 18-22 ga.	
	yellow on blue wire 18-22 ga.	
	white on grey wire 18-22 ga.	
	red on grey wire 18-22 ga.	
	green on grey wire 18-22 ga.	
	white on brown wire 18-22 ga.	
	green on brown wire 18-22 ga.	
61-8311	molex pin 08-50-0116	for wafer conn
61-8310	molex pin 08-03-0304	for Dual 22 conn.
61-8054	molex pin (male) 02-09-2118	
61-8055	molex pin (female) 02-09-1118	
88-4002	panduit tie wrap	
88-4025	panduit tie clamp PLC1-51-58	
88-4005	1/8" shrink tubing	

FLUORESCENT LIGHT ASSEMBLY

Part Number	Description
70-6052	fluor. light fixture
70-6057	fluor. bulb (cool white)
71-2429	fluor. light harness with 50" length
70-6054	fluor. light starter

EIGHT-WAY JOYSTICK ASSEMBLY refer to Figure 2, Joystick Assembly.

Part Number	Description
68-0030-10	upper mntg. plate
92-1002-10	handle w/ bushing
68-2031-10	lower disc
68-2030-10C	switch plate (Case Hardened Steel) 73-9081
73-9081	beleville spring washer
74-5189	screw #4-40 x 5/8 L phil. pan hd
74-6525	screw 10-24 x 2 1/2" L flat hd.
74-5248	#10 x 7/16" L spacer
74-5212	#10 x 1 1/2" L spacer
74-6506	#10 24 kep nut
74-5467	"E" ring .035 thick 7/16" shaft
74-5466	inner ring bushing (case hardened steel) .50 i.d. x .75 x 1/2 L
72-3059	cherry microswitch E23-50H (steel actuator)
or	
72-3060	cherry micro switch E33-50H (steel actuator)
or	
72-3063	Honeywell microswitch V3I-3005-D8
or	
72-3064	"Omron" microswitch V15FL-IC2-K

VENTURE (TM) SPEAKER ASSEMBLY

Part Number	Description	Reference
62-7061	6" X 9" Oval speaker	cab. interior
61-8056	conn. 2 pin male molex 03-09-2002	P4
61-8054	pins, male molex 02-09-2118	

"**Warning:** This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference."