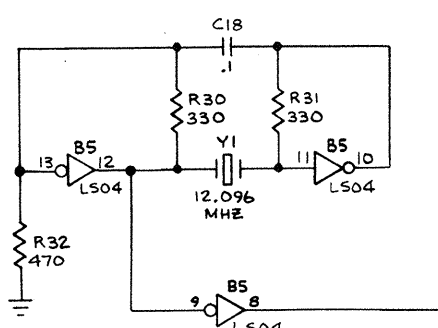


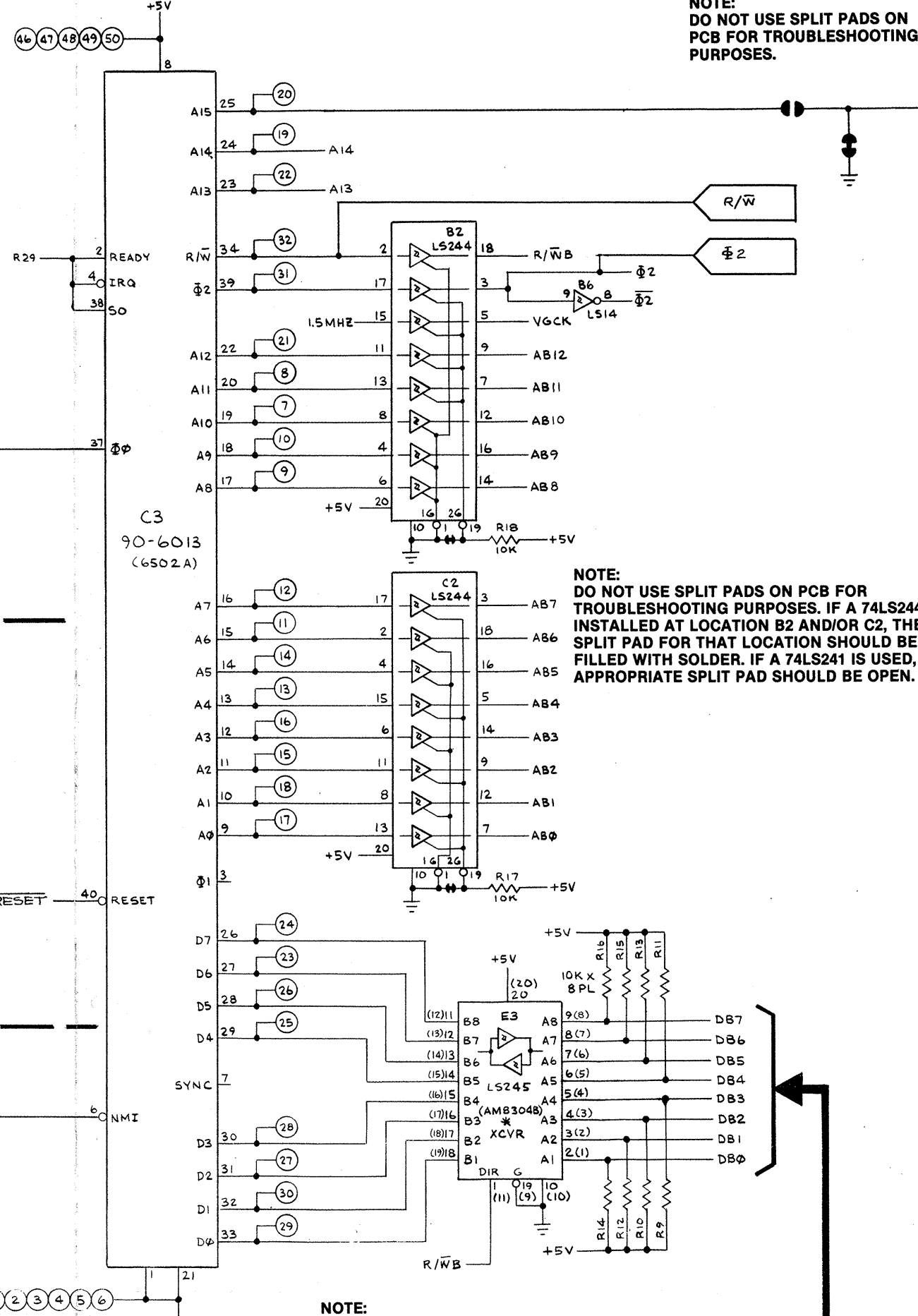
CLOCK CIRCUIT



The clock circuit consists of crystal Y1 and associated inverters and counters C4 and B4. Counters C4 and B4 count the crystal frequency down to the frequencies necessary for the Asteroids game.

NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY OF 1.5 MHz. THEREFORE THE MPU CHIP MUST BE 6502A. THE 6502'S MAXIMUM FREQUENCY IS 1 MHz AND IS NOT COMPATIBLE WITH THIS GAME.

MPU CIRCUITRY

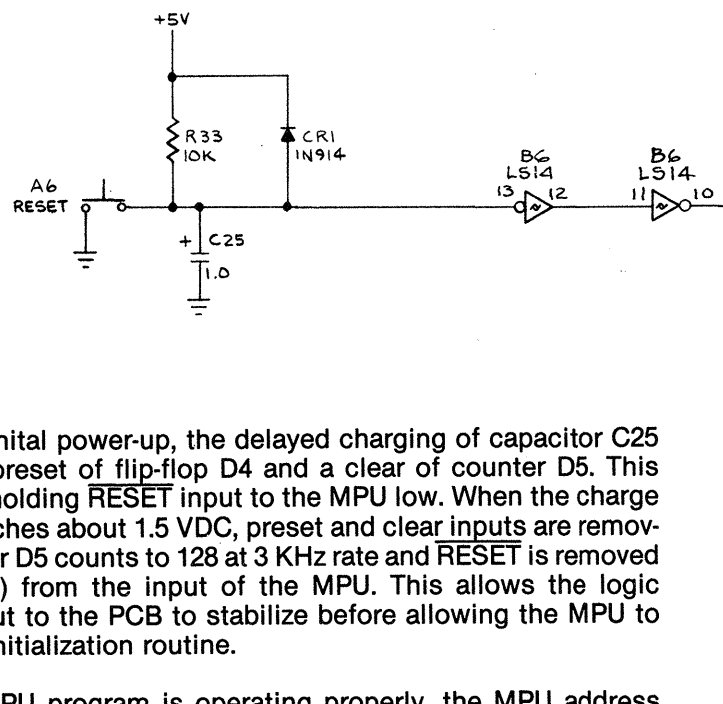


NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES.

NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES. IF A 74LS244 IS INSTALLED AT LOCATION B2 AND/OR C2, THE SPLIT PAD FOR THAT LOCATION SHOULD BE FILLED WITH SOLDER. IF A 74LS241 IS USED, THE APPROPRIATE SPLIT PAD SHOULD BE OPEN.

NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT ENCLOSED IN PARENTHESES ARE FOR 74LS245. PIN NUMBERS IN PARENTHESES ARE FOR AN AM8304B.

POWER RESET AND WATCHDOG COUNTER



During initial power-up, the delayed charging of capacitor C25 results in holding RESET flip-flop D4 and a clear of counter D5. This results in holding RESET to the MPU low. When the charge of C25 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

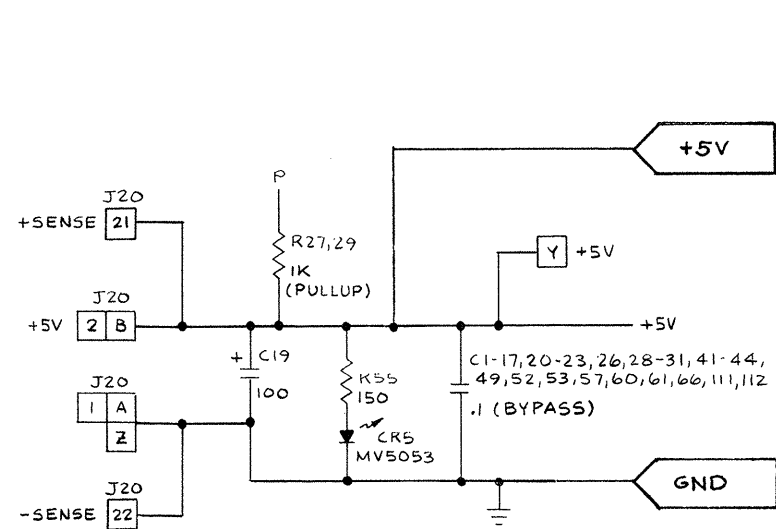
If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D5 will count up to the RESET state and cause the MPU to return to its initialization routine.

■ denotes change by indicated revision
○ denotes a test point

NMI COUNTER

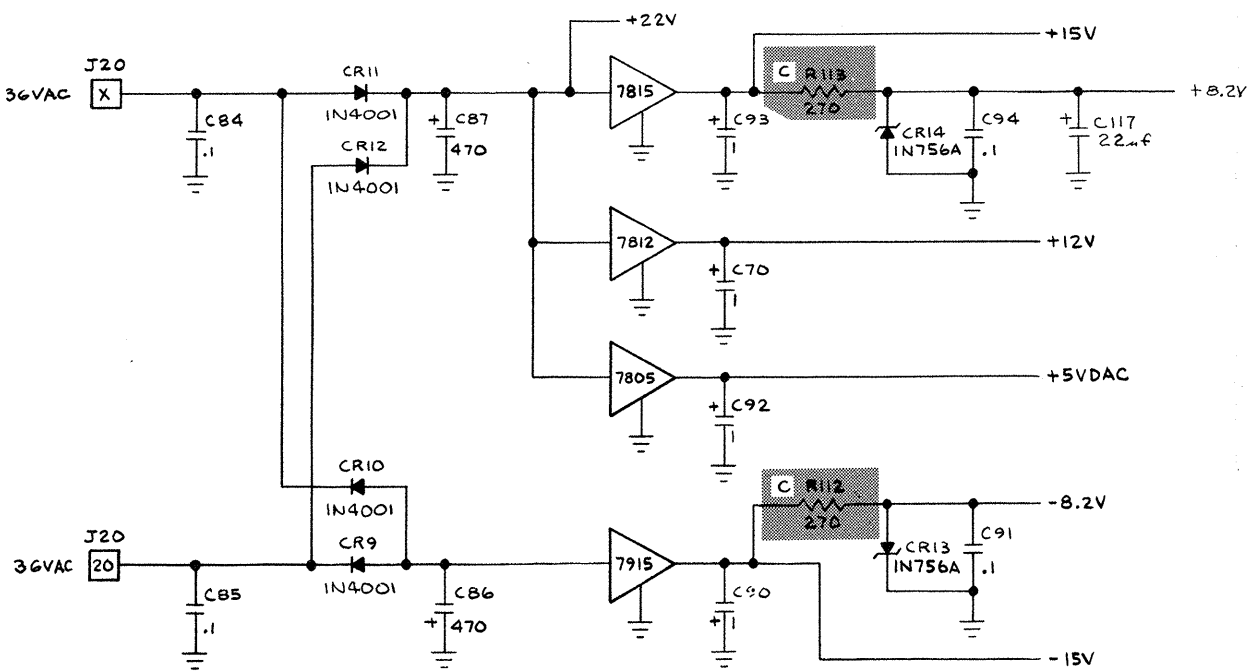
The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

POWER INPUT



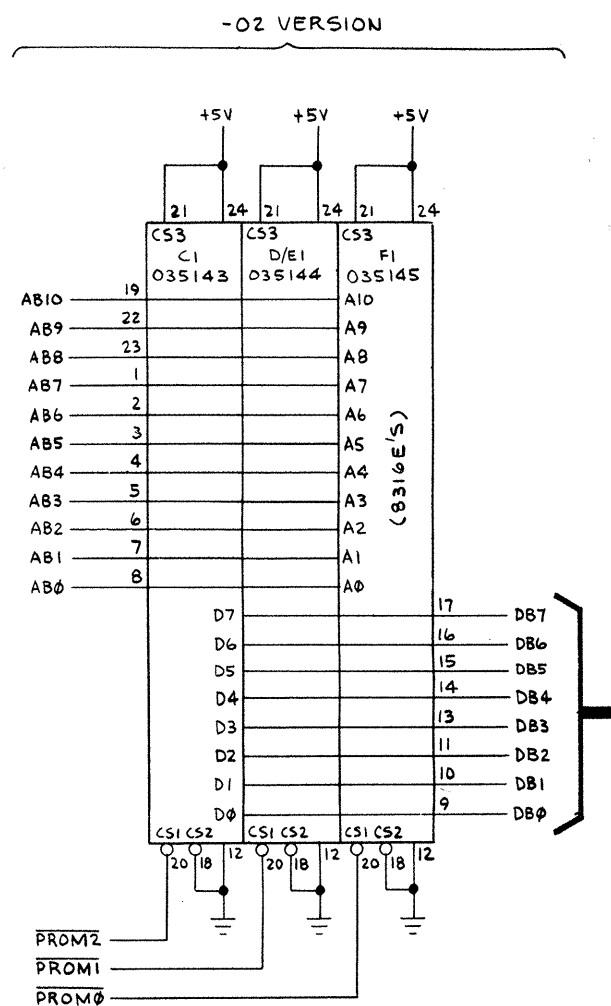
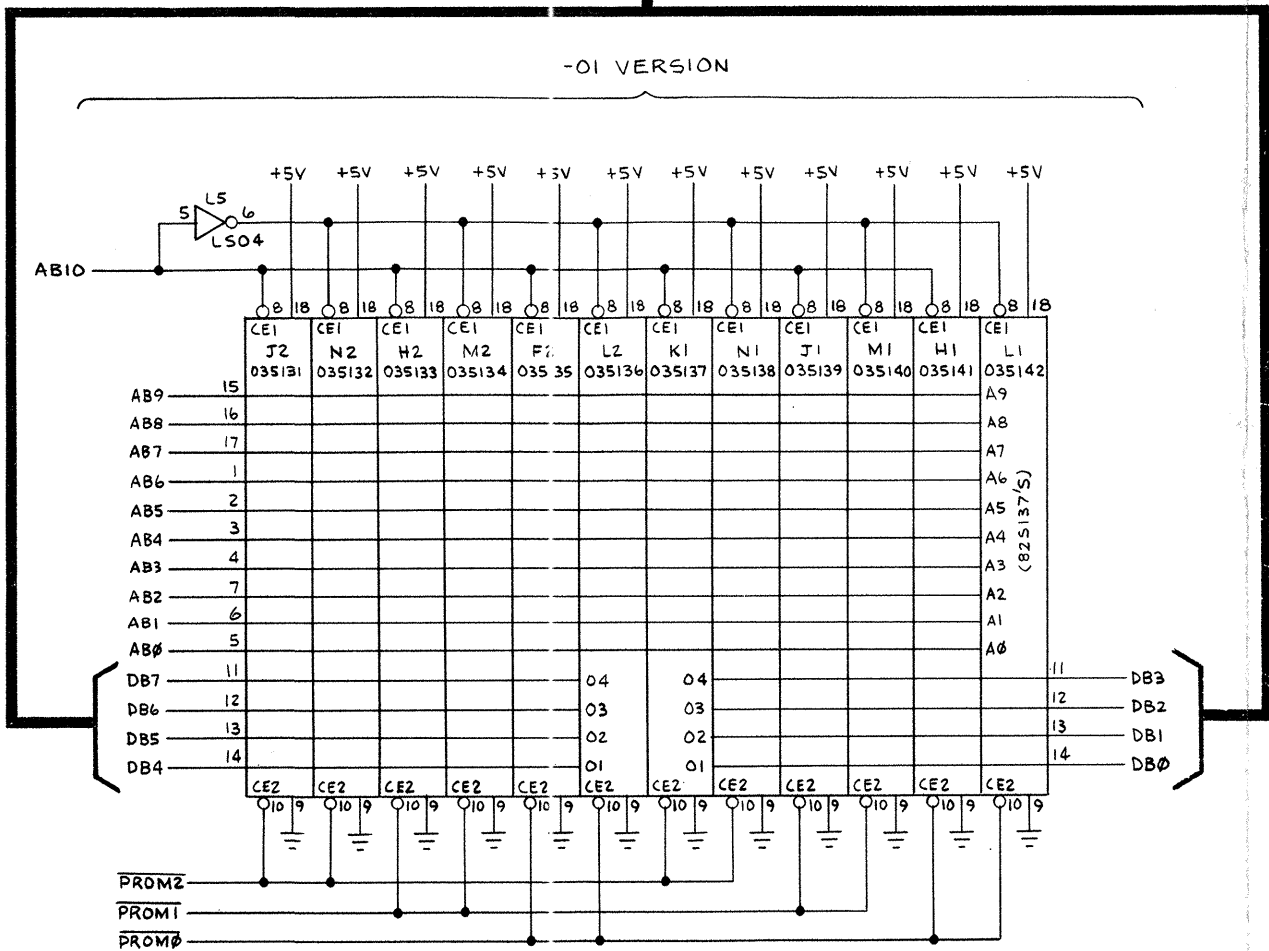
This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR10 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR11 and CR12 rectify the positive pulse of the 36 VAC input and the 7915 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.

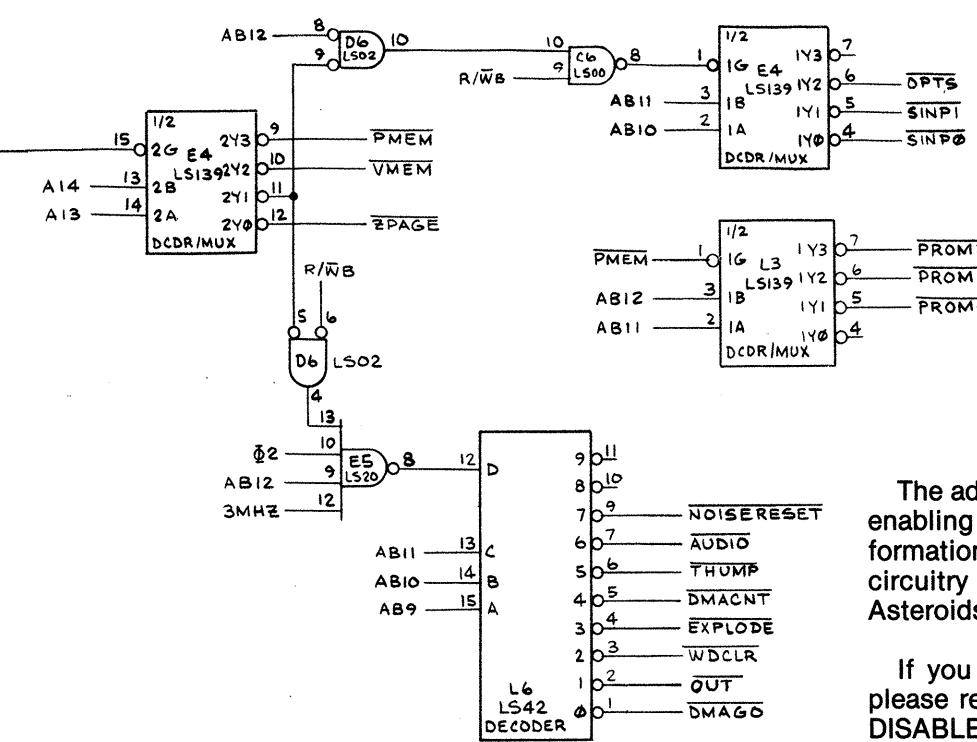


ROM/PROM CIRCUITRY

Program Memory for the Asteroids game is contained in PROMs for the -01 version of the PCB or ROMs for the -02 version of the PCB. One ROM is equivalent to four PROMs. All PROMs connected to a common enable must be removed before replacing with a ROM. For example, remove PROMs at locations F2, H1, L2 and L1 before replacing with ROM at location F1.



ADDRESS DECODING CIRCUITRY



The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids game.

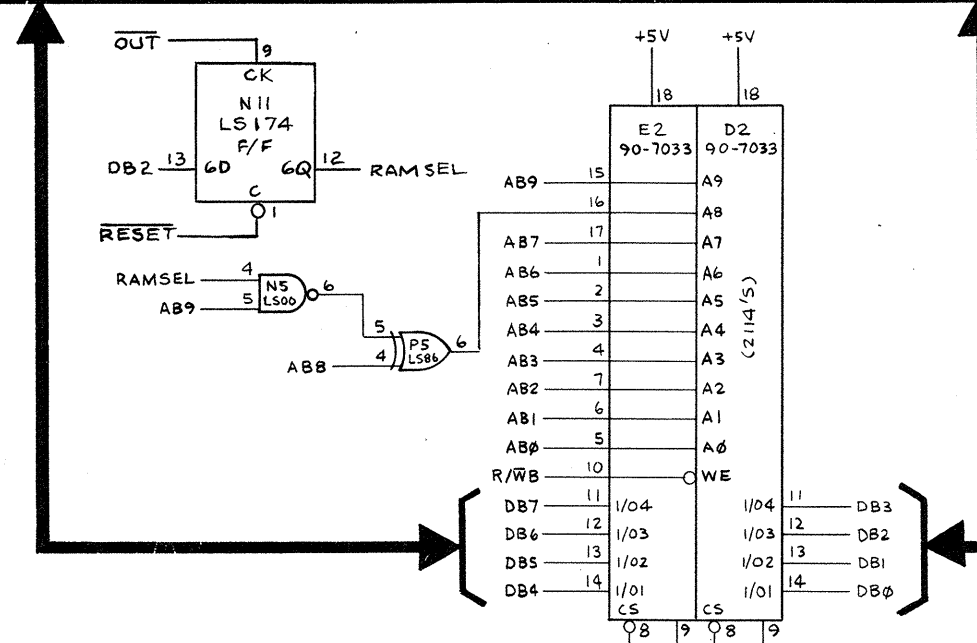
If you are going to use the Automatic RAM/ROM Test, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

HEXADDECIMAL	ADDRESS																DATA																FUNCTION
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0								
0000-01FF	0	0	0	0	0	0	0	1	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	ZERO & ONE PAGE RAM							
0200-02FF	0	0	0	0	0	0	1	0	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	PLAYER 1 RAM							
0300-03FF	0	0	0	0	0	0	1	1	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	PLAYER 2 RAM							
2001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	3 KHz							
2002	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	HALT							
2003	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	HYPERSPACE SW							
2004	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	FIRE SW							
2005	0	1	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	DIAG. STEP							
2006	0	1	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	SLAM SW							
2007	0	1	0	0	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	SELF TEST SW							
2400	0	1	0	0	0	1	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	D	D	LEFT COIN SW							
2401	0	1	0	0	0	1	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	D	D	CENTER COIN SW							
2402	0	1	0	0	0	1	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	D	D	RIGHT COIN SW							
2403	0	1	0	0	0	1	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	1 PLYR START SW							
2404	0	1	0	0	0	1	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	2 PLYR START SW							
2405	0	1	0	0	0	1	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	THRUST SW							
2406	0	1	0	0	0	1	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	ROT LEFT SW							
2407	0	1	0	0	0	1	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	D	ROT RIGHT SW							
2800	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	D	D	OPT SW (SW6, SW7)							
2801	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	OPT SW (SW6, SW5)							
2802	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	OPT SW (SW4, SW3)							
2803	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	R	D	D	D	D	D	D	D	D	D	OPT SW (SW2, SW1)							
3000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	DMAGO							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	2 PLYR START LAMP							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	1 PLYR START LAMP							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	RAMSEL							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	COIN CNTRL LEFT							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	COIN CNTRL CENTER							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	COIN CNTRL RIGHT							
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	WDCLR							
3600	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	EXPLOSION PITCH							
3600	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	EXPLOSION VOLUME							
3A00	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	THUMP VOLUME							
3A00	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	THUMP FREQUENCY							
3C00	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	SAUCER SOUND							
3C01	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	SAUCER FIRE SOUND							
3C02	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	SAUCER SOUND SELECT							
3C03	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	SHIP FIRE SOUND							
3C04	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	SHIP FIRE SOUND							
3C05	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	LIFE SOUND							
3E00	0	1	1	0	0	1	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	D	D	NOISE RESET							
4000-47FF	1	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	VECTOR RAM							
5000-5FFF	1	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	VECTOR PROM							
6800-7FFF	1	1	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	PROGRAM							

RAM CIRCUITRY

The RAM is the temporary storage space for the MPU and is enabled when ZPAGE (Zero Page enable) is low. When R/WB (from the MPU) is low, the RAM stores the data byte input (DB0 thru DB7) at the location addressed by the MPU address bus (AB0 thru AB7). When R/WB is high, the MPU reads the stored data byte at the addressed location.

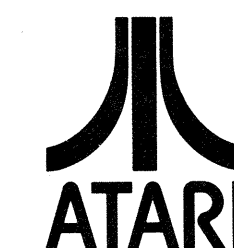
The signal RAMSEL, when low, has the effect of swapping pages 2 and 3 within the RAM. This allows greater programming flexibility.



Memory Components and Their Equivalents (Locations Shown in Bold)

-01 P.C. Boards (PROMs)	Alternate -01 P.C. Boards (PROMs)	-02 P.C. Boards (ROMs)
035131-01 J2		
035132-01 N2	035150-01 J2	
035137-01 K1		035143-01 C1
035138-01 N1	035153-01 K1	
035133-01 H2		
035134-01 M2	035151-01 H2	
035139-01 J1		
035140-01 M1	035154-01 J1	
035135-01 F2		
035136-01 L2		
035141-01 H1		035144-01 D/E1
035142-01 L1	035155-01 H1	

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Sheet 1, Side B
ASTEROIDS
Microprocessor

Section of 034986-XX F