ATARI INTER-OFFICE MEMO

TO : Distribution

FROM : Pat Brosnan

Date : Nov.26,1985

Subject : Conversion of Pole Position II boards from Japanese to English.

Fourteen changes are to be made to convert these boards from Japanese to English. Thirteen will be Eprom changes which we can reprogram inhouse. The other one will have to be ordered. The modifications to the CPU and Video boards are as follows :

136014-176 3L
136014-177 4L

CPU Board :

Remove	Insert	Location	
PP1-11	136014-147	2E	SOUND
PP1-12	-	2F	NOT NEEDED FOR CHEERING CROWD
PP1-13	-	1E	
PP1-14	-	1F	
PP4-5	136014-178	4M	FOR INSTRUCTION AT THE START OF THE GAME AND FOR ATARI NAME
PP4-6	136014-179	4L	
PP4-7*	136014-184	3M	
PP4-8*	136014-185	3L	

* These Eproms are 2732's they will be replaced by 2764'S.

Video Board :

Remove	Insert	Location	
PP1-19	136014-166	4N	
PP1-20	136014-167	4M	* MAINLY TO CHANGE "PREPARE TO QUALIFY" SIGN TO ENGLISH.
PP1-21	136014-168	3N	
PP1-22	136014-169	3M	
PP4-23	136014-174	~~2N~~ 2M *	
PP4-24	136014-175	~~2M~~ 2N *	HAVE TO CHANGE OTHERS BECAUSE OF THE ABOVE BEING CHANGED OTHERWISE SIGNS WILL LOOK WRONG.
PP4-25	136014-170	1N	
PP4-26	136014-171	1M	
PP4-6	136014-192**	6M *	

** This the IC which will have to be ordered as we are unable to copy it.

NOTE: There is an added connector put on the CPU board for some reason. We do not have any use for this connector so it will be removed.

cc. F.Murphy, J.Nugent, M.Nevin, A.Doyle

*
28165 ATAR EISSSS

TOO15

C/MN.

cc: JN
CS
FM
AD
AC
DS.

TO: ATARI IRELAND LTD MR. MIKE NEVIN
FROM: HIDE NAKAJIMA
DATE: NOV. 15, '85

150 POLE POSITION-II PCBS WERE SHIPPED 11/15/85.
ADDITIONAL 50 PCS WILL BE SHIPPED 11/20/85.
ONLY DIFERENCES BETWEEN US VERSION AND JAPANESE VERSION ARE:
1. VOICE 2. BILL BOARDS IN THE BACK GROUND OF THE RACE TRACK.

ALL THE BILL BOARDS ARE HOWEVER WRITTEN IN ENGLISH WHICH NEED NO CHANGES.
VOICE YOU'LL HERE IS A LADY SAYING ''QUALIFYING ROUND. START.'' IN JAPANESE.

OF COURSE IT IS BETTER IF NAMCO CAN CHANGE IT TO ENGLISH BUT IT SEEMS IMPOSSIBLE TO DO SO AT THIS TIME. BESIDES THIS JAPANESE ANNOUNCEMENT IS NOT A CRITICAL DEFECT OF THE GAME, AT ALL.
SO PLS TALK TO GOLDSTEIN THAT HE SHOULD NOT WORRY ANYTHING ABOUT THE VOICE.

IN FACT, ALL POLE POSITION COPIES WHICH WERE SMUGLED AND SOLD IN EUROPE (OVER 1000 PCS?) WERE WITH JAPANESE VOICE.
NO JAPANESE LAUNGAGES NOR VOICES BESIDE THIS ARE NOT IN THE PCBS ACCORDING TO THE BEST OF MY KNOWLEDGE. IN ADDITION, THE PEOPLE HERE HAVE BEEN TRYING SO HARD TO GATHER ALL 200 PCBS FOR IRELAND AND TOO LATE TO CHANGE OUR ORDER TO THEM.

YOUR UNDERSTANDING OF THE SITUATION AND YOURS AND DEVE'S EXTRA EFFORT TO MAKE GERALD UNDERSTAND THAT THERE SHOULD BE NO PROBLEM WILL BE APPRECIATED.

VIDEO BOARD PROBLEMS.
1) "PREPARE TO QUALIFY" IN JAPANESE
2) "PUSH PEDAL TO START"

THANKS AND REGARDS,
HIDE NAKAJIMA IN TOKYO

.....

1) can be changed.

Pat
File in my Pole Position Manual

c.c. F. Murphy
M. O'Rourke
B. Egan
E. McGrath.

Inter-Office Memo

ATARI
Games Division

To: Pat Bradman

From: Sam Deus Sam (DAVE WIESENSON'S INPUT)

Subject: Pole Position M.O. Problems Date: June 25, 1984

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1. Tearing of Cars and Signs:

   a. 9H, 9J, 10H, 10J, 10K, 10L, should be S161 - not National parts.
   b. 8D should be S158. A F158 works even better here.
   c. 7C, 6A should be S04. I've seen a 100 PF cap on Pin 4 to GND sometimes help, but officially this is not a good practice.
   d. 8B should be S00. (5 PART)
   e. Custom 04 at 7E is a rare problem. Try different date code.

2. Spotting of Cars and Signs:

   a. 9F, 10F must be 55ns parts.
   b. See 1a, 1c, 1d.

3. Look at signal on 9L-9. Should be clean pulse. If pulse and spike then try lift 9L-9 and connect 10B-5 to 9L-9.

4. On PPII, it is normal for a sign to tear only near or approaching the bridge with people over the course. This happens because too many motion objects are being displayed.

SD:jdh

29-6-84 PROBLEM WITH CUSTOM 04 with date codes 86-88.

FIELD SERVICE

Inter-Office Memo

ATARI
Games Division

21 NOV 1983

cc. M.J.O'R.
P. Brosnan
F. Murphy
K. Hayes.
T. Guerin

To: Darl Davidson

From: Sam Deus

Subject: Pole Position P.C. Board Problems

Date: 11/3/83

Our last run of Pole Position boards showed a high percentage of failures. The symptom of the failure is random RAM errors on the power up. This problem has been in existence since early builds, but never as severely as this run. Dave and I have been examining the problem very closely for the past few days. Here is the summary:

1.) Problem symptom: RAM failures in the self test on power up.

2.) Actual problem: The way that NAMCO designed the logic. The section of the logic using two PROMs (135, 136) as chip select and buffer enable decoders. Random gliches on the outputs of the PROMs generating improper chip selects at inappropriate times causing data to change in the RAMs.

3.) Why has this problem appeared all of a sudden?: Because the combination of IC's that we are using are very sensitive to the gliches. These include very fast Harris PROMs that react to changing address lines and produce excessive noise.

4.) Immediate solution: Currently bypassing one of the address lines with a 150 pF capacitor. This is not an ultimate solution but keeps the line going.

5.) What is the final solution?: Of course it would be a re-design, but that is out of the question. The reasonable solution is to use a different manufacturers PROMs which are slower than Harris parts. The first time National parts could become of some use. Because the National parts are slower, they operate somewhat like a filter and do not generate as many gliches. Unfortunately, all we have in inventory is Harris parts and there isn't enough time to get any Manufacturer's part into production in time to catch the last of the build.

I anticipate that when this batch of boards hits the market that you will get a small percentage of failures and complaints from the field. Be prepared to explain to our customers what the problem is and how to fix it. This is all I can think of that we can do. Please advise me if you see any other way that we can be of some help.

SD:br

cc: JOHN RAY
EMONN MC GRATH
DICK RECART
[illegible] HANCAT
WOODY WOODWORTH
FRANK BECKER

Inter-Office Memo

ATARI
Games Division

03 OCT 1983

To: Pat McSweeney

From: Sam Deus

Subject: Pole Position II Upgradability Date: 8/25/83

Since Pole Position II is coming in the very near future, I thought it would be a good idea to get the Pole Position boards ready now for upgrading to Pole Position II. My reasons for implementing this are as follows:

To upgrade the existing Pole Position boards, the labor cost will be considerably larger than if we were to exchange EPROMs and PROMs on Pole Position II ready boards.

To upgrade the Pole Position boards that are already built will require the following:

A) Unsoldering 7 PROMs and soldering 7 new ones.

B) Unsoldering two 24 pin sockets and soldering two 28 pin sockets.

C) Soldering three new 28 pin sockets into currently unused locations (after clearing the solder filled holes).

D) Replacing 16 new EPROMs and removing 12 old ones.

Unbuilt boards can be made ready for Pole Position II upgrading by stuffing 12 sockets for the cost of about 90 cents. This may not save any money directly to Atari, as a matter of fact, it will add to our cost, unless we have to do the upgrading at inventory level. However, it will have indirect benefits and will save allot of money for our future customers and 2000 less headaches to our field service department. If you agree with me on this, please let me know and I will give you the information on what needs to be done.

SD/br

cc: Darl Davidson
Singh Mangat
Dick Maslana
John Ray
Dan Van Elderen
Woody Woodworth

cc. Earnest
Martin
Frank
Elaine

Select BO.

Inter-Office Memo

ATARI
Coin-Operated Games Division

FIELD SERVICE
22 AUG 1983

cc. M.D.O.F.

To: Nancy Perkins

From: Sam Deus Sam.

Subject: National I.C. 74LS08 LOCATION 6C Date: 7/27/83

We are experiencing 30% failure on the Pole Position video boards at the final test. Dave Wiebenson's investigation showed that the problem is being caused by a combination of glich and a sensitive IC (National 74LS08) on the P.C. board. This part is currently on the A.V.L. list. We do not have substantial evidence to say that the part is defective or out of spec. However, the best solution to the problem is not to use the part at the present time until we find a better solution to control the documentation. It is best to replace all of the National IC's at the problem location of the video boards currently in production to avoid further problems in the field.

SD/br

cc: Dean Charrier
Rich Cocciolone
Darl Davidson

PROBLEM

INTERMITTENT RAM 0 DISPLAYED ON POWER-UP
-SOMETIMES CLEARS.

Copy all FSP
Elaine
Jeanette
Mike

ATARI

INTER-OFFICE MEMO

TO : M. O'Rourke, T. Guerin, Files

FROM : Eamonn McGrath EMC

DATE : 14th February, 1983

SUBJECT : Pole Position USA Board Problems

We experienced a greater than average Board failure rate in the first run of Atari Boards. This was attributed to a great extent to Audio Problems.

When I reported this to Sam Deus (Project Engineer), he was surprised that this audio problem had not been fixed by PCB test in the USA. They were aware of the problem and had a fix for it. This Audio problem will be fixed on Rev C PCB's. The bad Audio was apparent in all cases on immediate power-up and these boards should not have passed inspection in the PCB test area in USA.

For the record, the following are the three possible fault areas and soloutions, as discussed with Sam Deus on 10/2/83.

Problem 1. Bad Audio on 1 channel:
Timing Problem on Sound Rams

Solution: Add 220PF Cap between C6 and Ground on CPU PCB.
(Page 6B of SP. 218).

Problem 2. Color Dots on Motion Objects - Timing problems, parts specially selected.

Solution: Replace LS158 101th S158 at 8D on video PCB.
(Page 15A of SP.218).

Problem 3: Odd colors on CARS when using Mask Programmed Roms

Solution: Cut and lift Pin 1 of 11L and tie to Ground on Video PCB.
(Page 14A of SP. 218).

EMCG/vh

Famous

Inter Office Memo

ATARI®

Coin Operated Games Division

08 JUN 1983

To: Field Service Personel

From: Bernie Barranger BB

Subject: Pole Position

Date: May 25, 1983

Some power supply assemblies are developing lug contact problems on the bridge rectifier terminal. The heat generated at the terminal can melt the fuse and transformer wire insulation.

The solution at present is to inform the game owners to solder the transformer wire directly to the terminal.

BB/pd

Inter Office Memo

ATARI®

Coin Operated Games Division

23 DEC 1982

To: Darl Davidson

From: Bob Salmons

Subject: Pole Position Score-To-Date Date: Dec. 8, 1982

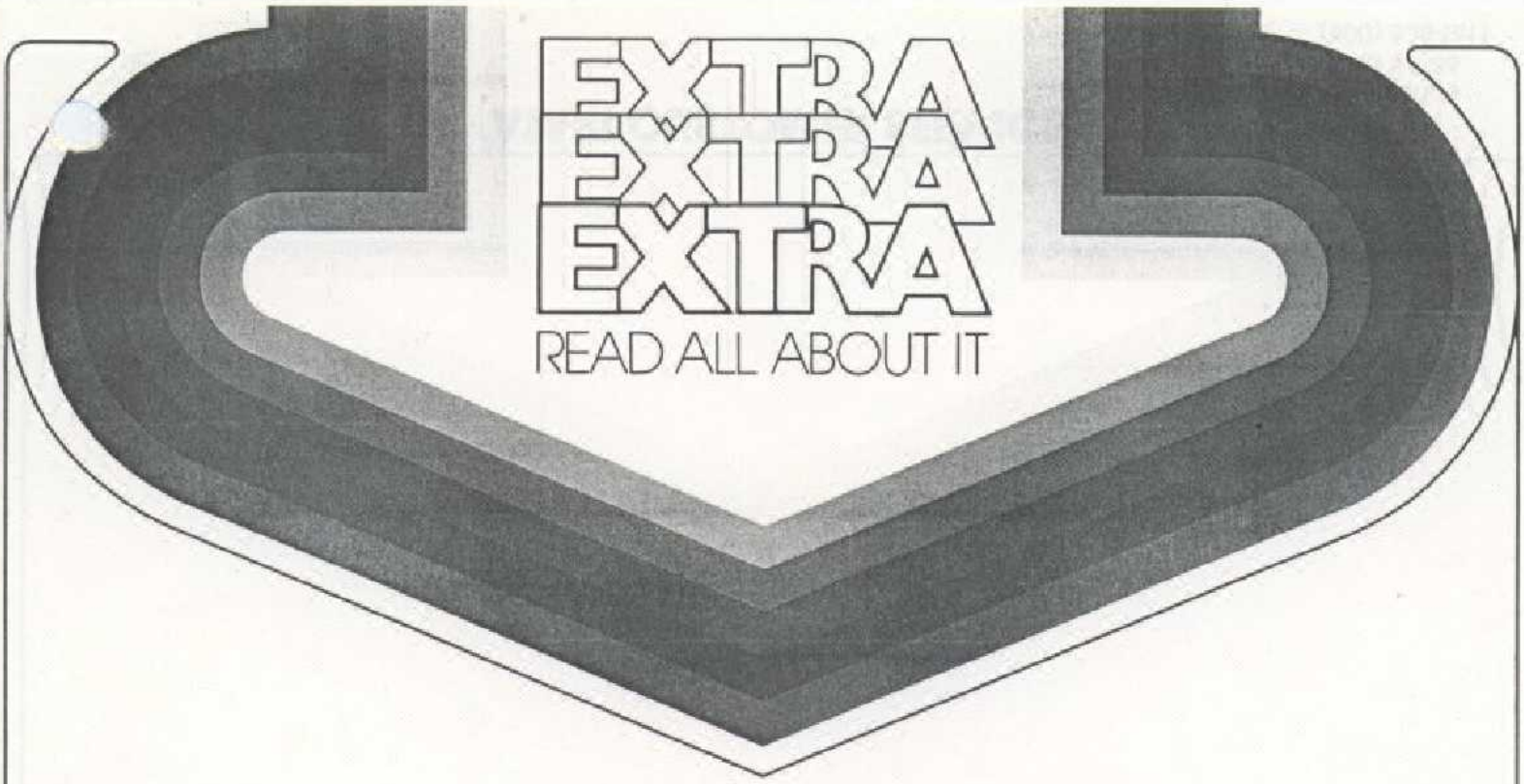
PROBLEM: Some Pole Positon games do not retain high score-to-date memory. The game allows you to write your name, but it does not save in memory.

SOLUTION: American Board: Replace CR6 a 1N4728 3.3v Zener Diode on CPU board to a 1N748A 3.9v ¼watt Zener Diode or a 1N5228 3.9v ½watt Zener Diode.

Japanese Board: Replace D10 a 1N4728 3.3v Zener Diode on CPU board to a 1N748A 3.9v ¼watt Zener Diode or a 1N5228 3.9v ½watt Zener Diode.

BS/ca

cc: Jim Alexander
Russ Mac Donald
Bernie Barranger
Frank Becker
Russell Gorr
Eamonn McGrath
Sunnyvale Techs
New Jersey Techs



IMPORTANT

08 FEB 1983

Pole Position Test Plugs

The CTS/1 Regulator Audio Board will not provide sufficient current for both the CPU and Video Board + 5 volt lines.

Use a second Regulator / Audio Board to provide +5 volts for the Video PCB.

Double crimp this + 5 volts onto terminal 3 of the 3 position Amp Video Power Connector, and ground to pin 2.

FIELD SERVICE BULLETIN

Eanlonn

Inter Office Memo

FIELD SERVICE 14 MAR 1983

ATARI®

Coin Operated Games Division

To: Field Service

From: Bernie Barranger BB

Subject: Pole Position ROM Failure

Date: March 4, 1983

Incorporate the following chart in the manual.

SELF TEST SCREEN DISPLAY
FAILED ROM CPU BOARD

DISPLAY	ATARI PCB	NAMCO PCB
ROM 0	7H	6H
ROM 1	7F	5H
ROM 2	3E	8M
ROM 3	4E	8L
ROM 4	3D	7M
ROM 5	4D	7L
ROM 6	3L	4M
ROM 7	4L	4L
ROM 8	3K	3M
ROM 9	4K	3L

BB/ca

Inter Office Memo

FIELD SERVICE
22 NOV 1982

ATARI
Coin Operated Games Division

To: ~~Sam Deus~~

From: Chris Downend Chris P. Downend

Subject: Coin Input Problem on Pole Position Date: 3 November 1982

I recommend the following solution. This is a modification of Solution #5 from your memo dated November 2, 1982. Build our games in the factory as follows:

A. Sitdown Games (These will be set on 50¢ play most of the time.)

1. Disconnect the wire from Coin Switch 2 and connect it to the same input as Coin Switch 1. This means that a coin placed in either coin mechanism registers in the same coin counter and the problem disappears. However, it creates a problem with the manual. The operator also looses the ability to put different denomination coin mechanisms in the same game.

2. Add a stuffer sheet to the manual explaining to the operator that the coin option switch listed for "Coin 1" work for both coin mechanisms and the option settings listed under "Coin 2" do not apply.

B. Upright Games (These will be on 25¢ play most of the time.)

1. Leave the coin switches connected to separate inputs with separate option selections. This creates a problem if a game is placed in 50¢ play.

2. Add a stuffer sheet to the manual warning the operator that, "In 2 Coin/1 Credit or 3 Coin/1 Credit or 3 Coin/2 Credit or 4 Coin/3 Credit coin modes, the multiple coins must be placed in the same coin mechanism." Also explain how to wire both coin switches to the same input.

I think this is the best solution since:

Solution #1 cannot happen in time.
Solution #2 creates a less reliable product (2 coin mechs are more reliable than one).
Solution #3 advertises we screwed up.
Solution #4 advertises we screwed up and irritates operators.

CD:cak
cc: S. Calfee
B. Falconer
M. Fujihara
D. Hawes
D. Van Elderen

Nov. 21, 1984

Pole Position Video Board — Manufacturing Defects

The principle problem with the Pole Position Video boards was a masking error; $\overline{VSYNC}$ was being disrupted by a signal which was being output from pin 8 of IC 2J. Pin 8 of 2J had to be cut & lifted from the feedthru pad because the $\overline{VSYNC}$ trace was erroneously masked & subsequently etched from pin 17 of IC 2F (custom IC 07) to pin 8 of IC 2J (74LS10) which is supposed to be an unused output, Not an input. See page 3 of 10 (Video PC BD schematics)