5. SIMCHECK II OPERATION

This section outlines the operation of SIMCHECK II, or SIMCHECK II se. It instructs you on how to handle the SIMM sockets, and describes all the SIMCHECK II tests in some detail. We strongly recommend that you read at least this section before putting the manual away.

5.1 INSERTION AND REMOVAL OF MODULES

1. Do not insert or remove a module when the Module Power red LED is on! (Press ESC to turn it off prior to insertion/removal.)

2. Do not insert two modules at the same time.

3. Never use excessive force to insert a SIMM module. If a module is not sliding in smoothly - please review the instructions on this page.

4. When testing 30-pin or 72-pin SIMMs, remove the Sync Adapter.

INSERTION:

Make sure the Module Power **red** LED is off (if not - press ESC). 30-pin SIMM modules are inserted into the lower socket and 72-pin SIMM modules are inserted into the larger socket above. Note that the lower left corner has a curved notch for pin 1 identification. Also notice that there are standard holes on each side of the module. The socket has two flanges that can be pushed back about 35 degrees. Inspect them closely and notice that each flange has a pin which is designed to enter into the holes on the module's sides when they are correctly inserted. With very gentle pressure, insert the module into the socket and tilt it backward (thus also tilting the flanges) until the small pins on the socket flanges enter the holes in the module sides. With both hands return the flanges to the normal vertical position until the SIMM module enters the socket. Practice it a few times and you will be amazed how easy it is compared to working with regular SIMM sockets!

REMOVAL:

Make sure that the Module Power **red** LED is off (if not - press ESC). In certain modules, the **red** LED may still be glowing slightly, even when the tester is in Standby Mode; if this occurs, it is still safe to remove the module from the socket, as the module is allowing only a minor amount of leakage current to flow. This however, should not be an indication of a defective device.

Place one finger on top of the SIMM module to **prevent the module from popping upward** and simultaneously push the two flanges away from you.

NOTE: Both SIMM sockets are of the best available quality. They are rated for 10,000 to 30,000 cycles of removal and insertion. Using them carefully will provide you with a long period of use. In particular, do not subject them to humidity and always follow the above instructions for smooth handling.

5.2 MEMORY TYPES AND TEST CATEGORIES

5.2.1 SDRAM AND EDO/FPM MEMORY TYPES

SDRAM technology is radically different than STANDARD EDO/FPM DRAM technology. As it offers significant advantages and has become widely used, we have released new test equipment to support this technology.

The SIMCHECK overall test flow for SDRAM memory types is similar to the test flow for EDO/FPM memory types, with the exception that the Single Bit test is not used for SDRAM devices. Therefore, you will need to ignore Section 5.3.5 when testing SDRAM devices

Section 5.4 of the manual covers SDRAM testing, as used by the Sync DIMMCHECK 168 (part of the SIMCHECK II/II se PLUS), the Sync DIMMCHECK 144, the Sync DIMMCHECK 100, and the Sync CHIP TESTER. Much of the information covered in Section 5.3, which primarily describes the EDO/FPM tests, is also relevant for SDRAM testing.

Throughout this manual we will use the term 'Sync Adapter' when making a general reference to any one of these items. We will omit the '168' or '144' or '100' unless it is necessary to distinguish one unit from the other.

5.2.2 TEST CATEGORIES

SIMCHECK II tests are composed of a variety of routines. They are generally divided into two categories:

1. Within-Specification tests.
2. Out-of-Specification tests.

The first group of tests is done with the module operating within

the manufacturer's specifications and conventional safety margins. Detected errors are therefore indicative of a definite chip malfunction and the test is terminated with an error message (and an audible signal).

The second category of tests makes use of comparative tests during which the module is operating outside its normal specifications. This type of test gives some indication of the module's behavior under varying conditions, for example, relative cell storage leakage at various temperatures, or at Out-of-Specification voltage spikes. These tests, called Relative Refresh and Relative Voltage Spikes, provide you with comparative figures, not with absolute Engineering Units. For example: a refresh figure "5", is indicating a "better" refresh performance than "4". No error messages are given by this type of test, because the module is working outside its specifications. However, the comparative figures, combined with common sense, can help detect some unique problems. For example: let's assume that we suspect a module to be defective, yet it passes all the Within-Specification tests. During the Out-of-Specification test phase we notice that the comparative refresh figure is much lower than normally seen on other modules. This leads to suspicion of a potential intermittent refresh problem.

The Out-of-Specification tests are part of the EXTENSIVE test described later in this section. **Notice that under no condition is the module operated outside its absolute maximum ratings.**

5.3 TEST MODES AND PHASES

SIMCHECK II employs a wide variety of test modes, which makes it more than just a go/no-go tester. SIMCHECK II provides a detailed insight into the **quality** of the tested module.

SIMCHECK II tests work in either MULTI-BYTE or a SINGLE BIT mode:

- **MULTI-BYTE** test checks all the bits simultaneously.
- **SINGLE BIT** test checks each bit individually. The Single Bit test is not used for SDRAM testing.

The main tests of SIMCHECK II, the BASIC test, the EXTENSIVE test, and the AUTO-LOOP are MULTI-BYTE tests.

SIMCHECK II starts with the BASIC test which lasts between 2 and 30 seconds, depending on module size. The EXTENSIVE test automatically follows the BASIC test and it lasts several minutes. It includes different voltage and temperature related test procedures, as well as mode analysis. The AUTO-LOOP test proceeds in an endless loop of varying pattern (and algorithm) tests.

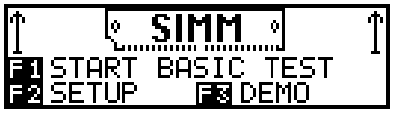
You can terminate a test at any time or switch to the SINGLE BIT test for testing a particular bit on the DUT.

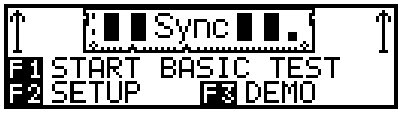
The following sub-sections describe each of the default main test phases: BASIC, EXTENSIVE, AUTO-LOOP, and the optional SINGLE BIT.

Section 6. describes the SIMCHECK II SETUP mode which allows you to perform advanced tests in which you setup your own parameters and testflow.

5.3.1 STANDBY MODE

SIMCHECK II's starting mode is the STANDBY mode where you are prompted with the following message to insert a module and start the test:





This is the mode when you are not testing any devices and SIMCHECK II tries to reduce its own power consumption.

From STANDBY mode, you select the following actions:

F1 - starts the automatic test which is described in the following sections.

F2 - allows you access to all of SIMCHECK II's advanced setup functions which are described in Section 6.

F3 - run the DEMO program.

F4 -allows you to view the Test Log or to view the modified setup of SIMCHECK II.

The **Test Log** is a unique feature of SIMCHECK II. It is actually a scrollable list of all the results obtained during the last test. The information in the Test Log remains until you

perform a new test.

F5 -is used by our technical personnel to run SIMCHECK II's extensive diagnostic programs.

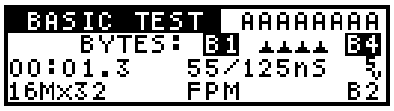
5.3.2 BASIC TEST

The initial group of tests determines module size, mode type, speed, cycle time, and looks for basic wiring, addressing, and defective bit problems.

Some devices utilize various wiring or addressing variations of the original JEDEC standard. This variation is legitimate on specific motherboards, but may result in failure in other motherboards that do not support this variation. If SIMCHECK II encounters such legitimate variation, it will flash a short warning message as in the following screen:

But it will not stop the test as this module will work perfectly in all motherboards that support the 4K refresh feature.

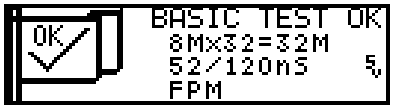
During BASIC test, the graphic display shows animation depicting the progress of the test, a test timer, module type and size. The shortened notation 55/125nS indicates the module as having an access time of 55nS and a cycle time of 125nS (Please refer to APPENDIX D for an explanation of cycle time measurement).



You will also note the '5_V' voltage indicator next to the access and cycle time. The '5_V' or the '3_V' marks indicate that the DUT is being tested as a 5V or a 3.3V device. The animation characters show the DUT at bit or bytes resolution. For example, the above screen shows a x32 device, which requires 4 bytes

animation characters. Similarly, a x40 module will require 5 byte animation characters, while a x72 requires eight. The screen also displays the HEX code of the current test pattern used on the top right corner. The B2 at the bottom right corner indicates BANK 2 is currently being tested.

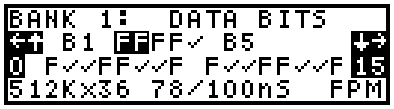
If the module passes the BASIC test, a few summary screens will follow to provide additional information on the module tested, including a translation of the JEDEC notation to the module size in whole.



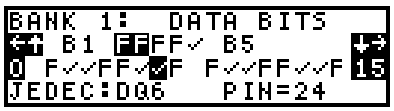
If a problem is detected, the test is halted with the corresponding error message. If no initial problem is detected, the test continues with **every cell being written to and read from several times with different basic bit patterns.**

Refer to section 4.5.6 for other types of error menus.

In case of data bits error, the test halts and the defective bits ("chips") are indicated as in the following message:

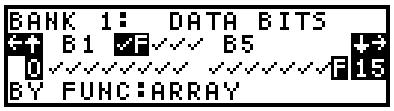


Pressing the ← or → keys allows you to examine the memory array two bytes at a time. In the above example, Bytes 1 and 2 are currently selected, and the corresponding 8 bits per byte are displayed. Pressing ↓ allows you to move down one line to examine each defective bit. The display at the bottom will then change to identify the data line corresponding to the selected bit and its pin number as indicated below:



The example above indicates that Byte 1 and Byte 2 are selected. Bit 7 of Byte 1 is being examined by the user as being DQ6 and being located on pin 24 of the module. Pressing ↑ allows you to move up one line and subsequently select to view the remaining bytes.

By pressing ↓ a few times, you can scroll down through more error information as discussed in Section 4.5.6. These include error address information, actual write/read pattern information, and more details about the test function type which caused the error to result:

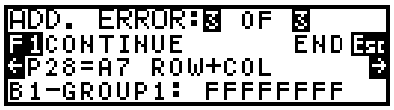


Many other types of errors may be detected by SIMCHECK II.

The following screen shows an Address Column error in address line A0 (pin 12) of Bank 1, Group 1.

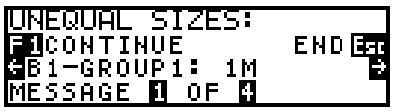
We use Group1 or Group2 to describe how the memory device data bus is mapped onto SIMCHECK II's internal 32 bit bus. Memory devices with 32 bits or less are directly mapped to Group1. Memory devices with 33 to 40 bits are mapped to Group1 and Group2. In Group2, bits 33 to 40 are mapped to the most significant byte.
In the example, the '00000004' hex code indicates that the above address error occurred only in the third bit of group 1.

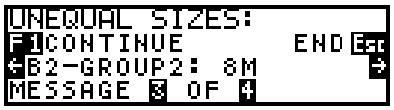
The next example shows another instance of an address error:



The first line of error information indicates that the error was found in both the row and the column portion of the address. The code in bank 1, group 1 is 'FFFFFFFF' indicating that all the data bits mapped to this group exhibit the address error, leading to the conclusion that the fault in this case, is at the DUT connector and is, indeed, common to the entire group.

The Unequal Sizes error message appears when different banks or different data bit groups of the same DUT exhibit different sizes, as shown in the following screens:





The first screen shows that Bank1-Group1 has 1M, while the second screen shows that Bank2-Group2 has 8M.

All the errors are also recorded in the Test Log, which can be viewed by pressing F4 from the STANDBY mode. The following partial sequence of two screens shows how the Test Log indicates an inconsistency in the Mode type of the various groups:

The first screen indicates the device to be FPM (Fast Page Mode) while the second screen shows that in Bank1-Group2 the mode was NIBBLE instead of FPM.

You can also activate this screen by pressing F5 during the BASIC test.

Detailed Structure Information:

SIMCHECK II provides explicit information on the module's structure, after a successful BASIC test. Such information is illustrated below:

The above screen shows the structure of the tested module as being JEDEC type, having 2 Banks, 4 RAS control lines and 4 CAS control lines. SIMCHECK II also provides information on

the PRD settings and tells if the module is ECC type.

Some complex DUT require more than one screen for their structure information. Device type errors which precede BASIC test are also shown on the second structure information screen.

ON-THE-FLY PARAMETER CHANGES

Except when using the Sync DIMMCHECK 168, change-on-the-fly is not available on SIMCHECK II se. Use setup instead.

```
CHANGE-ON-THE-FLY:
F1 SPEED     Esc RETURN
F2 VOLTAGE
```

You can change some test parameters on the fly using our "one feature. Simply press F2 during the BASIC TEST to access this function, then make the necessary selection. Because this is a "one time" change, the next memory device tested will not be affected.

The BASIC test determines the fastest Access Time of the tested memory device as well as the cycle time of the module. See Section 6 for details about the more advanced Speed Setup, which remains in effect also after you turn your SIMCHECK II off.

"One Time" Speed Override:

This kind of speed override is in effect only while the current module is tested. To set a "one time" speed override, press F2 as stated above during the BASIC test to reach the CHANGE-ON-THE-FLY screen, then press F1 to select SPEED.

```
SPEED OVERRIDE:
61nS

↑↓RAS ACCESS:  61nS ↓→
```

Afterwards, use the ← or → to position the cursor over the current speed and then press either the ↑ or ↓ keys to increase or decrease the value. Press F1 to enter your selected speed. Thereafter, subsequent test phases will be conducted at the selected speed, as displayed on the screen with an "@" marker. Note that this speed override is not effective during the SINGLE BIT test.

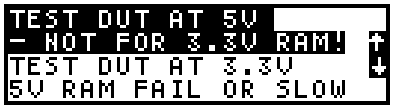
When using the Sync Adapter, the speed override feature allows you to set a "one time" frequency override.

```
SPEED OVERRIDE:
100MHz
F1 ENTER        ABORT Esc
← 100MHz              →
```

Like the regular access time override, an "@" marker will appear on subsequent test phases. Use the ← and → keys to scroll through the available frequency rates.

"One Time" Voltage Override:

To set a "one time" voltage override, press F2 during the BASIC test to reach the CHANGE-ON-THE-FLY screen, then select F2 for voltage. The following screen will be displayed:



You may use ↑ or ↓ to select the voltage setting that is to be used for this test, then press F1 to start the test at the selected value.

Please note that devices such as the Sync DIMMCHECK Adapters, the DIMMCHECK 168P PRO and the DIMMCHECK 144P PRO, which will detect 3V devices, will not alter the voltage even if it is changed-on-the-fly.

Next Phase:

- If an error is detected, the defective bit(s) are identified and you can use the various error menus to examine all the details of the error. Press ESC to return to STANDBY mode. Before you press F1 to test your next device, you can press **F4** to view the Test Log of the last tested DUT.

You can skip BASIC test to reach the EXTENSIVE test for DUT that fails BASIC test. See Section 6.

- In the default SIMCHECK II testflow, you cannot reach EXTENSIVE and AUTO-LOOP tests unless the BASIC TEST has been completed successfully.

- If you do not elect to terminate the test after BASIC test, the following menu appears, prompting you to select the next test:

Press **F1** to go to EXTENSIVE test, **F2** to go to AUTO-LOOP, or **F3** to go to the SINGLE BIT test. If 5 seconds

pass with no user selection the EXTENSIVE test is initiated.

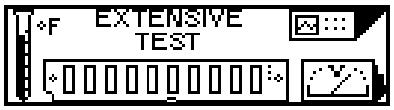
- As always, ESC terminates the test. Before you press F1 to test your next device, you can press **F4** to view the Test Log of the last tested DUT.

THE BASIC TEST IS SUFFICIENT FOR MOST SCREENING TESTS. Most defective modules will be detected during this test.

Significance of Successful BASIC Test:

The BASIC test provides module type and speed information. It verifies that all wiring on the module is sound and that all cells in the module are operative. It also confirms basic refresh capabilities. It may not detect intermittent and/or pattern sensitivity problems due to its short execution time.

5.3.3 EXTENSIVE TEST



The EXTENSIVE test is an extremely comprehensive test! Module behavior is tested under varying voltage conditions, including numerous test functions, thereby achieving a remarkably high reliability level.

What is being tested:

Pressing F1 during the EXTENSIVE test terminates the current step and proceeds to the next one (within the EXTENSIVE test).

- **Voltage Cycling:** Testing under all allowable voltage conditions. These include 4.50V, 4.75V, 5.00V, 5.25V, and 5.50V (or the range of 3.00V to 3.60V for low voltage devices).
- **Mode Test:** Testing the special DRAM mode of the DUT. DRAM technology uses two common modes: EDO and Fast Page mode. Older memory devices may use the Nibble mode and the Static Column mode. Fast Page mode is the most widely available mode, with EDO growing in popularity. Mode failure does not halt the test, but the offending bits are shown with 'X' marks. If you test a nibble mode DRAM memory, the display will show 'XXXXXXXX'. Static column modules should pass this test. Hard failure (which is not part of a specific mode), terminates the test with the familiar 'F' marks. Upon completing the mode test, the SIMCHECK II test program will display explicit information, using the notation 'EDO'

for Extended Data Output Mode, 'FPM' for Fast Page mode, 'Nibble' for Nibble mode, and 'SCM' for Static Column mode. This test also provides a measurement of the Tac parameter, or the access time from CAS, of the memory device. The value is displayed briefly during the test and is recorded in the test log.

- **Voltage Bounce:** Testing data retention during voltage variation between read and write (e.g. write at 4.5V, read at 5.5V, or write at 3.6V and read at 3.0V and vice versa).

- **March Up/Down:** The march up/down algorithm is designed to reveal intricate problems caused by adjacent cell interference. In simplified terms, the test is done by first writing 0 to all memory locations, then, while scanning from first address to last address, the test verifies that a 0 remains in each location, then it is replaced with a 1. After the entire memory address is "marched up" in this fashion, the process reverses itself to perform the "march down" test. This time while scanning from the last address to the first address, the test verifies that a 1 remains in each location and then replaces it with a 0. SIMCHECK II's new implementation of the March Up/Down algorithm is more advanced than our previous implementation in the original SIMCHECK, and it also incorporates several extra steps.

Please refer to Section 6.3.5 for information on Refresh Setup.

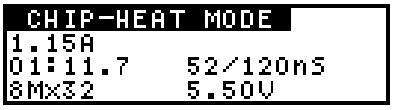
- **Relative Refresh/cell leakage:** This test provides a relative value for the ability of the memory chip to retain data between refresh cycles. "Relative" means that the result is not an absolute time value but a comparative one. Relative relation between values is exponential.
  For example: A chip with a relative value of "5" retained data integrity twice as long as one with a value of "4" without requiring refresh. Typical good values are 3 and higher. Since this test is of the Out-of-Specification type, lower results do not imply that a module is defective, as it can still work within its published specifications!

- **Relative Voltage Spikes Performance:** This test provides a relative value that indicates how well a module can sustain voltage spikes before a data loss occurs. Relative relations here are not exponential. Typical good values are 3 and above. Since this test is of the Out-of-Specification type, lower results do not imply that a module is defective, as it can still work within its published specifications!

As you watch the red Module Power LED during the Relative Voltage Spikes test, you will see that it flashes vigorously. This LED is directly connected to the module's power supply. SIMCHECK II creates artificial voltage spikes (of 5V to 1.5V or to 6.0V) after loading a complete test pattern. Memory devices with higher Relative Voltage Spikes figures can withstand more spikes in an actual application. Take into account that modules with larger built-in capacitors normally exhibit higher Relative Voltage Spikes figures due to the capacitors' smoothing effect on the spikes. Some complex modules, which utilize PAL chips and/or logic chips, may exhibit significantly lower Relative Voltage Spikes figures.

Note that ALL relative tests are absolutely safe, as SIMCHECK II DOES NOT exceed any allowable voltage/current rating!

- **Temperature stress test (Chip-Heat mode):** In this phase, SIMCHECK II tests memory chips at the actual higher operation temperature experienced inside a computer. Being able to test at the proper temperature is extremely important because some memory problems are not exhibited until the chip is warmed up. As the mode progresses, you will note that SIMCHECK II will display the heating current in Ampere units.



The Chip-Heat mode utilizes a unique phenomenon which was revealed in our research. When a DRAM chip is subjected to a unique waveform pattern, it is heated internally without the need of external heating techniques. Furthermore, this Chip-Heat method is absolutely safe as we explicitly DO NOT use higher voltages or currents beyond the memory manufacturer's ratings.

The EXTENSIVE test display shows the current test type, duration of test, applied voltage, Access Time (speed) and Cycle Time, and module mode type and size. The final test results look similar to those of the BASIC test. Note that because the DUT is tested at a higher temperature during the Chip-Heat portion of

the EXTENSIVE test, the Access Time might be slower than the value obtained at the BASIC test.

Next Phase:

- If an error is detected during the EXTENSIVE test, the defective bit(s) are identified and the display waits for your acknowledgment. Press ESC to terminate the test or F3 to go to the SINGLE BIT test (not for SDRAM testing).

- If no errors are detected - an OK test result is shown and you are prompted to continue. Press F1 to go to AUTO-LOOP. Press F3 to go to the SINGLE BIT test (not for SDRAM testing). If the time delay passes with no user selection, the AUTO-LOOP test is initiated.

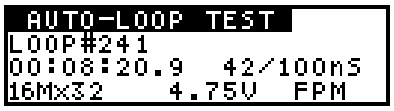
- As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

Significance of Successful Test:

The EXTENSIVE test verifies proper module operation under varying voltage conditions. It will detect intermittent problems which are either temperature dependent or resulting from adjacent cell interference. It provides comparative scores of module performance. It further tests the module with additional data patterns besides those utilized by the BASIC test.

5.3.4 AUTO-LOOP TEST

During the AUTO-LOOP test, the module is endlessly tested with different patterns of data bits, generated by different algorithms.



The time of the test, the iteration (loop) number, applied voltage, module speed and cycle time, module size, and mode type are displayed.

Next Phase: The AUTO-LOOP test terminates when an error is detected or in response to the user's command.

- If an error is detected, the defective bit(s) are identified and the display waits for your acknowledgment.
- If no error is detected, the test will continue indefinitely; or until ESC is pressed to terminate the test, or F3 is pressed to go to SINGLE BIT test.
- As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

Significance of a Successful Test:

AUTO-LOOP is designed to detect pattern sensitivity problems, as it tests the modules under many different patterns. 20 minutes or more are sufficient to detect most pattern sensitivity problems.

Notice that the AUTO-LOOP mode makes SIMCHECK II an excellent instrument for continuous burn-in procedure.

5.3.5 SINGLE BIT TEST

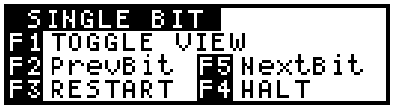
The SINGLE BIT test allows you to test each individual data bit of the EDO/FPM module by itself with minimal interference from

other data bits. This is achieved by activating only the actual RASx and CASx control lines which connect to the currently tested bit. Since each control line usually activates several chips (each typically have more than one bit), all the bits except the one currently tested are masked out to avoid interference.

You can select the SINGLE BIT test any time by pressing F3 from the BASIC test, EXTENSIVE test, or AUTO-LOOP.

If an error was found by the BASIC test, you may still go to the SINGLE BIT test from STANDBY during the first three seconds after returning from the error menu.

After the initial SINGLE BIT mode screen, the SINGLE BIT menu will appear giving you the available keyboard options during the test.



During the SINGLE BIT test, each bit is tested sequentially. (We use the term "bit" rather than "chip" because in most modules you have fewer chips than bits as many chips have x4, x8 or even x16 configuration.) The SINGLE BIT test reports the speed of each individual bit and other individual information. **Unlike the MULTI-BYTE test, a detected error in one bit does not terminate the test.** The error message for the bad bit (chip) will stay on the display, but testing of the other bits will continue. Each bit will be progressively indicated as good, by a check mark " ", or not good, by an "**F**". The speed shown will correspond to the currently tested bit. Note that the displayed Access Times in the SINGLE BIT test are per individual bit and not for the module as a whole.

The SINGLE BIT mode is repeated continuously, but it should not be confused with the FULL BYTE AUTO-LOOP mode.

The SINGLE BIT test has two views: the GRAPH view and the BIT view. The GRAPH view shows the status of all bytes of the module, with a local zoom on the currently tested bit. It is similar to SIMCHECK I and is the default viewer.

The BIT view concentrates only on the currently tested bit, showing the exact -CASx and -RASx control lines which are needed to activate only this bit. The BIT view also identifies the tested bit's pin number and its JEDEC's "DQ" name.

You can toggle between the two views at any time during the SINGLE BIT test by pressing F1.

The F2-F5 keys function the same regardless of the selected view. ← allows you to skip left to the previous bit. → allows you to skip right to the next bit. F3 restarts the SINGLE BIT test, and F4 is the HALT button. You can halt the test any time and use ← or → to scan previous results during the HALT mode.

Press F4 once again to continue the test at the current bit setting.

A special progress counter is placed on the top right corner; it shows two numbers, like 23/72. The number on the right, for example 72, indicates the number of bits times the number of banks, which equals to the total of all the individual bits to test. The left number, for example 23, on the progress counter shows how many individual bits have been tested. If you use → to skip several bits, you will see that the left number will not reach 72 until all skipped bits are tested! Once you reach a full test (72/72 or 32/32 or 9/9 etc.), the left number increments at every subsequent bit test.

Next Stage:

- Make no selection to continue SINGLE BIT testing (with changing patterns).

- As always, **ESC** terminates the test. Before you press F1 to test your next device, you can press **F4** to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

5.4 SDRAM TESTING

The SIMCHECK II line provides comprehensive support for testing SDRAM DIMMs and SO DIMMs using the Sync DIMMCHECK 168 (p/n INN-8558-6) and the new Sync DIMMCHECK 144 (p/n INN-8558-7) and Sync DIMMCHECK 100 (p/n INN-8558-8). Additionally, there is the Sync CHIP TESTER (p/n INN-8558-9) for testing individual TSOP SDRAM chips. All Sync DIMMCHECK Adapter units utilize the same patent pending 133MHz test engine, which is combined with the the SIMCHECK II line's 1nS technology to achieve true high-speed testing of your SDRAM modules.

DIMM/S.O. DIMM HANDLING

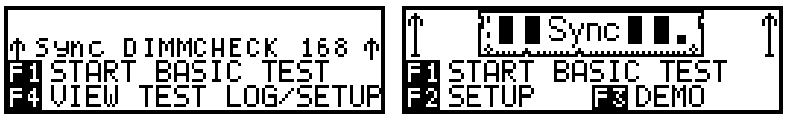
INSERTION: The Sync DIMMCHECK Adapter uses a vertically mounted high quality test socket with two ejectors that need to be opened prior to insertion. Carefully insert the DIMM into the socket, pushing it evenly along its top. When the DIMM is properly inserted, the ejectors will snap onto the semi-circular notches on each side of the module.

REMOVAL: The DIMM is easily released from the socket by pulling both ejectors sideways.

5.4.1 TEST PROCEDURE

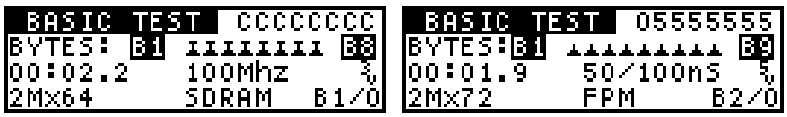
Turn SIMCHECK II ON once the Sync Adapter is installed in

the expansion slot. THERE IS NO NEED TO SETUP SIMCHECK II, as it automatically recognizes this tester. When SIMCHECK II enters the STANDBY mode, the display will reflect the presence of the Sync Adapter. Below is SIMCHECK II's display when using the Sync DIMMCHECK 168.



NOTE: Do not have a module inserted in the Sync Adapter upon initial turn on, as this may load certain signals that are necessary when SIMCHECK II performs its initial locking functions to the adapter.

The Sync Adapter test procedure is initiated by pressing the F1 key as with regular modules. The test procedure is similar to our regular module tests, with the exception that single bit testing is not included for SDRAM modules.



Note that the Sync DIMMCHECK Adapter will automatically recognize and test a DIMM, regardless if it is an SDRAM device, or an EDO or FPM device. For SDRAM DIMMs, the speed is displayed in the form of the module's fastest functional frequency rate, and size is displayed in specific JEDEC notation.

SIMCHECK performs numerous timing tests at the start of the BASIC test in order to determine the frequency of the SDRAM module. Please refer to APPENDIX C to further explain SIMCHECK's speed determination process.

Once the frequency is determined, SIMCHECK will commence to test the entire memory module at the selected frequency. If a problem is encountered, SIMCHECK will automatically reduce the frequency (in the order of 133MHz, 125MHz, 112MHz, 100MHz, 83MHz, 75MHz, and 66MHz), unless you have setup SIMCHECK to test at a fixed frequency by either Setup or the Change-on-the-fly feature. If the tester behaves erratically, with subsequent tests of the same modules giving widely differing frequencies, the problem may be a bad locking of SIMCHECK II and the Sync DIMMCHECK Adapter. Simply remove the

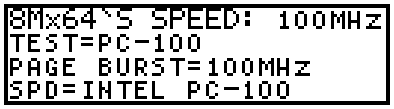
module, reset SIMCHECK by turning it OFF and ON and then try to test again.

During the BASIC test, the screen will inform you of the voltage used to test the module, and display a constant change of patterns used to test it. As we use complex test patterns, only the first pattern is shown. There are two LEDs on the Sync DIMMCHECK Adapter. You will note that the SDRAM LED indicator will glow when an SDRAM module is detected, and as the test procedure continues, you will see the Page Burst LED flash as memory patterns are bursted into the device at real clock rates.

After passing the BASIC test, SIMCHECK II will display our familiar message indicating a successful test, plus additional information on whether the module is a 2 or 4 clock device.

The BASIC TEST OK message is followed by a series of summary screens detailing speed and structure information. Please keep in mind that all speed and structure information is automatically recorded into the Test Log, which is accessible by pressing F4 from standby after the test. The information is retained in the Test Log until a new test is initiated.

Please note that if you want to reach the summary screens quickly, even before the end of the Basic Test, simply abort the test by pressing F5 during the Basic Test.



A necessary Calibration & Upgrade procedure is

The determination of the PC-100 or PC-133 compliance appears on the second line of the screen, and it has the header "TEST=" followed by "PC-100" if SIMCHECK determines that the module is PC-100, or "PC-133" if the module is determined to be PC-133. The third line indicates "PAGE BURST=xxMHz"; it indicates the maximum frequency page burst of the tested module. The fourth line in this example indicates "SPD=INTEL

available from the factory. Refer to Appendix H for details.

PC-100", which indicates that the data in the SPD claims the module to be a PC-100. More examples are shown in APPENDIX C.

If SIMCHECK determines that the module is PC-66, the message "TEST=PC-66" will appear. If a module's SPD is marked for PC-66 while the module timing parameters are measured within the PC-100 range, you will see the message "TEST=PC-100 RANGE". Similarly, if the module exhibits characteristics that place it in the range of being PC-133, SIMCHECK will report "TEST=PC-133 RANGE".

The SINGLE BIT Test Mode is not used for SDRAM testing due to the different structure and behavior of SDRAM devices.

IMPORTANT NOTE: The BASIC Test is the only test used by SIMCHECK II to determine PC-100 or PC-133 compliance. It provides an information summary that gives specific information if the module is compliant with the PC-100 or PC-133 standard.

Your adapter must be equipped with the latest 133MHz test engine in order to achieve these results. It is recommended that your unit be sent for a factory calibration & upgrade procedure to ensure optimum conditioning.

Other frequencies are used throughout the Extensive Test to create additional conditions for the test. Therefore, if a module finishes BASIC Test as PC-133, the fact that it may run at 100MHz during Extensive Test or AUTO LOOP does not mean that the module is not a PC-133.

The first speed summary screen is followed by the Tac measurement screen as in the following examples:

```
8Mx64'S SPEED:
Tac (CL=3): 8.5nS
Tac (CL=2): 8.0nS
83MHz <PC-66>
```

```
4Mx72'S SPEED:
Tac (CL=3): 5.0nS
Tac (CL=2): 5.0nS
Tac RANGE: <PC-133>
```

The screen shows the measurements of Tac (access time from clock) for CAS latency 2 and 3. Please refer to APPENDIX C for further details about these important measurements.

Following this screen will be the module's explicit structure information.

```
16Mx64'S STRUCTURE:
BANKS:2   -S:0+1+2+3
CHIP SIZE: 4x2Mx8
SDRAM 168P UNBUFFERED
```

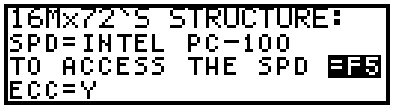
It shows the size of the module, its type, number of the module's banks (not to be mistaken by the individual SDRAM banks), the use of the -S control lines, and the size of the individual chips used in the module. The above example shows an unbuffered 16Mx64 SDRAM module with two banks, using control lines S0, S1, S2, and S3, and employing 4x2Mx8 chips.

The size of each individual chip of the module is shown in the format of [number of banks] x [each chip bank's size in Meg] x [bus width in bits]. The following examples show some typical chip sizes:

2x1Mx8 - a 16Mbit chip with overall size of 2Mx8;
4x2Mx8 - a 64Mbit chips with overall size of 8Mx8;
4x4Mx4 - a 64Mbit chip with overall size of 16Mx4;
2x2Mx4 - a 16Mbit chip with overall size of 4Mx4;
4x1Mx16 - a 64Mbit chip with overall size of 4Mx16.

SPD MANAGEMENT

Most SDRAM modules employ an SPD device. The final structure screen allows you to view the SPD as follows:



SDRAM modules without an SPD will show a 'MISSING SPD!' message. Choosing to view the SPD will stop the test and allow you to review its information, otherwise, the test procedure will continue with the Extensive Test.

NOTE: Please refer to Section 5.5 for detailed SPD Management information on viewing, saving, editing and programming the 256-byte SPD information.

As the test program continues to develop, SIMCHECK will display additional information on SPD. The test log will reflect this by displaying SPD = xx for various characteristics, where xx is the programmed status of the device (i.e. SPD=INTEL PC-100). *This information is provided as a form of translation for the SPD, and is NOT obtained as a result of a measurement of the memory device.* Actual measurements such as access time,

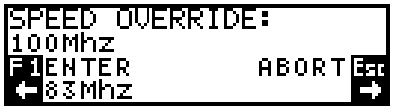
number of banks used, or CAS latency will be displayed without the "SPD =" indicator.

As seen above, SIMCHECK will indicate if the SPD device is programmed to show module compliance with the Intel PC-66, or the PC-100. This indication does not qualify the module for the Intel structure, it is only meant as an indication of the SPD's program.

As seen above, SIMCHECK will indicate if the SPD device is programmed to show module compliance with the Intel PC-66, PC-100, or PC-133. This indication does not qualify the module for the Intel structure, it is only meant as an indication of the SPD's program.

BASIC TEST CHANGE-ON-THE-FLY

The Change-On-The-Fly function is also supported with the Sync DIMMCHECK Adapter. You can access it by pressing F2 during the Basic Test, then selecting either Speed or Refresh override. The SPEED override menu uses a horizontal scroll format:



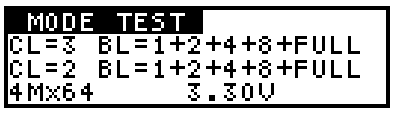
Use the ← and → keys to scroll through the available frequencies: 63MHz, 75MHz, 83MHz, 100MHz, 112MHz, 125MHz and 133MHz. Pressing F1 will restart Basic Test at the selected frequency. If you select a frequency beyond the capabilities of the tested module (e.g. selecting 125MHz), the test will definitely fail. Some PC-100 modules may run at 112MHz. Some modules that are determined to be 83MHz by the automatic mode may still run at 100MHz, however SIMCHECK will still indicate that the module is a PC-66, not a PC-100.

EXTENSIVE TEST

The EXTENSIVE TEST proceeds as with our Standard modules, with the exception of the Relative Refresh and Relative Spikes Tests.

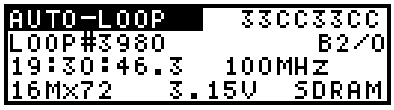
Additionally, the MODE TEST provides information on module

burst lengths:



AUTO LOOP

During the AUTO-LOOP test, the module is endlessly tested with different patterns of data bits, generated by different algorithms.



Some long tests like Self Refresh are incorporated into AUTO LOOP as shown in the following screen:

AUTO-LOOP is an excellent means for a burn-in procedure, as it will continue indefinitely until the user presses the Esc key.

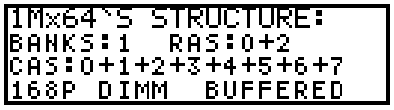
EDO/FPM DIMM TESTING ON THE Sync DIMMCHECK

All Sync DIMMCHECK adapters can test EDO/FPM DIMM modules in accordance to our regular test procedure. There is no need for user setup, as SIMCHECK will automatically recognize SDRAM or EDO/FPM modules. Please note that the LEDs will not glow when Standard DRAM DIMMs are tested. The EDO/FPM DIMM module has an internal architecture similar to the 72-pin SIMM module, but to achieve a wider data bus, the number of -CASx control lines has been doubled from four (-CAS0, 1,2,3) to eight (-CAS0,1,2,3,4,5,6,7). Also, two Write Enable control lines (-WE0 and -WE2) and two Output Enable (-OE0 and -OE2) have been added. This arrangement allows for one-bank (e.g. 1Mx72, 4Mx64, 16Mx80) or two-bank (e.g. 2Mx64, 8Mx72) embodiments. Special A0 and B0 address lines (for the first multiplexed address line) have been implemented within the DIMM 168-pin standard for optimized bank interleaving operation. The 144-pin Small Outline DIMM uses

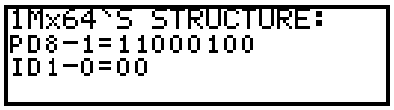
only 2 -RASx lines (-RAS0,1) and no OEx lines.

Simply press F1 to start the test! The Sync DIMMCHECK Adapter will automatically test a Standard EDO/FPM DIMM without setup.

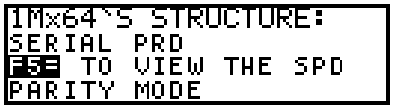
After the BASIC test, SIMCHECK II will provide explicit structure information on the module tested.



SIMCHECK II also provides the PRD settings as well as the ID settings of the DUT.

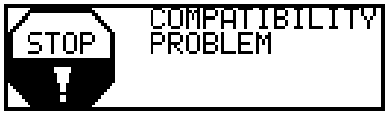


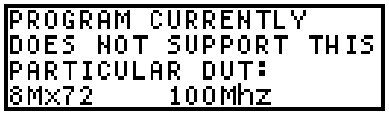
If SIMCHECK II detects the use of an SPD EEPROM chip, a summary screen will appear giving you the option of entering the SPD Management Mode (See Section 5.4.2).



UNSUPPORTED MODULES

As there are various types of modules in the market, you may encounter some that may not be supported in the Sync DIMMCHECK Adapter test tables. SIMCHECK II will then show the following screen displays.





These displays are merely an indication that the tested module is not supported, they are NOT an indication of failure. Please contact us when acquiring these displays, as there may be a need to add this module to our test tables.

5.5 SPD MANAGEMENT

SPD (Serial Presence Detect) is a small 8-pin EEPROM chip mounted on DIMMs & SO DIMMs that includes vital information about the module's parameters.

You can activate the SPD management screen at the start of the Basic Test by entering:

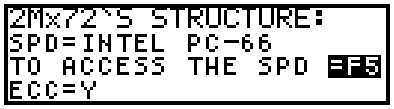
F5 → F5

Or from Standby Mode by entering:

F4 → F3

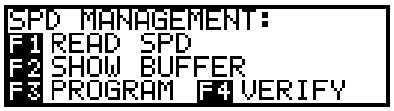
The SPD Management Mode is only available when using the Sync DIMMCHECK 168, the Sync DIMMCHECK 144, the DIMMCHECK 144P PRO, or the DIMMCHECK 168P PRO, and testing a module that uses an SPD.

You can access the SPD Management Mode from Standby Mode by pressing F4, F3. You can also enter this mode after the Basic Test has begun by pressing F5, F3, and F5. At the conclusion of the Basic Test, the final summary screen will give you the option to access the SPD Management Mode once again.



This example shows results obtained with an SDRAM DIMM. SIMCHECK indicates if the SPD device is programmed to show module compliance with the Intel PC-66, or the PC-100.

If you choose not to view the SPD, do nothing, and the test flow will continue as normal. Choosing to view the SPD of the device (by pressing F5) will terminate the test flow and display the SPD management screen.

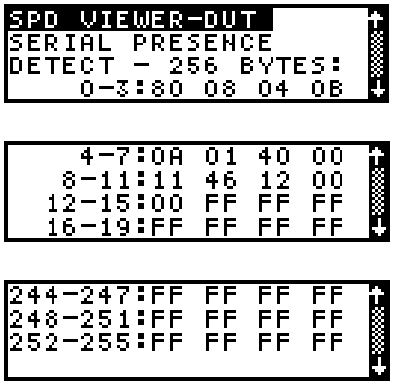


SIMCHECK's SPD Management mode is the operational mode to read and program SPD data.

READ SPD

Press F1 to read the current module's SPD and keep this information in SIMCHECK's buffer. The SPD viewer displays information in a multipage list format. Use the ↑ and ↓ keys to scroll between the pages. The following screen images show a

partial view of the SPD codes for a typical DIMM.



In the above examples, byte 0 contains "80", byte 1 contains "08", byte 5 contains "01", and byte 9 contains "46". You will also note that bytes 244 through 255 contain "FF"; this is an indication that these bytes are not being used.

SIMCHECK's buffer will retain this SPD information until:

a) new SPD data is read;
b) an SPD file is downloaded from the PC Downloader;
c) your SIMCHECK is turned off.

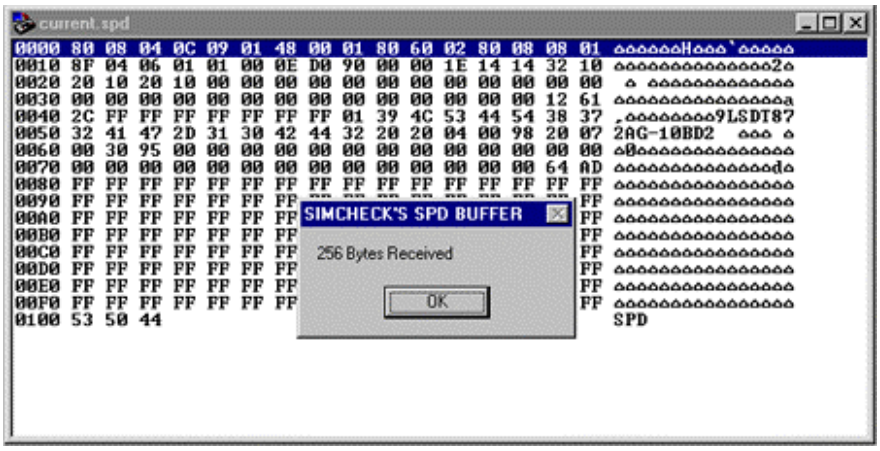
SHOW BUFFER

Use SHOW BUFFER to view the current contents of SIMCHECK's buffer without reading the SPD of a module installed in the tester. This allows you to view the buffer after an SPD file download, or after reading the SPD of a module.

SPD EDITING AND FILING

When SIMCHECK communicates with the PC Program Software, you can further read SPD data into the PC, edit the data on your PC screen, save it into *.spd files on your PC, or download stored SPD files into SIMCHECK's buffer for programming other modules.

NOTE: When viewing information on the PC Screen, the SPD data, as well as the address locations, are displayed in hexadecimal format. When viewing the information on SIMCHECK's LCD display, the address locations are displayed in decimal format, while the SPD data values remain in hex.



SPD PROGRAMMING

SPD programming should only be done by manufacturers and individuals that are well familiar with SPD data; therefore we recommend that these features only be performed by advanced users, as programming a DIMM module's SPD with erroneous data will render the module inoperable!!!

Use **F3** to program the data in the buffer into the SPD on the inserted DIMM module. To avoid casual users from programming wrong SPD data, the default SPD setting in your SIMCHECK is to have SPD programming disabled:

```
PROGRAMMING DISABLED!
USE SETUP-CONFIG-SPD
```

You may enable SPD programming from Standby Mode by entering the following key sequence:

F2 Enters Setup Mode
F3 Enters CONFIG. Menu
F4 MORE
F3 SPD

A warning screen will appear indicating that this function is for advanced users only. To continue, press F1. Select the F2 key to enter Programming Mode,

Please refer to Section 6.5.6 for an explanation of Programming Modes.

Use the right arrow button to select the programming mode. Press F1 to enter your selection. Press the ESC key a few times to return to Standby Mode.

Remember that you must have a valid SPD file in the SIMCHECK buffer (use SHOW BUFFER to make sure) before you start programming. Press F3 from the SPD Management Mode Menu to program your SPD. SIMCHECK programs the SPD and verifies the data with an OK (or fail) message at the bottom of your screen:

VERIFY

The VERIFY function (F4) compares the actual SPD data on the inserted DIMM module with SIMCHECK's internal buffer. This will either indicate OK if the data matches, or FAIL if the data is different.

PRODUCTION MODE

The Production Mode is a special SPD programming setup whereby the SPD of the module being tested is programmed immediately following the test.

This setup is for advanced users only. Those wishing to setup the production mode may acquire further details from our Application Note listed in the Tech Support section of our website.