Debug Port Requirements for the Pentium® Processor

An Application Note

www.arium.com

The following is American Arium's recommendation for implementation of a Pentium® target debug port.

Debug Port Signal Description

Signal	Dir	Pin	Description
TDO	O	13	TAP Data Out
TDI	I	12	TAP Data In
TMS	I	14	TAP Mode Select
TCLK	I	16	TAP Clock
TRST#	I	18	TAP Reset
BSEN#	I	20	Boundary scan (TAP) enable. COMET has access to TAP signals of processor when BSEN# is low.
R/S#	I	7	Processor R/S# signal. (Usually used for the primary processor in a dual processor system.)
R/S#2	I	23	Processor R/S# signal, usually for the secondary processor R/S# signal in a dual processor system.
PRDY	O	11	Processor PRDY signal. (Usually used for the primary processor in a dual processor system.)
PRDY2	O	21	Processor PRDY signal, usually for the secondary processor PRDY signal in a dual processor system.
INIT	O	1	Processor INIT signal (not currently used by American Arium)
RESET	O	3	Processor RESET signal.
DBRESET	I	2	Debugger reset output. When driven high, the target system should reset the system and processor.
DBINST#	I	19	Debugger installed. Installing cable connects this signal to ground, allowing the system to detect the debugger's presence.
VCC	O	6	VCC from target. COMET uses this to detect target powered up. Connect through 1k ohm series resistor.
SMIACT#	O	5	Processor SMIACT# signal. Useful primarily in a single processor system as an extension to the 30-pin debug port definition. *Important: See Note 1.*
GND		4,8,10,15, 17,22,29	Signal grounds. Pin 4 is unique in that it is sensed to determine if a target is attached. *Important: See Note 0 for pin 29 special case.*
N/C		9,24,25,26 ,27,28,30	No Connects

The resistor values given are typical values. Actual values are dependent on the target layout.

Dir (Signal Direction) is relative to target board. O (Out) is from target to ITP port. I (In) is from ITP port to target.

The Debug Port connection is achieved by way of a 30-pin connector specified as an AMP 104068-3. The pinout and suggested circuitry are fully described in the 1994 edition of the *Pentium® Processor Family User's Manual, Volume 1: Data Book, chapter 31, Figures 31-2 through 31-5* from Intel Corporation.

Note 0:

To indicate to American Arium equipment (ECM-55) that SMIACT# is present on pin 5 of a single processor system, connect pin 29 to 3.3v or 5v with a 1k ohm resistor (or less) and bypass to ground with a capacitor of .01 micro Farads or greater.

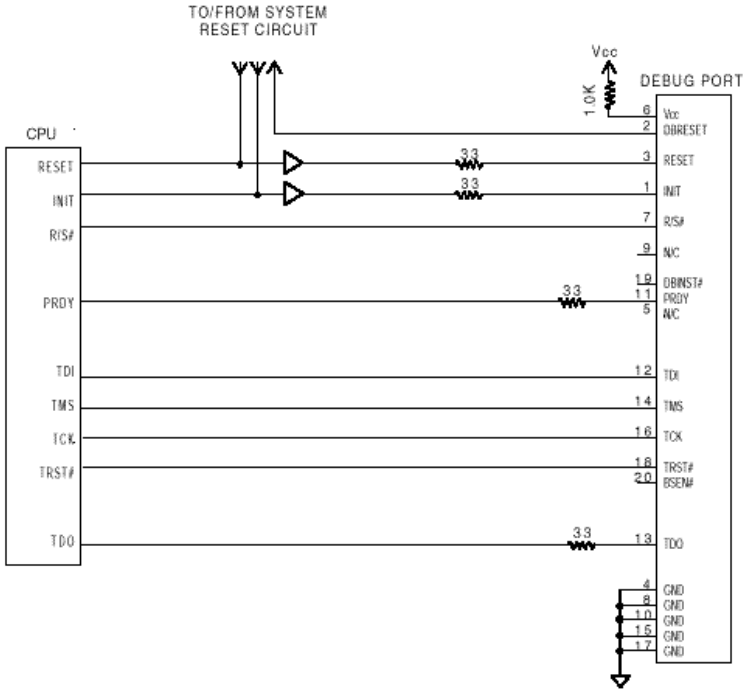
Note 1:

Simply connecting SMIACT# to pin 5 does not serve for dual processor systems. For implementation in a dual processor system, SMIACT# and D/P# must be bussed and an American Arium ECM-55 must be used with WinDb to monitor SMM entry and exit. Additional SMM logic must also be built such that SMM ENTRY is considered when either of the processors has control AND SMIACT# is asserted. SMM EXIT is considered when NEITHER processor is asserting SMIACT#. Regardless, American Arium can only guarantee SMM ENTRY and SMM EXIT breakpoints when using the American Arium POD-W54, TRC-55 or TAP-55 hardware interfaces.

Note 2:

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

The following is a schematic of the Intel defined debug port. Note that SMIACT# is not on this schematic. American Arium recommends adding this connection to pin 5 of the debug port (see Note 1 above)



14281 Chambers Road
Tustin, CA 92780
Voice: 714-731-1661
Fax: 714-731-6344
Web: www.arium.com
E-mail: info@arium.com