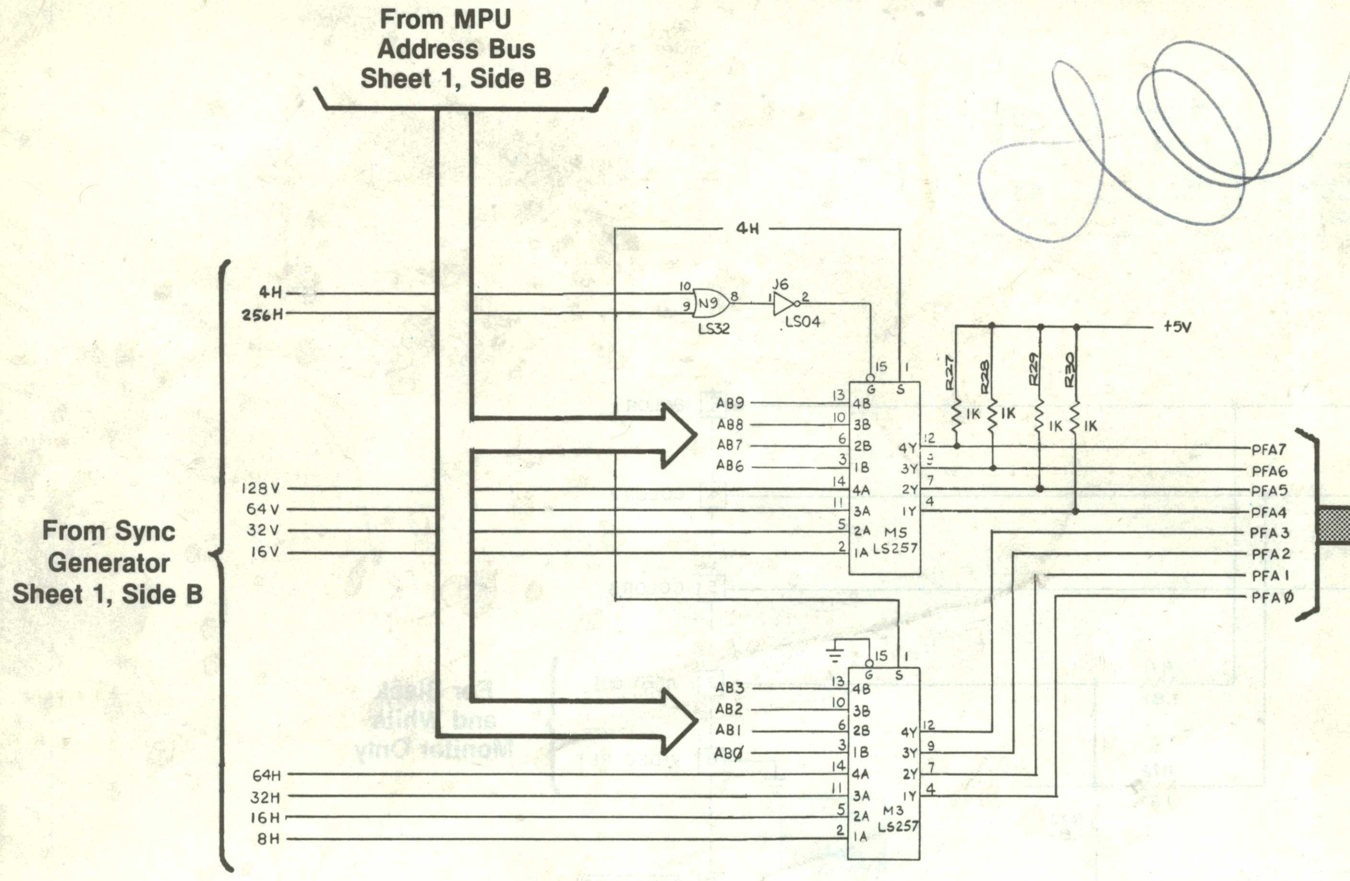
Playfield Address Selector

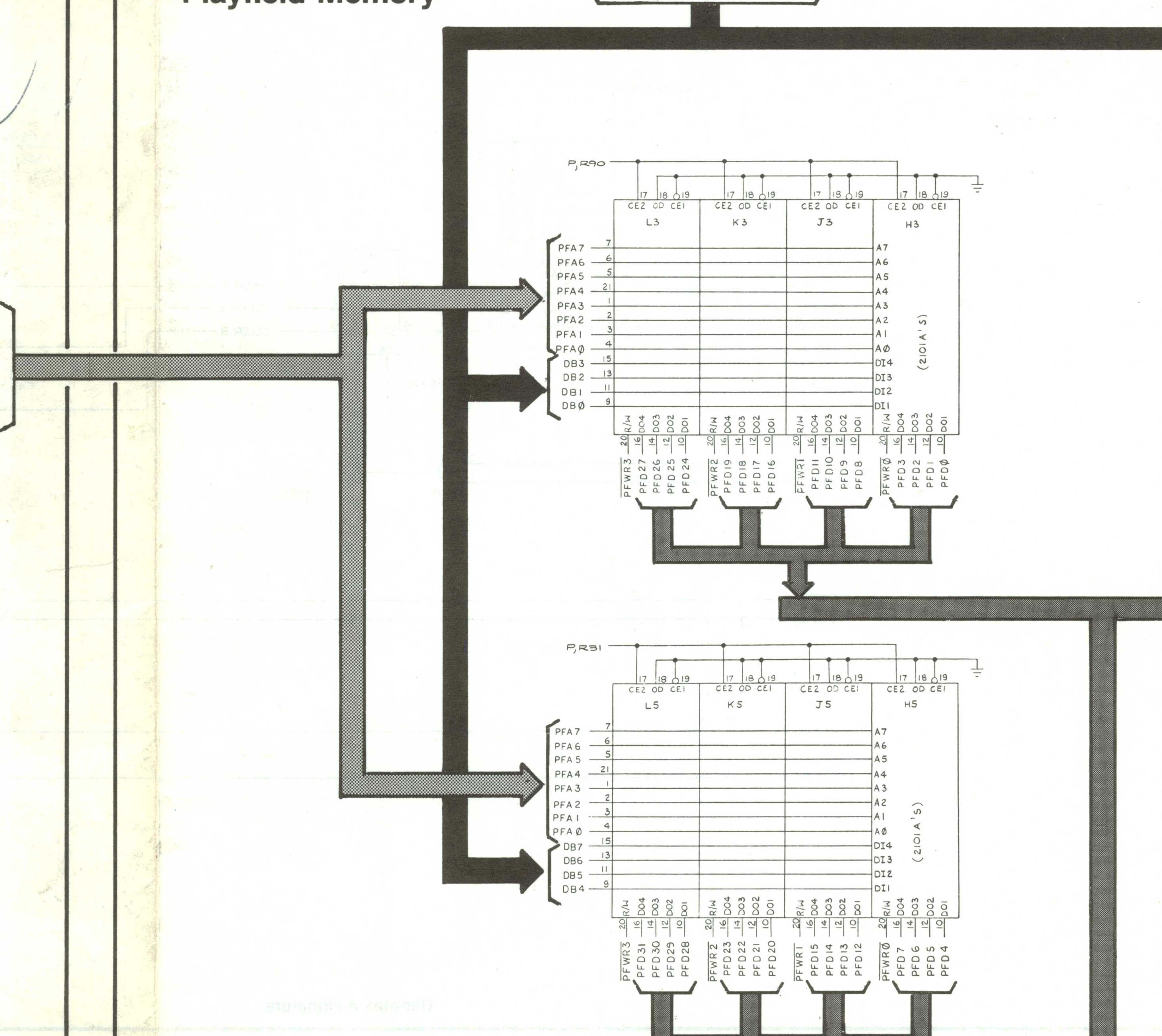


The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers M3, and M5 and gates J6 and N9.

When 4H on pin 1 of M3 and M5 is low and pin 15 on M5 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on M3 and 16V, 32V, 64V, and 128V on M5 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

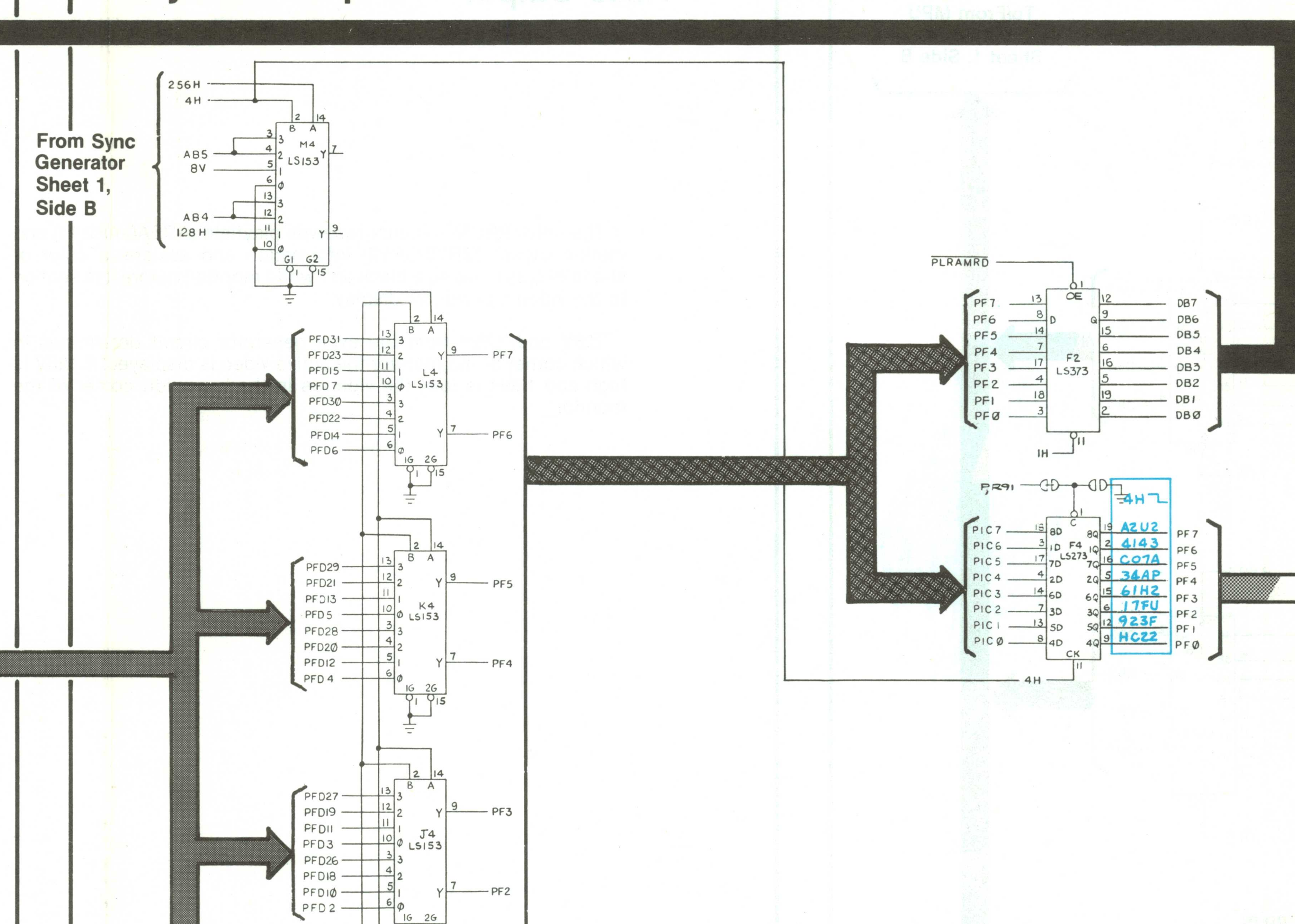
When 4H goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of M5 is high) the outputs of M5 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

Playfield Memory



The playfield RAM contains the playfield display information. The playfield RAM consists of H3, J3, K3, L3, H5, J5, K5, and L5. The alpha, numeric and the playfield picture components are displayed as 8-line by 8-bit blocks of video on the monitor screen. The microprocessor loads the playfield location bits into the playfield RAM via DB0-DB7 and the RAM outputs are PFD0-PFD31.

Playfield Multiplexer



The Playfield Multiplexer receives playfield data from the playfield memory (PFD0-PFD31) and the output (PF0-PF7) is a code that determines what is 1) displayed on the monitor, or 2) read or updated by the MPU. The Playfield Multiplexer consists of select multiplexers H4, J4, K4, L4 and M4.

When 256H is low and 4H is high, AB4 and AB5 from the MPU address bus is the selected output from M4. This output is applied to multiplexers H4, J4, K4, and L4 as select inputs. When the MPU is accessing the playfield code multiplexer, the playfield data is either being read or updated by the MPU. When 256H is high and 4H is low, the inputs from the sync generator (128H and 8V) are the selected outputs. These signals then select which bits of data PFD0-PFD31 are sent out via H4, J4, K4, and L4 for the playfield codes that eventually are displayed on the monitor.

The playfield codes (PF0-PF7) are latched by F2 and F4 to the MPU data bus (F2) and to the picture data PROM circuitry (F4). When PLRAMD is low and 1H from the sync generator goes high, the inputs on F2 (PF0-PF7) are latched out to the MPU via DB0-DB7. When 4H on pin 11 of F4 goes high, the inputs (PF0-PF7) are latched to the picture data PROM circuitry.

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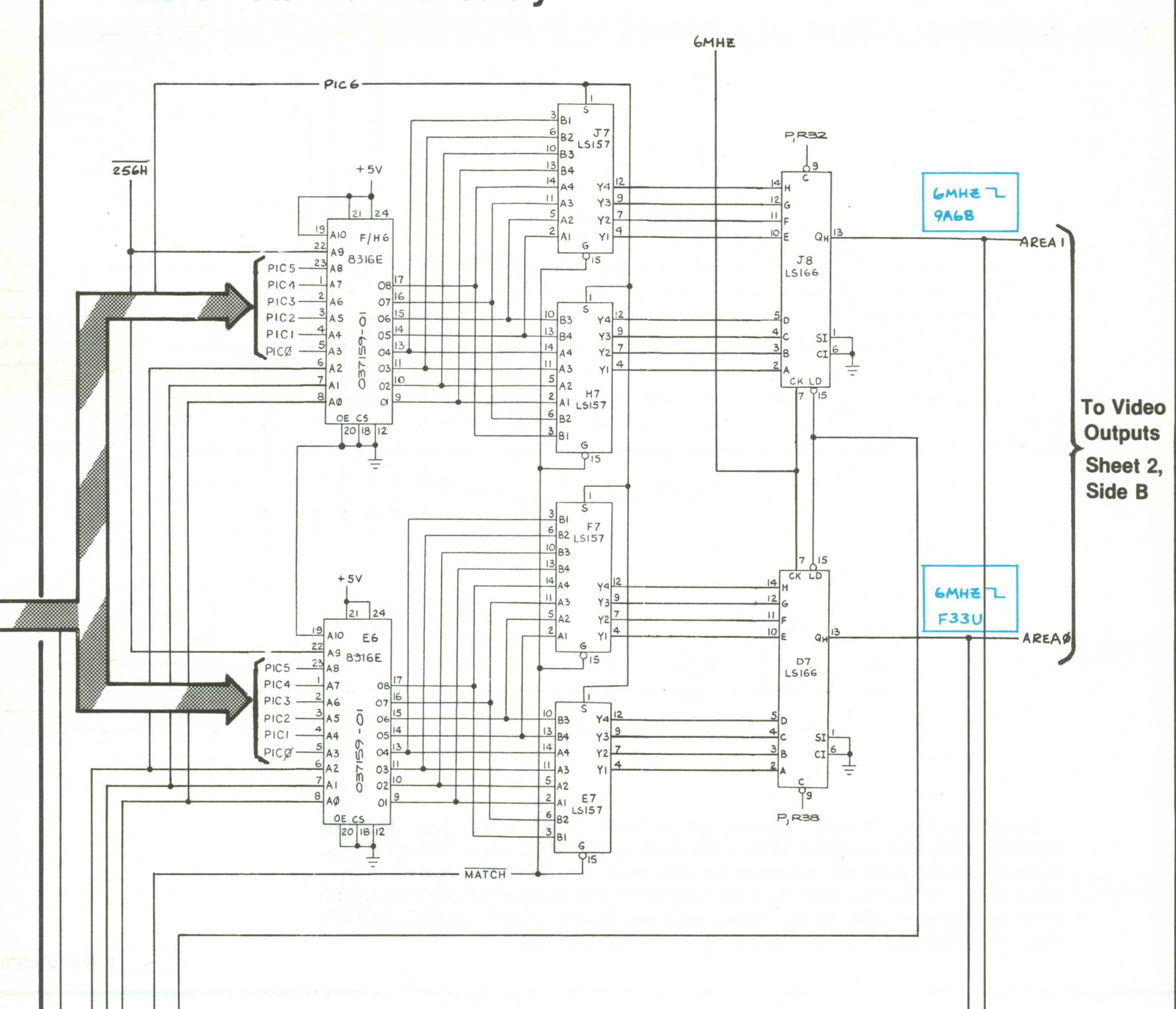
Picture Data ROM Circuitry



The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices E6 and F/H6, multiplexers E7, F7, H7 and J7 and shift registers D7 and J8.

The picture ROMs receive PIC0-PIC5 from the playfield code multiplexer, MGA0-MGA2 (motion graphics address) from the motion object circuitry, and 256H from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA2 set one of eight different combinations of the 8-line by 8-bit blocks of picture video.

256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM outputs D1-D8 on E6 and F/H6, are multiplexed by E7, F7, H7 and J7, and shifted out serially at D7 and J8 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuitry.

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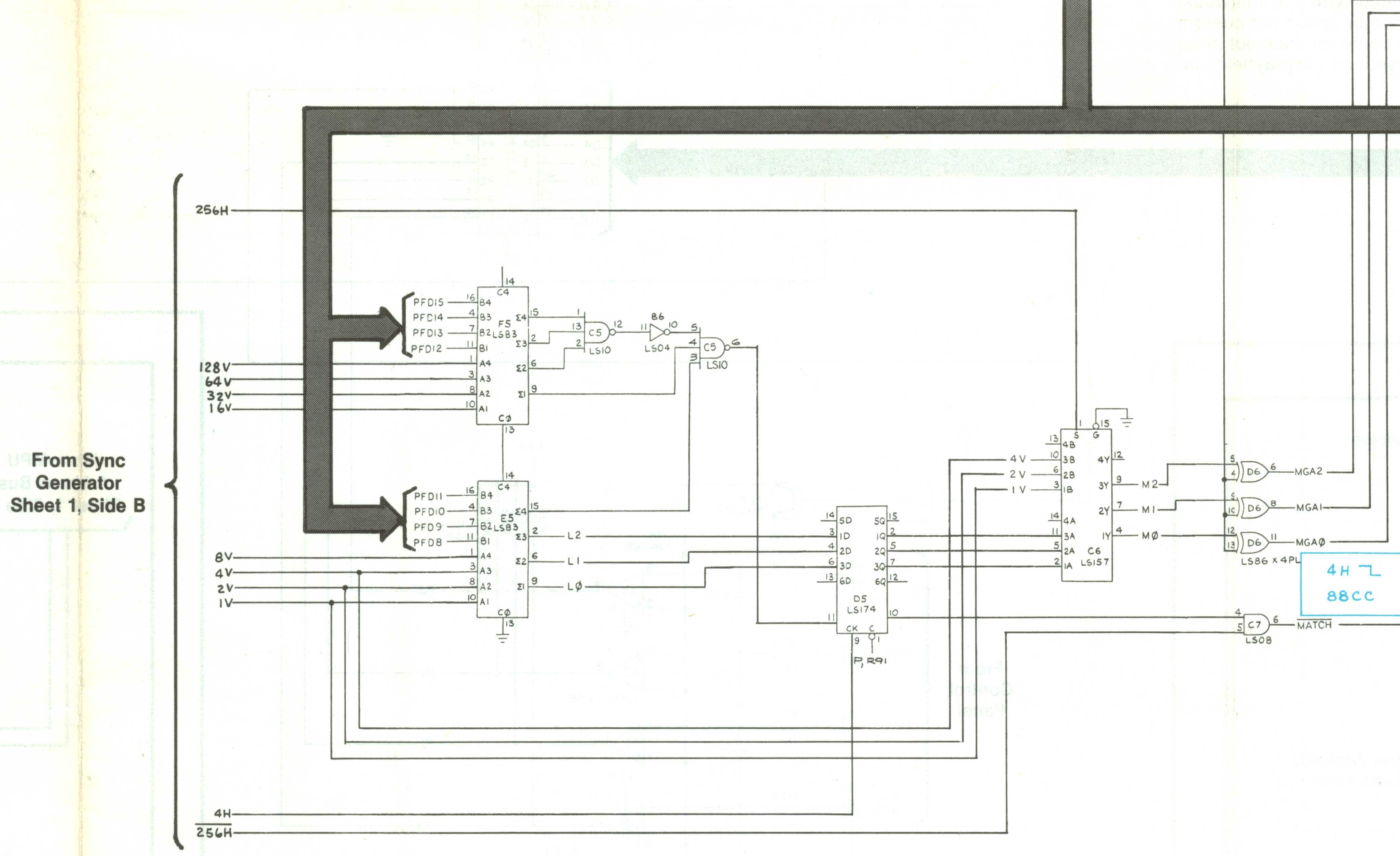
Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry

Section of 036434-01 B

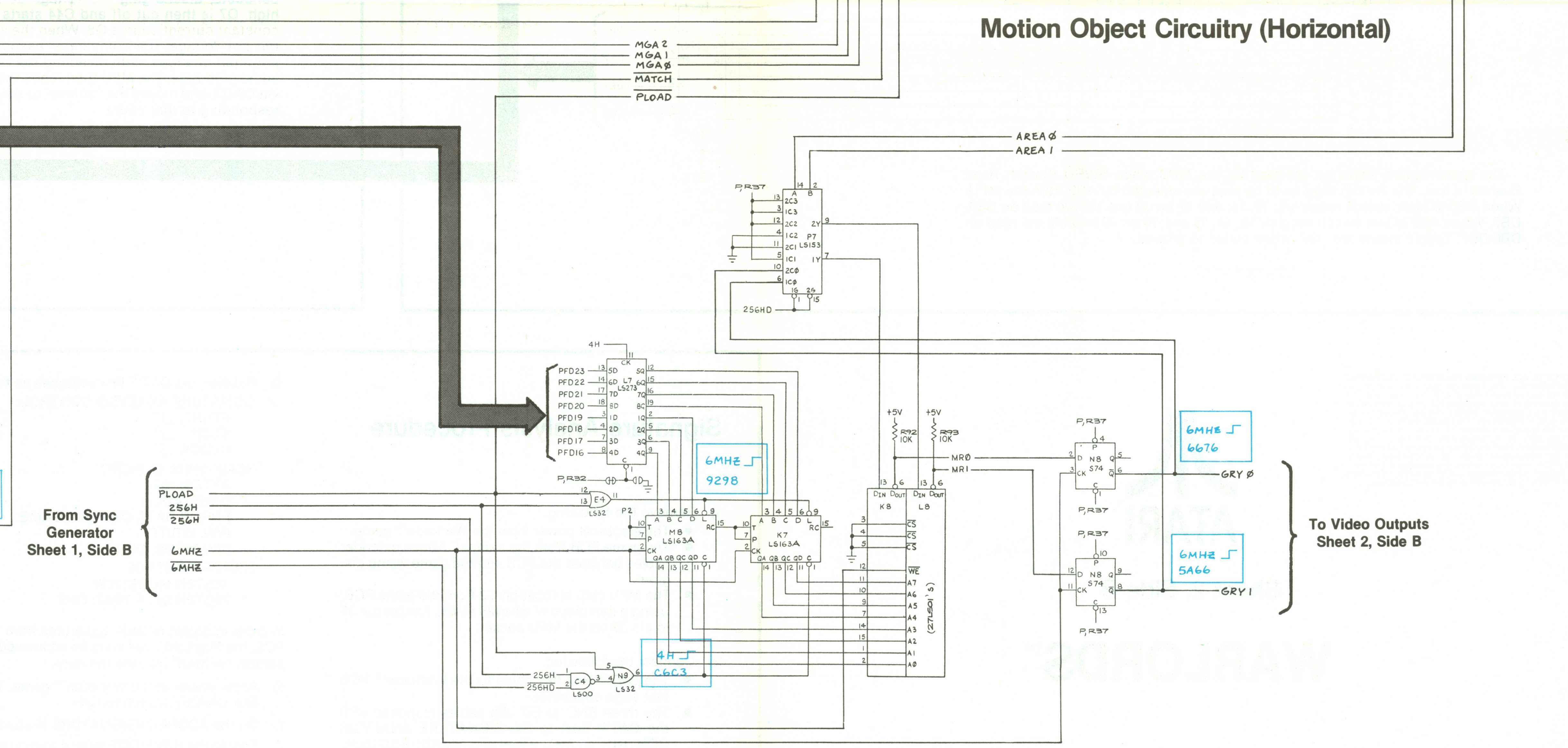
Motion Object Circuitry (Vertical)



The Motion Object Circuitry (vertical) receives playfield data and vertical inputs from the sync generator circuitry to generate the vertical component of the motion object video. PFD8-15 from the playfield memory and 1V-128V from the sync generator are compared at E5 and F5. The output is gated by C5 when a motion object is on one of the eight vertical lines and is latched by D5 to AND gate C7. A low on C7 pin 6 indicates the presence of a motion object on one of the vertical lines during non-active video time. This signal (MATCH) enables the multiplexers in the picture data circuitry.

When 256H on pin 1 of C6 goes high, the sync generator inputs (1V, 2V and 4V) are selected. When 256H goes low, the latched output of D5 is selected. The output of C6 is EXCLUSIVE OR gated at D6 and is sent to the picture data selector circuitry as motion graphic address (MGA0-MGA2). The other input to EXCLUSIVE OR gate D7 is PIC7 from the playfield code multiplexer circuitry. PIC7 when high causes the output of D7 to be complimented. If MGA0 is high, MGA1 is low and MGA2 is high, a high at PIC7 causes MGA1 to be high and MGA2 to be low. This causes the motion object video to be inverted top to bottom.

Motion Object Circuitry (Horizontal)



The motion oject circuitry (horizontal) receives playfield data and horizontal inputs from the sync generator circuitry. PFD16-PFD23 from the playfield memory determines the horizontal position of the motion object. This data is latched by L7 and loaded into the horizontal position counters K7 and M8 by a low on pin 9 of K7 and M8. The horizontal position counters then address video RAMs K8 and L8. These RAMs are loaded with the video data for the particular motion object from shift registers D7 and J8 (which were loaded from the graphics ROM). The output for RAMs K8 and L8 is then sent to the color PROM circuitry as MR0 and MR1.

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