ON TARGET

TECHNICAL NEWSLETTER VOLUME 5, ISSUE 1 JAN./FEB. 1984 MYLSTAR ELECTRONICS, INC.

M.A.C.H. 3 TROUBLESHOOTING (CONT.)

INTRODUCTION

The newly developed Video Disc system in games required manufacturers to develop new technologies to utilize these systems. Mylstar Electronics, Inc. created a fully interactive game system using the video disc player for the background images, and overlaid computer generated graphics on top. This game system was created by our Engineering Department by modifying our GG-III game computer board, and incorporating two new P.C. Boards.

This issue of our On-Target Newsletter will focus on one of the new boards, the A2 Interface Board. The purpose and function of this board will be outlined, to give a background understanding of why and how it works. The second part will concentrate on troubleshooting the board through circuit descriptions and signal tracing.

The Interface Board's function is to create a medium in which the two systems can communicate. The game graphics computer uses the data bus and 5 strobes to communicate with the Interface Board. The information going to and from the video disc player is in four different signal formats. The Interface Board will operate on three of those signal formats; the 11 bit coded Command Control signals going into the video disc player, the 24 bit Phillips Frame Number code from the composite video signal, and the digitally encoded Audio Track 2/R from the video disc.

Located on the A1 CPU Board, one of the Input Ports is a 20 pin DIP socket which carries the Data Bus to the Interface Board. This socket carries three Input Port Select Functions, $\overline{IP5}$, $\overline{IP6}$, and $\overline{IP7}$, and three Output Port Select Functions, $\overline{OP1}$, $\overline{OP6}$, and $\overline{OP7}$. These read and write control lines will be used by the CPU to latch data to and from the Interface Board. This data is used when the CPU needs to send commands to the video disc player, or receive information from it.

FRAME NUMBER DECODER

In order to properly start a game and place the jet fighter and targets on the screen, the CPU must know what frame is being displayed on the screen. Encoded on every frame in a CAV (standard play) disc is a frame number, from 1 to 54000, which is inserted into the vertical blanking period of every odd field of each frame. This frame number is stripped from the composite video signal on the Color/Sync Board and is received at the Interface Board via J3.

The 24 bit bi-phased Frame Signal is inverted by one gate of A2 (a Schmitt trigger inverter). The signal is sent to C29, R30, and another gate of A2 for positive edge detection, which is inverted once for negative voltage spikes, and also is sent to another positive edge detector (C30, R31, and a third gate of A2), which is inverted twice for positive voltage spikes. The positive and negative voltage spikes are summed by A4 (a two-input NAND gate) so that B4 (a non-retriggerable monostable multivibrator) can produce a clock pulse (FCLK) for the serial to parallel shift registers. The positive and negative voltage spikes are

inverted by A3 and summed with the clock pulse to produce Set and Reset pulses for the D-type Flip Flop (B3). This will produce a serial data train representing the Frame Number.

The serial Frame Number (FDATA) is then shifted into three serial-to-parallel shift registers, B1, G1, and H1, by the FCLK signal. Within the Frame code we have to represent numbers from 1 to 54000, one for each video frame. One binary coded digit (BCD) can be represented by four binary bits, so the five digits of number 54000 will be represented by 20 bits. The high order four bits of the 24 bit Frame Number code are all ones, which will be shifted into the high orders four bits of the most significant shift register (B1) and generate the Valid Frame Number latching pulse. The dual four-input NAND gate (E1) is configured to detect the four high bits and generate a clocking pulse that latches the Frame Number into the 8 bit latches B2, G2, and H2. The game machine CPU will strobe the input port functions $\overline{IP5}$, $\overline{IP6}$, and $\overline{IP7}$ to read the Frame Number onto the data bus.

AUDIO TRACK DECODER

The video disc has not only composite video information stored on the disc, but also contains two separate discrete audio channels. One channel contains pure sound, such as the jet noise and voice, which is routed directly to the A6 Sound Board for pre-amplification.

The other channel contains a digitally encoded audio frequency, which carries target information relating to the game play and proper placement of targets, and the horizon.

During active play time of the disc, the Audio Track 2/R will be continuously transferring serial digital data to the Audio Track Decoder section at a 5 KHz rate. Approximately every one and a half seconds the Interface Board will have received a 1K block of digital information which will then be transferred to the game machine CPU.

The digital data coming from the audio track is encoded in an audio frequency, rising and falling across the zero volt level at its own clock rate. The audio track must be decoded to determine the clock rate and to detect transitions through ground to generate positive pulses.

The Audio Track 2/R is a 1 volt peak-to-peak signal which comes into J6. The audio signal is first sent to a amplifier (R46, R47, R48 and Q3) through C78 to give a better signal-to-noise ratio. The 5 volt peak-to-peak signal passes through a DC clamping circuit (C79, D1, and D2), a biasing network (R10 and R11), a low pass filter (R36 and C10), and on to the zero crossing detector (X4). The IC X4 is a dual voltage comparator that has been configured to be a zero crossing detector. Both outputs of the zero crossing detector are tied to a two input AND gate (S4) which will produce a pulse train at pin 8 that is high when the input wave passes through a 100 mV window around ground. This signal is sent to E3, M5, and V5, so that the data clock and break in transmission signals can be formed.

The output is also connected to a data detector consisting of A4 and S2. This circuit determines whether an edge is detected between clock pulses, indicating that a logic "1" was received at the zero crossing detector. When that occurs, the data detector generates a high pulse to be clocked into a serial to parallel converter (K1) via the clock from the clock generator (M5).

As the parallel data is received it is sent to a bus transceiver (M1) and to a Buffer Starts Detector, (N3 and N2) which will detect the buffer sync byte, 67, the first byte in the 1K block of data. A high pulse is produced at N2, pin 2, when the buffer sync byte is detected. This high pulse is inverted by the NAND gate (S3) and clears the Buffer Ready Flag D flip flop (V4) and the RAM address counters (V1, V2, and V3) through the AND gate (S4). The audio track data clock will begin clocking the Module 8 Counter (V4 and N4) which will generate the RCLOCK function every eight data bits. The RCLOCK function is multiplexed through the RCLOCK MUX (S3) to generate the clocking pulses for the RAM address counters. The RAM address counters

then sequentially address the Buffer RAM (S1) to store the 1K block of data from the audio track for the game machine's later use.

The CPU machine, as mentioned earlier, has several input and output port select lines connected to the Interface Board to control certain portions of the board. To access the Audio Track Decoder section the game machine CPU will use the $\overline{OP6}$ and $\overline{OP7}$ functions in conjunction with the D0 bit to create two latching functions, STB1 and STB2, (B3 and E3). The function STB1 is used to read the Status Register (E2) to report to the CPU the condition of certain portions of the interface circuitry.

One of the status functions read by the game machine is the Buffer Ready Flag (V4), which is pulled high when the most significant bit of the RAM address counters goes high. This indicates that the Buffer RAM (S1) has been filled with the 1K block of data. The game machine then pulls the D0 bit low as it strobes the $\overline{OP6}$ function for the B3 flip flop to change output states. The Q output of B3 is OR'd with $\overline{IP7}$ strobe to produce STB2.

The RCLOCK MUX circuitry is made of 3 two-input NAND gates configured so that if the Buffer Ready Flag is low, then the RCLOCK function will be used to determine the clocking rate for the RAM address counters. When the Buffer Ready Flag goes high, it enables the game machine to set the clocking rate with the STB2 function through the RCLOCK MUX. The STB2 signal is sent to a Schmitt trigger inverter (A2), and to a monostable multivibrator (B4) for glitch-free pulse shaping of the signal to match the data transfer rate of the game machine CPU. This pulse shaped signal (MSTB2) will now sequentially increment the RAM address counters, while the STB2 function will read the data on to the Data Bus through the eight bit buffer (K2).

COMMAND CONTROLLER

The Command Controller section of the A2 Interface Board creates the means by which the game machine sends instructions to the video disc player. The video disc player has 26 functions, such as freeze frame, fast forward, search to frame, play, reverse, etc., that can be controlled from an infra-red generating remote control unit, or from an External Control input port at the rear of the player. The External Control port is a serial, two wire, interface input that disables the remote control receiver when connected.

The Command Controller section, therefore, is a serial interface encoder and transmitter. It not only converts the parallel, 8 bit, command from the game machine CPU to a serial format, but must also generate the protocol necessary for the control section to communicate with the video disc player. The correct protocol consists of a series of bursts of a carrier frequency, with the bursts separated by a specific length of time that determines whether a "0" or a "1" is being transmitted.

Any of the 26 commands can be encoded using a serial 11 bit pulse code modulation (PCM) scheme. The PCM scheme means to modulate the time between the bursts to indicate the "0" or "1" status of the bit within the code. Each pulse burst consists of 10 pulses of the 38 KHz carrier frequency and is approximately 0.263 milliseconds long. The elapse time between bursts, termed the Bit Period, is either 1.05 milliseconds to indicate a logic "0" or 2.10 milliseconds to indicate a logic "1".

The game machine CPU will initiate a command transfer through another output port function, $\overline{OP7}$. The $\overline{OP7}$ function latches the CPU's command from the data bus into a parallel-to-serial shift register (M2) and also resets the Start Transmission Flag (W2). The Start Transmission Flag enables the counter chain made up of X2, W1, and X1 and the burst clock (X3) a LM555 timer. The LM555 timer produces a 38 KHz clock signal to the counter chain when pin 4 is high. The clock can be calibrated with the Self-Test mode or by moving jumper JP14 from normal to test and adjusting R22 until the period of the signal at pin 3 is 26 usec.

One half of W2, a D-type flip flop, generates the Start Transmission Flag while the other half is used to gate the 38 KHz bursts to the output.

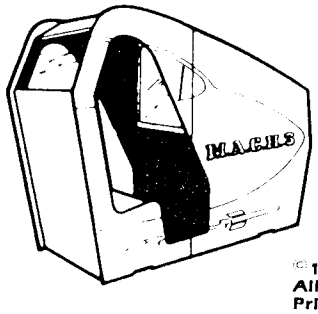
A presettable decade counter (X2) is used as a Burst Counter which strobes W2 to gate 10 clock cycles to the output. W1 is a data-to-period counter which receives the serial data output from the parallel-to-serial shift register, (M2). If the data from M2 pin 9 is a logical high the W1 is preset with an 8 which produces an approximately 2.1 msec period. If the data is a logical low, the W1 is preset with a binary 4 that produces an approximately 1.05 msec output period. The I.C. X1 is a Bit Counter which counts 11 bits and then disables the Start Transmission flip flop and sets the End Of Transmission Flag. When the End Of Transmission Flag is high the game machine CPU will read it through the Status Register (E2) to allow the CPU to send another command if it needs to.

CONCLUSION

The proper operation of the game system is the normal condition under which these circuit descriptions apply. Of course, a defective Interface Board will halt proper game operation, possibly even prevent initialization. The use of the Self Test mode in the game, will aid the technician in troubleshooting. When entering any specific test in the Video Test section of the Self Test mode the game machine CPU will begin to send commands to the Command Controller section and look for responses from the Status Register. This will allow a technician to check the Command Controller section. Until a specific test is begun the game machine will stay in a wait state, so by pressing the "Play" button on the front panel of the video disc player, the disc will spin up and output its signals to the Interface and Color/Sync Boards. A technician can now check the input and initial decoding of the Frame Number and Audio Track Decoder sections.

M.A.C.H. 3

MILITARY AIR COMMAND HUNTER



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