4. RAMCHECK OPERATION

This section outlines the operation of RAMCHECK. It instructs you on how to handle the socket, and describes the RAMCHECK tests in some detail. We strongly recommend that you read at least this section before putting the manual away. Please note that actual screen displays may vary as RAMCHECK's firmware is modified.

4.1 INSERTION AND REMOVAL OF MODULES

INSERTION:

Make sure the Module Power **red** LED is off (if not - press ESC). RAMCHECK uses a vertically mounted high-quality test socket with two ejectors that need to be opened prior to insertion. Carefully insert the DIMM into the socket, pushing it evenly along its top. When the DIMM is properly inserted, the ejectors will snap onto the semi-circular notches on each side of the module.

REMOVAL:

Make sure that the Module Power **red** LED is off (if not - press ESC). In certain modules, the **red** LED may still be glowing slightly, even when the tester is in Standby Mode; if this occurs, it is still safe to remove the module from the socket (only in Standby Mode), as the module is allowing only a minor amount of leakage current to flow. This however, should not be interpreted as an indication of a defective device.

Place one finger on top of the DIMM module to **prevent the module from popping upward** and simultaneously pull both ejectors sideways.

NOTE: The socket used is of the best available quality. It is rated for 10,000 to 30,000 cycles of removal and insertion. Using it carefully will provide you with a long period of use. In particular, do not subject it to humidity and always follow the above instructions for smooth handling.



1. Do not insert or remove a module when the Module Power <u>red</u> LED is on! (Press ESC to turn it off prior to insertion/removal.)

2. Never use excessive force to insert a DIMM module. If a module is not sliding in smoothly - please review the instructions on this page.

4.2 MEMORY TYPES AND TEST CATEGORIES

4.2.1 SDRAM AND EDO/FPM MEMORY TYPES

SDRAM technology is radically different than STANDARD EDO/FPM DRAM technology as it offers significant advantages and has become widely used.

The RAMCHECK overall test flow for SDRAM memory types is similar to the test flow for EDO/FPM memory types.

4.2.2 TEST CATEGORIES

RAMCHECK tests are composed of a variety of routines. They are generally divided into two categories:

- 1. Within-Specification tests.
- 2. Out-of-Specification tests.

The first group of tests is done with the module operating within the manufacturer's specifications and conventional safety margins. Detected errors are therefore indicative of a definite chip malfunction and the test is terminated with an error message (and an audible signal).

The second category of tests makes use of comparative tests during which the module is operating outside its normal specifications. This type of test gives some indication of the module's behavior under varying conditions, for example, relative cell storage leakage at various temperatures, or at Outof-Specification voltage spikes. These tests, called Relative Refresh and Relative Voltage Spikes, provide you with comparative figures, not with absolute Engineering Units. For example: a refresh figure "5", is indicating a "better" refresh performance than "4". No error messages are given by this type of test, because the module is working outside its specifications. However, the comparative figures, combined with common sense, can help detect some unique problems. For example: let's assume that we suspect a module to be defective, yet it passes all the Within-Specification tests. During the Out-of-Specification test phase we notice that the comparative refresh figure is much lower than normally seen on other modules. This leads to suspicion of a potential intermittent refresh problem.

The Out-of-Specification tests are part of the EXTENSIVE test

described later in this section. <u>Notice that under no condition</u> is the module operated outside its absolute maximum ratings.

4.3 TEST PHASES

The main tests of RAMCHECK, the BASIC test, the EXTENSIVE test, and the AUTO-LOOP are MULTI-BYTE tests where all bits are checked simultaneously.

RAMCHECK starts with the BASIC test, which lasts, between 3 and 30 seconds, depending on module size. The EXTENSIVE test automatically follows the BASIC test and it lasts several minutes. It includes different voltage and temperature related test procedures, as well as mode analysis. The AUTO-LOOP test proceeds in an endless loop of varying pattern (and algorithm) tests.

The following sub-sections describe each of the default main test phases: BASIC, EXTENSIVE, AUTO-LOOP.

Section 5 describes the RAMCHECK SETUP mode, which allows you to perform advanced tests in which you setup your own parameters and testflow.



4.3.1 STANDBY MODE

RAMCHECK's starting screen begins in the STANDBY mode where you are prompted with the following message to insert a module and start the test:

Î		Î
F 1 9	START BASIC TEST	
F4 l	<u>/IEW_TEST_LOG/SE⁻</u>	ΓUΡ

NOTE: Do not have a module inserted in the socket upon initial turn on, as this may load certain signals that are necessary when RAMCHECK performs its initial locking functions internally.

During STANDBY MODE, no devices are being tested, and RAMCHECK internally tries to reduce its own power consumption.

From this mode, you may select the following actions:

- F1 starts the automatic test as described in the following sections.
- **F2** allows you access to all of RAMCHECK's advanced setup functions, which are described in Section 5.
- **F3** run the DEMO program.
- F4 -allows you to view the Test Log or to view any modified setup of RAMCHECK.

The **Test Log** is a unique feature of RAMCHECK. It is actually a scrollable list of all the results obtained during the last test. The information in the Test Log is retained until you perform a new test.

F5 -is used by our technical personnel to run RAMCHECK's extensive diagnostic programs.



4.3.2 BASIC TEST



The initial group of tests determines module size, mode type, SDRAM frequency rate (or speed/cycle time for EDO/FPM), and looks for basic wiring, addressing, and defective bit problems.

BASIC T	EST CCC	CCCCC	BASIC		5555555
BYTES: B	1 		BYTES:B		
00:01.2	133MHz	UBFR	00:03.9	63/150)ns ጚ
32M×64	SDRAM	B1/0	16M×72	FPM	B2/1

Note that RAMCHECK will automatically recognize and test a DIMM, regardless if it is an SDRAM device, or an EDO/FPM device. For SDRAM DIMMs, the speed is displayed in the form of the module's fastest functional frequency rate, and size is displayed in specific JEDEC notation; the speed for EDO/FPM modules is displayed as the fastest functional access time from RAS, in nanoseconds.

RAMCHECK performs numerous timing tests at the start of the BASIC test in order to determine the frequency of the SDRAM module. Please refer to APPENDIX D to further explain RAMCHECK's speed determination process.

RAMCHECK OWNER'S MANUAL



The frequency list is subject to change with firmware development.

Once the frequency is determined, RAMCHECK will commence to test the entire memory module at the selected frequency. If a problem is encountered, RAMCHECK will automatically reduce the frequency (in the order of 184MHz, 166MHz, 150MHz, 133MHz, 125MHz, 112MHz, 100MHz, 83MHz, 75MHz, and 66MHz), unless you have setup RAMCHECK to test at a fixed frequency by either Setup or the Change-on-the-fly feature.

During the BASIC test, the screen will inform you of the voltage used to test the module, and display a constant change of patterns used to test it. As we use complex test patterns, only the first pattern is shown. There are two LEDs next to the display on RAMCHECK. You will note that the MODULE POWER LED indicator will glow when a module is being tested, additionally, when testing SDRAM devices, you may see the Page Burst LED flash as memory patterns are bursted into the device at real clock rates.

After passing the BASIC test, RAMCHECK will display a message indicating a successful test, plus additional information on whether the module is a 2 or 4 clock device.

The BASIC TEST OK message is followed by a series of summary screens detailing speed and structure information. Please keep in mind that all speed and structure information is automatically recorded into the Test Log, which is accessible by pressing F4 from standby after the test. The information is retained in the Test Log until a new test is initiated.

Please note that if you want to reach the summary screens quickly, even before the end of the Basic Test, simply abort the test by pressing F5 during the Basic Test.

8M×64`S SPEED: TEST=PC-100 PAGE BURST=100P SPD=INTEL PC-10	100MHz
TEST=PC-100	
PAGE BURST=100	1HZ
SPD=INTEL PC-10)0

The determination of the PC-100 or PC-133 compliance appears on the second line of the screen, and it has the header "TEST=" followed by "PC-100" if RAMCHECK determines that the module is PC-100, or "PC-133" if the module is determined to be PC-133. The third line indicates "PAGE BURST=xxMHz"; it indicates the maximum frequency page burst of the tested module. The fourth line in this example indicates "SPD=INTEL PC-100", which indicates that the data in the SPD claims the module to be a PC-100. More examples are shown in APPENDIX C. If RAMCHECK determines that the module is PC-66, the message "TEST=PC-66" will appear. If a module's SPD is marked for PC-66 while the module timing parameters are measured within the PC-100 range, you will see the message "TEST=PC-100 RANGE". Similarly, if the module exhibits characteristics that place it in the range of being PC-133, RAMCHECK will report "TEST=PC-133 RANGE".

IMPORTANT NOTE: The BASIC Test is the only test used by RAMCHECK to determine PC-100 or PC-133 compliance. It provides an information summary that gives specific information if the module is compliant with the PC-100 or PC-133 standard.

Other frequencies are used throughout the Extensive Test to create additional conditions for the test. Therefore, if a module finishes BASIC Test as PC-133, the fact that it may run at 100MHz during Extensive Test or AUTO LOOP does not mean that the module is not a PC-133.

The first speed summary screen is followed by the Tac measurement screen as in the following examples:

8Mx64`S_SPEED:	4Mx72`S SPEED:
Tac_(CL=3): 8.5nS	Tac (CL=3): 5.0nS
Tac (CL=2): 8.0nS	Tac (CL=2): 5.0nS
83MHz (PC-66)	Tac RANGE: <pc-133></pc-133>

The screen shows the measurements of Tac (access time from clock) for CAS latency 2 and 3. Please refer to APPENDIX C for further details about these important measurements.

Following this screen will be the module's explicit structure information.

16M×64`S_S	TRUCTURE:
	-5:0+1+2+3
ILBER SIZES	4×2M×8
SDRAM 168P	UNBUFFERED

The above example shows the size of the module, its type, number of the module's banks (not to be mistaken by the individual SDRAM banks), the use of the -S control lines, and the size of the individual chips used in the module. The above example shows an unbuffered 16Mx64 SDRAM module with two banks, using control lines S0, S1, S2, and S3, and employing 4x2Mx8 chips.

The size of each individual chip of the module is shown in the

format of [number of banks] x [each chip bank's size in Meg] x [bus width in bits]. The following examples show some typical chip sizes:

2x1Mx8 - a 16Mbit chip with overall size of 2Mx8; 4x2Mx8 - a 64Mbit chips with overall size of 8Mx8; 4x4Mx4 - a 64Mbit chip with overall size of 16Mx4; 2x2Mx4 - a 16Mbit chip with overall size of 4Mx4; 4x1Mx16 - a 64Mbit chip with overall size of 4Mx16; 4x8Mx8 - a 256Mbit chip with an overall size of 32Mx8; 4x16Mx4- a 256Mbit chip with an overall size of 64Mx4;

Some devices utilize various wiring or addressing variations of the original JEDEC standard. This variation is legitimate on specific motherboards, but may result in failure in other motherboards that do not support this variation. If RAMCHECK encounters such a legitimate variation, it will flash a short warning message as in the following screen:

DEVICE	TYPE	WA	RNIN	G:
ASYMMET	FR IC	4K	REFR	ESH
12 ROWS	5 10	Col	UMNS	

But it will not stop the test, as this module will work perfectly in all motherboards that support the 4K-refresh feature.

During the BASIC test, the graphic display shows animation depicting the progress of the test, a test timer, module type and size. The shortened notation 44/100nS for EDO/FPM devices indicates the module as having an access time of 44nS and a cycle time of 100nS (Please refer to APPENDIX D for an explanation of cycle time measurement).

BASIC 1	EST	AAAAA	AAA
BYTES:		******	68
00:01.8	44/	100nS _	. <u>S</u>
8M×64	EDO	<u> </u>	1/0

You will also note the ' 3_V ' voltage indicator next to the access and cycle time. The ' 3_V ' or the ' 5_V ' marks indicate that the DUT is being tested as a 3.3V or a 5V device. The animation characters show the DUT at bit or bytes resolution. For example, the above screen shows a x64 device, which requires 8 animation characters representing 8 bytes of memory. Similarly, a x40 module will require 5 byte-animation characters, while a x72 requires eight. The screen also displays the HEX code of the current test pattern used on the top right corner. If the module passes the BASIC test, a few summary screens will follow to provide additional information on the module tested, including a translation of the JEDEC notation to the module size in whole.



If a problem is detected, the test is halted with the corresponding error message. If no initial problem is detected, the test continues with every cell being written to and read from several times with different basic bit patterns.

In case of data bits error, the test halts and the defective bits are indicated as in the following message:

BANK 1:	DATA		
🚰 B1 🗸			
- <u>488</u>			
16MX72	67/15	ons	FPM

Pressing the \leftarrow or \rightarrow keys allows you to examine the memory array two bytes at a time. In the above example, Bytes 7 and 8 are currently selected, and the corresponding 8 bits per byte are displayed on the next line. Pressing \checkmark allows you to move down one line to examine each defective bit. The display at the bottom will then change to identify the data line corresponding to the selected bit and its pin number as indicated below:



This example indicates that Byte 1 and Byte 2 are selected. Bit 7 of Byte 1 is being examined by the user as being DQ6 and being located on pin 24 of the module. Pressing \uparrow allows you to move up one line and subsequently select to view the remaining bytes.

By pressing \checkmark a few times, you can scroll down through more error information as discussed in Section 3.5.6. These include error address information, actual write/read pattern information, and more details about the test function type which caused the error to result:





Refer to section 3.5 for additional information regarding menus.

Many other types of errors may be detected by RAMCHECK.

The following screen shows an Address Column error in address line A0 (pin 12) of Bank 1, Group 1.



We use Group1 or Group2 to describe how the memory device data bus is mapped onto RAMCHECK's internal 32-bit bus. Memory devices with 32 bits or less are directly mapped to Group1. Memory devices with 33 to 40 bits are mapped to Group1 and Group2. In Group2, bits 33 to 40 are mapped to the most significant byte.

In the example, the '00000004' hex code indicates that the above address error occurred only in the third bit of group 1.



The Unequal Sizes error message appears when different banks or different data bit groups of the same DUT exhibit different sizes, as shown in the following screens:

UNEQUAL SIZES: F1CONTINUE GB1-GROUP1: 1M MESSAGE 10 OF 14	END <mark>Est</mark> →
UNEQUAL SIZES: F1CONTINUE +B2-group2: 8M Message 8 of 4	END Est ⊋

The first screen shows that Bank1-Group1 has 1M, while the second screen shows that Bank2-Group2 has 8M.

All the errors are also recorded in the Test Log, which can be viewed by pressing F4 from the STANDBY mode. The following partial sequence of two screens shows how the Test Log indicates an inconsistency in the Mode type of the various groups:



MODE: FPM	Ť
IN B1-GROUP2:	8
MODE: NIBBLE	
IN B2-GROUP2:	+

The first screen indicates the device to be FPM (Fast Page Mode) while the second screen shows that in Bank1-Group2 the mode was NIBBLE instead of FPM.

Detailed Structure Information:

RAMCHECK provides explicit information on the module's structure, after a successful BASIC test. Such information is illustrated below:

16Mx64`S STRUCTURE:	1Mx64`S STRUCTURE:
BANKS:2 -S:0+1+2+3	BANKS:1 RAS:0+2
CHIP SIZE: 4×2M×8	CAS:0+1+2+3+4+5+6+7
SDRAM 168P UNBUFFERED	168P DIMM BUFFERED

The left screen above shows the structure of the tested module as being an unbuffered SDRAM, having 2 Banks, 4 -S control lines, and using chips that are architectured as 4x2Mx8. The right screen shows structure information for a typical EDO buffered DIMM module, having 1 Bank, 2 –RAS control lines and 8 –CAS control lines.

RAMCHECK also provides information on the PRD and SPD settings and tells if the module is ECC type, PC133, PC100, or PC66.

SPD MANAGEMENT

Most SDRAM modules employ an SPD device. The final structure screen allows you to view the SPD as follows:

16Mx72`S 9	STRUC	STURE	
SPD=INTEL	PC-:	100	
16M×72`S S SPD=INTEL TO ACCESS ECC=Y	IHE	SPU	= 65

SDRAM modules without an SPD will show a 'MISSING SPD!' message. Choosing to view the SPD will stop the test and allow you to review its information, otherwise, the test procedure will continue with the Extensive Test.

NOTE: Please refer to Section 4.4 for detailed SPD Management information on viewing, saving, editing and programming the



You can also activate this screen by pressing F5 during the BASIC test. 256-byte SPD information.

As the test program continues to develop, RAMCHECK will display additional information on SPD. The test log will reflect this by displaying SPD = xx for various characteristics, where xx is the programmed status of the device (i.e. SPD=INTEL PC-100). *This information is provided as a form of translation for the SPD, and is NOT obtained as a result of a measurement of the memory device*. Actual measurements such as access time, number of banks used, or CAS latency will be displayed without the "SPD =" indicator.

As seen above, RAMCHECK will indicate if the SPD device is programmed to show module compliance with the Intel PC-66, PC-100, or PC-133. This indication does not qualify the module for the Intel structure, it is only meant as an indication of the SPD's program.

ON-THE-FLY PARAMETER CHANGES



You can change some test parameters on the fly using our "one time" override feature. Simply press F2 during the BASIC TEST to access this function, then make the necessary selection. Because this is a "one time" change, the next memory device tested will not be affected.

The above screen image reflects the override menu when testing SDRAM modules. EDO/FPM modules will not include the Page Burst selection (P. Burst above), and will display "SPEED" in place of frequency. The following sections describe each of the override selections.

"One Time" Speed Override:

When testing SDRAM modules, the speed override feature allows you to set a "one time" frequency override.

SPEED OVERR	IDE:
100MHz	
FIENTER	ABORTER
←100MHz	→

This kind of speed override is in effect only while the current



The BASIC test determines the fastest Access Time of the tested memory device as well as the cycle time of the module. See Section 5 for details about the more advanced Speed Setup, which remains in effect also after you turn your RAMCHECK off. module is tested. To set a "one time" speed override, press F2 as stated above during the BASIC test to reach the CHANGE-ON-THE-FLY screen, then press F1 to select SPEED.

Use the \leftarrow and \rightarrow keys to scroll through the available frequency rates.

When testing EDO/FPM modules, the speed override feature allows a "one time" change of nanosecond access time from RAS. Enter the speed override by pressing F2 during the Basic Test and select Speed.

SPEED 61nS	OVERRIDE	:
€1 RAS	ACCESS:	6 1 nS 🐶

Afterwards, use the \leftarrow or \rightarrow to position the cursor over the current speed and then press either the \uparrow or \checkmark keys to increase or decrease the value. Press F1 to enter your selected speed.

Thereafter, subsequent test phases will be conducted at the selected speed, as displayed on the screen with an "@" marker.

Please note that when modules are detected as being 3V devices, RAMCHECK will not alter the voltage even if it is changed-onthe-fly.



SDRAM modules cannot be set to 5V.

"One Time" Voltage Override:

To set a "one time" voltage override, press F2 during the BASIC test to reach the CHANGE-ON-THE-FLY screen, then select F2 for voltage. The following screen will be displayed:

TEST DUT AT 5V - Not for 3.3v ram!	÷
TEST DUT AT 3.3V 5V RAM FAIL OR SLOW	ŧ

You may use \uparrow or \checkmark to select the voltage setting that is to be used for this test, then press F1 to start the test at the selected value.

Please note that RAMCHECK can detect 3V devices, and therefore will not alter the voltage even if it is changed-on-the-fly.

"One Time" Refresh Override:

To set a "one time" Refresh Override, select F3 from the Change-On-The-Fly menu. Remember that longer refresh intervals create a slower refresh rate, and vice versa (refresh rate =1/refresh interval). To set this rate, use \leftarrow or \rightarrow to position the cursor, then use \uparrow or \checkmark to set the refresh value. Press F1 to enter your selected value.

"One Time" Page Burst Override:

When testing SDRAM modules, you may elect to turn off the Page Burst feature on RAMCHECK. To do so, select F4 from the Change-On-The-Fly menu. This will toggle the Page Burst function to OFF.

CHANGE-ON-THE-ELY:
F3 ŘĚFŘĚŠH F4 OFF

The Full-Page Burst function is used by RAMCHECK for rapid testing of SDRAM devices. Page burst support, however, varies among modules, as some will only include support for 1-bit, 2-bit, 4-bit, and 8-bit bursting. Not all SDRAM devices will include Page Burst support as it is not a requirement for compliance of the PC-133, PC-100, or PC-66 standards.

Next Phase:

- If an error is detected, the defective bit(s) are identified and you can use the various error menus to examine all the details of the error. Press ESC to return to STANDBY mode. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT.
- In the default RAMCHECK testflow, you cannot reach EXTENSIVE and AUTO-LOOP tests unless the BASIC TEST has been completed successfully.
- If you do not elect to terminate the test procedure after BASIC test, the following menu appears, prompting you to select the next test:





You can skip BASIC test to reach the EXTENSIVE test for a DUT that fails BASIC test. See Section 5. Press F1 to go to EXTENSIVE test, F2 to go to AUTO-LOOP. If 5 seconds pass with no user selection the EXTENSIVE test is initiated.

• As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT.

Significance of Successful BASIC Test:

The BASIC test provides module type and speed information. It verifies that all wiring on the module is sound and that all cells in the module are operative. It also confirms basic refresh capabilities.

It may not detect intermittent and/or pattern sensitivity problems due to its short execution time.

4.3.3 EXTENSIVE TEST

Ĩ∦∘F	EXTENSIVE TEST	
	<u>10000000000</u>	5. <u>- 7</u>

The EXTENSIVE test is an extremely comprehensive test! Module behavior is tested under varying voltage conditions, including numerous test functions, thereby achieving a remarkably high reliability level.

What is being tested:

- Voltage Cycling: Testing under all allowable voltage conditions. These include a range from 3.00V to 3.60V (or for 5V devices, a range of 4.50V to 5.50V).
- Mode Test: Testing the special DRAM mode of the DUT. DRAM technology uses two common modes: EDO and Fast Page mode. Mode failure does not halt the test, but the offending bits are shown with 'X' marks. Hard failure (which is not part of a specific mode), terminates the test with the familiar 'F' marks. Upon completing the mode test, the RAMCHECK test program will display explicit information, using the notation 'SDRAM' for Synchronous memory, 'EDO' for Extended Data Output Mode, 'FPM' for Fast Page mode, 'Nibble' for Nibble mode, and 'SCM' for Static Column mode. This test also provides a measurement



THE BASIC TEST IS SUFFICIENT FOR MOST SCREENING TESTS. Most defective modules will be detected during this test.





Pressing F1 during the EXTENSIVE test terminates the current step and proceeds to the next one (within the EXTENSIVE test).

of the Tcac parameter, or the access time from CAS, of the memory device. The value is displayed briefly during the test and is recorded in the test log.

Additionally, the MODE TEST provides information on SDRAM module burst lengths:

MODE TE	
CL=3 BL=	1+2+4+8+FULL
CL=2 BL=	1+2+4+8+FULL
4 M×6 4	<u>3.30V</u>

- Voltage Bounce: Testing data retention during voltage variation between read and write (e.g. write at 4.5V, read at 5.5V, or write at 3.6V and read at 3.0V and vice versa).
- March Up/Down: The march up/down algorithm is designed to reveal intricate problems caused by adjacent cell interference. In simplified terms, the test is done by first writing 0 to all memory locations, then, while scanning from first address to last address, the test verifies that a 0 remains in each location, then it is replaced with a 1. After the entire memory address is "marched up" in this fashion, the process reverses itself to perform the "march down" test. This time while scanning from the last address to the first address, the test verifies that a 1 remains in each location and then replaces it with a 0. RAMCHECK's new implementation of the March Up/Down algorithm is more advanced than our previous implementation in the original SIMCHECK, and it also incorporates several extra steps.
- **Relative Refresh/cell leakage:** This test provides a relative value for the ability of the memory chip to retain data between refresh cycles. "Relative" means that the result is not an absolute time value but a comparative one. Relative relation between values is exponential.
 - **For example:** A DUT with a relative value of "5" retained data integrity twice as long as one with a value of "4" without requiring refresh. Typical good values are 3 and higher. Since this test is of the Out-of-Specification type, lower results do not imply that a module is defective, as it can still work within its published specifications!
- Relative Voltage Spikes Performance: This test provides a relative value that indicates how well a module can sustain voltage spikes before a data loss occurs. Relative relations here are not exponential. Typical good values are 3 and above. Since this test is of the Out-of-Specification type,



Please refer to section 5.3.5 for information on Refresh Setup. lower results do not imply that a module is defective, as it can still work within its published specifications!

As you watch the red Module Power LED during the Relative Voltage Spikes test, you will see that it flashes vigorously. This LED is directly connected to the module's power supply. RAMCHECK creates artificial voltage spikes (of 5V to 1.5V or to 6.0V) after loading a complete test pattern. Memory devices with higher Relative Voltage Spikes figures can withstand more spikes in an actual application. Take into account that modules with larger built-in capacitors normally exhibit higher Relative Voltage Spikes figures due to the capacitors' smoothing effect on the spikes. Some complex modules, which utilize PAL chips and/or logic chips, may exhibit significantly lower Relative Voltage Spikes figures.

Note that ALL relative tests are absolutely safe, as RAMCHECK DOES NOT exceed any allowable voltage/current rating!

• Temperature stress test (Chip-Heat mode): In this phase, RAMCHECK tests memory chips at the actual higher operation temperature experienced inside a computer. Being able to test at the proper temperature is extremely important because some memory problems are not exhibited until the chip is warmed up. As the mode progresses, you will note that RAMCHECK will display the heating current in Ampere units.

CHIP-HER	AT MODE
1.040	
1.04A 00.14.1 32M×64	133MHZ 3.60V

The Chip-Heat mode utilizes a unique phenomenon, which was revealed in our research. When a DRAM chip is subjected to a unique waveform pattern, it is heated internally without the need of external heating techniques. Furthermore, this Chip-Heat method is absolutely safe, as we explicitly DO NOT use higher voltages or currents beyond the memory manufacturer's ratings.

The EXTENSIVE test display shows the current test type, duration of test, applied voltage, Access Time (speed in nanoseconds or frequency rate), and module mode type and size. The final test results look similar to those of the BASIC test. Note that because the DUT is tested at a higher temperature during the Chip-Heat portion of the EXTENSIVE test, the Access Time might be slower than the value obtained at the BASIC test.

Next Phase:

- If an error is detected during the EXTENSIVE test, the defective bit(s) are identified and the display waits for your acknowledgment. Press ESC after review to return to Standby Mode.
- If no errors are detected an OK test result is shown and you are prompted to continue. Press F1 to go to AUTO-LOOP or ESC to terminate the test. If the time delay passes with no user selection, the AUTO-LOOP test is initiated.
- As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

Significance of Successful Test:

The EXTENSIVE test verifies proper module operation under varying voltage conditions. It will detect intermittent problems which are either temperature dependent or resulting from adjacent cell interference. It provides comparative scores of module performance. It further tests the module with additional data patterns besides those utilized by the BASIC test.



4.3.4 AUTO-LOOP TEST



During the AUTO-LOOP test, the module is endlessly tested with different patterns of data bits, generated by different algorithms.

AUTO-LOOP TEST	AUTO-LOOP 33CC33CC
L00P#241	L00P#3980 B2/0
00:08:20.9 42/100n5 16Mx32 4.75V FPM	19:30:46.3 100MHz
16M×32 4.75V FPM	16Mx72 3.15V SDRAM

AUTO-LOOP is an excellent means for a burn-in procedure, as

it will continue indefinitely until the user presses the Esc key.



A necessary Calibration & Upgrade procedure is available from the factory. Refer to Appendix H for details. The time of the test, the iteration (loop) number, applied voltage, module speed and cycle time, module size, and mode type are displayed.

Some long tests like Self Refresh are incorporated into AUTO LOOP as shown in the following screen:

AUTO-LOOP	55555555
SELF REFRES	
19:17:37.5	100MHz
8Mx64 3.	45V SDRAM

Next Phase: The AUTO-LOOP test terminates when an error is detected or in response to the user's command.

- If an error is detected, the defective bit(s) are identified and the display waits for your acknowledgment.
- If no error is detected, the test will continue indefinitely; or until ESC is pressed to terminate the test.
- As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

Significance of a Successful Test:

AUTO-LOOP is designed to detect pattern sensitivity problems, as it tests the modules under many different patterns. 20 minutes or more are sufficient to detect most pattern sensitivity problems.

Notice that the AUTO-LOOP mode makes RAMCHECK an excellent instrument for continuous burn-in procedure.

4.4 SPD MANAGEMENT

SPD (Serial Presence Detect) is a small 8-pin EEPROM chip mounted on DIMMs & SO DIMMs that includes vital information about the module's parameters.

You can access the SPD Management Mode from Standby Mode

by pressing F4, F3. You can also enter this mode after the Basic Test has begun by pressing F5, F3, and F5. At the conclusion of the Basic Test, the final summary screen will give you the option to access the SPD Management Mode once again.

2M×72`S ST SPD=INTEL	PC-6	56	
TO ACCESS ECC=Y	THE	SPD	=F5

This example shows results obtained with an SDRAM DIMM. RAMCHECK indicates if the SPD device is programmed to show module compliance with the Intel PC-66, PC-100, or PC-133.

If you choose not to view the SPD, do nothing, and the test flow will continue as normal. Choosing to view the SPD of the device (by pressing F5) will terminate the test flow and display the SPD management screen.

SPD MANAGEMENT: E1 READ SPD
FIREAD SPD
F2 SHOW_BUFFER
F3 PROGRAM F4 VERIFY

RAMCHECK's SPD Management mode is the operational mode to read and program SPD data.

READ SPD

Press F1 to read the current module's SPD and keep this information in RAMCHECK's buffer. The SPD viewer displays information in a multipage list format. Use the \uparrow and \checkmark keys to scroll between the pages. The following screen images show a partial view of the SPD codes for a typical DIMM.

SPD VIEW Serial P Detect - 0-3:	RE 2	5 E N C	E YTE	5: 0B	↑
4-7: 8-11: 12-15: 16-19:	11 00	01 46 FF FF	40 12 FF FF	00 00 FF FF	↑ ₩
244-247 248-251 252-255	FF	FF FF FF	FF FF FF	FF FF FF	+

In the above examples, byte 0 contains "80", byte 1 contains "08", byte 5 contains "01", and byte 9 contains "46". You will

also note that bytes 244 through 255 contain "FF"; this is an indication that these bytes are not being used.

RAMCHECK's buffer will retain this SPD information until:

- a) new SPD data is read;
- b) an SPD file is downloaded from the PC Downloader;
 - c) your RAMCHECK is turned off.

SHOW BUFFER

Use SHOW BUFFER to view the current contents of RAMCHECK's buffer without reading the SPD of a module installed in the tester. This allows you to view the buffer after an SPD file download, or after reading the SPD of a module.

SPD EDITING AND FILING

When RAMCHECK communicates with the PC Program Software, you can further read SPD data into the PC, edit the data on your PC screen, save it into *.spd files on your PC, or download stored SPD files into RAMCHECK's buffer for programming other modules.

NOTE: When viewing information on the PC Screen, the SPD data, as well as the address locations, are displayed in hexadecimal format. When viewing the information on RAMCHECK's LCD display, the address locations are displayed in decimal format, while the SPD data values remain in hex.



SPD PROGRAMMING

SPD programming should only be done by manufacturers and individuals that are well familiar with SPD data; therefore we recommend that these features only be performed by advanced users, as programming a DIMM module's SPD with erroneous data will render the module inoperable!!!

Use **F3** to program the data in the buffer into the SPD on the inserted DIMM module. To avoid casual users from programming wrong SPD data, the default SPD setting in your RAMCHECK is to have SPD programming disabled:

PROGRAMMING DISABLED! USE SETUP-CONFIG-SPD

You may enable SPD programming from Standby Mode by entering the following key sequence:

F2 Enters Setup ModeF3 Enters CONFIG. MenuF4 MOREF3 SPD

A warning screen will appear indicating that this function is for advanced users only. After a small time delay, the SPD Programming menu appears (Press F1 if you wish to bypass this time delay in the future). Select the F2 key to enter Programming Mode,





Please refer to Section 5.5.6 for an explanation of Programming Modes.

Use the right arrow button to select the programming mode. Press F1 to enter your selection. Press the ESC key a few times to return to Standby Mode.

Remember that you must have a valid SPD file in the RAMCHECK buffer (use SHOW BUFFER to make sure) before you start programming. Press F3 from the SPD Management Mode Menu to program your SPD. RAMCHECK programs the SPD and verifies the data with an OK (or fail) message at the bottom of your screen:

```
PROGRAMMING...
(16-BYTE PAGE) ****
OK
```

VERIFY

The VERIFY function (F4) compares the actual SPD data on the inserted DIMM module with RAMCHECK's internal buffer. This will either indicate OK if the data matches, or FAIL if the data is different.

PRODUCTION MODE

The Production Mode is a special SPD programming setup whereby the SPD of the module being tested is programmed immediately following the test.

This setup is for advanced users only. Those wishing to setup the production mode may acquire further details from our Application Note listed in the Tech Support section of our website (www.innoventions.com).