9000A-010

DEMO/TRAINER

Instruction Manual

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INTRODUCTION 1-1.

The 9000A-010 Demo/Trainer is an 80286-based product that functions as a video terminal. When the 9100 keyboard and monitor are connected, the operator can type characters from the keyboard to the screen. Built-in tests demonstrate RUNUUT, breakpoint, and other UUT code-dependent functions of the 9100 series and the 80286 pod. Faults introduced from a set of fault switches can be detected using various 9100 series tests.

FEATURES 1-2.

Demo/Trainer features mentioned below are shown in Figure 1.

1. RS-232-C Connector

2. Video Connector

3. On (1) Off (0) switch

4. Power Connector: Accepts a standard three-prong power cord for 100, 120, 220, or 240V ac power.

5. Fuse: 100 or 120V ac uses 1.0A SLO BLO (110/120); 220 or 240V ac uses 0.5A SLO BLO (220/240). See Line Fuse Replacement.

6. Line Voltage Selector Card: Card orientation in the slot determines line voltage compatibility. See Line Voltage Selection.

7. Fault Switches: Six switch banks (SW1 through SW6) of eight segments each. For normal operation, all SW1 segments must be closed and all SW2 through SW6 segments must be set to OPEN. In any different configuration, each switch segment introduces a fault in the circuit.

8. Functional Test Switches: Four momentary push buttons connected to the Peripheral Interface Adapter. These switches control the function tests.

9. Status LEDs: The upper LED shows the number of the self-test in process. The lower LED shows either a cycling indication when code is running or a flashing “F” when a fault has been detected.

10. Keyboard Connector

11. RESET Switch: Aborts any current operation and starts the self-test cycle.

12. RUN/TEST Switch: controls the on-board microprocessor. Use RUN for normal operation, or use TEST when the pod is connected.

13. Pod Test Connector

14. Power Indicator LED

LINE FUSE REPLACEMENT 1-3.

The line fuse is located in the combined line cord receptacle/fuse holder located to the right of the power switch.

1. Push the power switch to off (0), and disconnect the power cord at the Demo/Trainer.

2. Slide the plastic fuse cover (labeled FUSE PULL) to the left.

3. Pull the lever over to raise the fuse out of the holder.

Fuse installation requires following the previous three steps in reverse. Make sure the proper fuse is installed:

- For 100 or 120V ac, use 1.0A SLO BLO (110/120)

- For 220 or 240V ac, use 0.5A SLO BLO (220/240)

LINE VOLTAGE SELECTION 1-4.

The Demo/Trainer can be operated with 100, 120, 220, or 240V ac ±10% (250V ac maximum) at 50 or 60 Hz ±5%. Any one of the four line voltages can be selected without disassembling the instrument.

Line voltage is determined by the position of the voltage selection card (see Figure 1). The card is recessed in the fuse holder assembly. With the fuse removed, the “100”, “120”, “220”, or “240” printed on the card can be viewed through a window in the fuse holder.

A different voltage setting can be selected by changing card orientation in the slot. Use the following procedure to change the voltage setting:

1. Set the power switch to off (0), and disconnect the power cord at the Demo/Trainer.

2. Slide the fuse cover to the left, and remove the fuse.

3. Using needlenose pliers, grip the upper card edge and pull straight out. If this action does not dislodge the card easily, use the pliers first to lever the card up from the side.

4. Rotate the card so that only the desired voltage setting will be visible in the fuse holder window.

5. In order, insert the card, replace the fuse, and connect the line power cord.

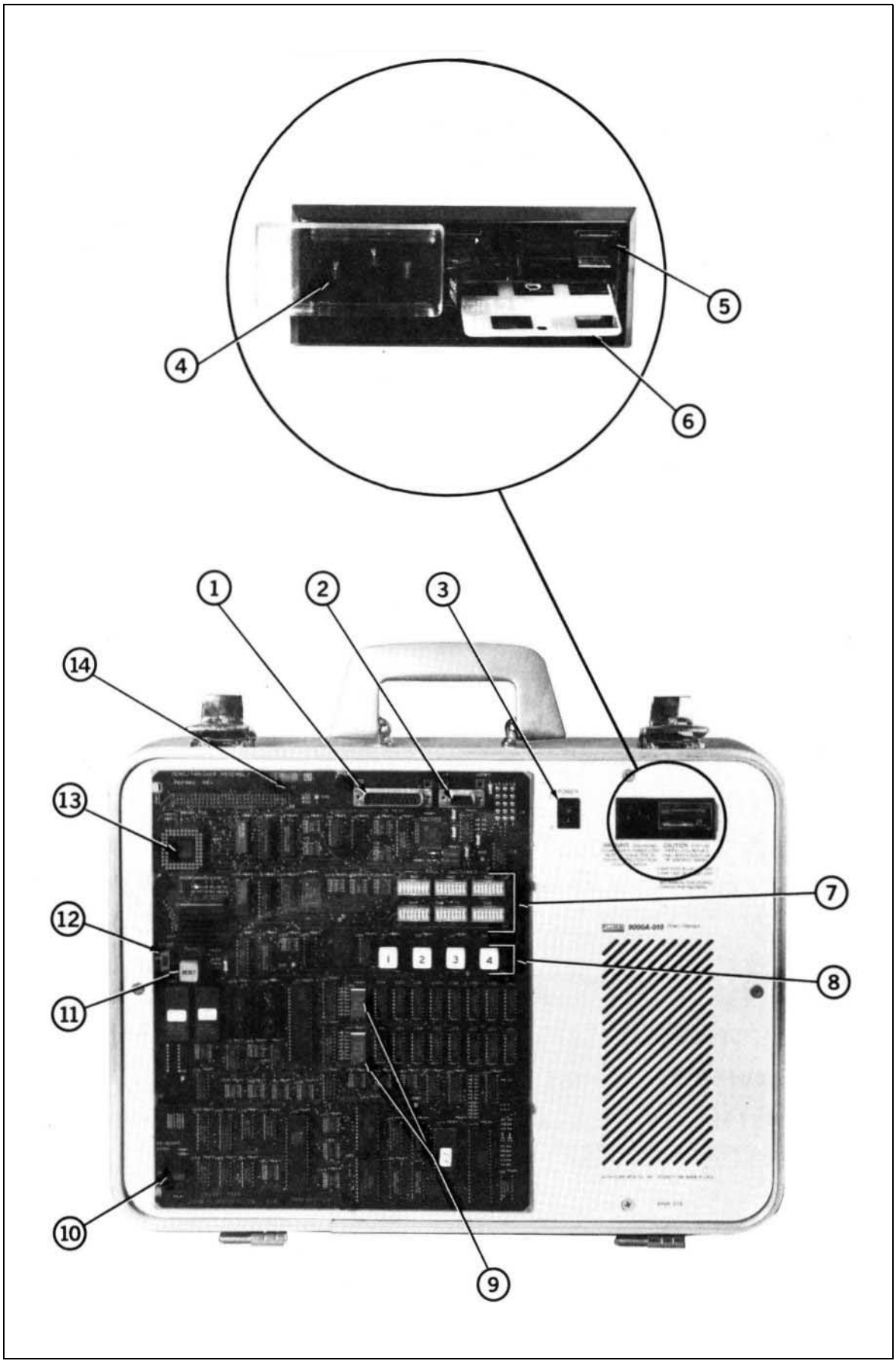


Figure 1. Features

SETUP 1-5.

The Demo/Trainer can be exercised independently (using a keyboard and monitor) or in conjunction with a 9100A and 80286 Pod.

Use with the 80286 Pod 1-6.

Use the following sequence when running the Demo/Trainer with the 9100 A and 80286 Pod:

1. With the Demo/Trainer power off (0), connect the Pod cable to J5 (labeled 13 in Figure 1).

2. Ensure that S5 (labeled 12 in Figure 1) is set to TEST.

CAUTION

With Pod operation, power must not be applied to the Demo/Trainer before it is applied to the connected 9100 and 80286 Pod. The Pod is protected through its energized protection circuitry.

3. Apply power to the 9100.

4. Now apply power to the Demo/Trainer.

5. On the 9100, press first the RUN UUT key, then the F2 key. Verify that the starting address (FFFF0) is displayed, then press the ENTER YES key. If an error is encountered, press RESET on the Demo/Trainer and repeat this step.

6. The 9100 display should now read “RUNUUT active” and the RUNUUT status light should be on.

Stand Alone Operation 1-7.

Use the following sequence when using the Demo/Trainer without the 80286 Pod:

1. If a keyboard and monitor are to be used, first ensure that power is off (0). Then connect the keyboard to J6 (labeled 10 in Figure 1) and the monitor to J3 (labeled 2).

2. Ensure that S5 (labeled 12 in Figure 1) is set to RUN.

3. Apply power (1).

DEMO/TRAINER OPERATION 2-1.

Built-In Self-Test Routines 2-2.

Demo/Trainer circuits are checked using the following five test routines:

Name	Number (Lower LED)
RAM Self-Test	1
ROM Self-Test	2
PIA Self-Test	3
UART Self-Test	4
Video Self-Test	5

The routines are sequenced through automatically at power-up or reset. Each routine can be run individually by exercising the Looping Test.

RS-232 and keyboard loop back are tested with a separate self-test program (see I/O Test).

Two LEDs indicate that the self-test routines are running. The upper LED identifies the test number. The lower LED displays a rotating pattern, signifying that the test is in progress. This pattern halts (blanks) during test selection (when Functional Test Switch 1 is pressed) and resumes with test initiation (when Functional Test Switch 4 is pressed).

NOTE

The rotating pattern in the lower LED demonstrates that the processor is running. Except during the Looping Test, it should be present at all times during stand-alone operation. When the 80286 pod is in control, this rotating pattern should be present during runuut.

A self-test failure is distinguished with a blinking “F” in LED B (lower) as the test number is displayed in LED A (upper). The blinking “F” indication continues for about five seconds, after which testing resumes.

RAM SELF-TEST (1) 2-3

The RAM test uses the same algorithm as the 9100. If major RAM problems are present, this test offers little help. The stack and variables stored in RAM would then be lost, resulting in a system crash.

ROM SELF-TEST (2) 2-4

This test compares a stored ROM signature (crc) with the signature calculated by the ROM self-test routine.

PIA SELF-TEST (3) 2-5

This test addresses the internal registers, verifying proper operation of the 8255 Peripheral Interface Adapter (PIA), and reads the ports to check for known values.

UART SELF-TEST (4) 2-6

The UART test addresses the internal UART registers and checks for known values. It also verifies that the UART registers can be changed. The test places the UART into self-test mode with an internal loop back and checks that both send and receive functions work properly.

The MAX232 driver chip can be tested using the I/O test (Functional Test Switch 2).

VIDEO SELF-TEST (5) 2-7

This test addresses the internal video registers and checks for known values. It also verifies that these registers can be changed.

Function Tests 2-8.

The Functional Test Switches (see Figure 1) provide an entry point for exercising the Demo/Trainer.

LOOPING TEST 2-9

The Looping Test allows for individual selection of the self-test routines previously described.

- Press Functional Test Switch 1 to activate test selection.
- For test 1 (RAM), press switch 4 to initiate the test, or
- For tests 2 through 5, press switch 1 again to select a test; each press scrolls to the next test. The tests are:

  2 ROM
  3 PIA
  4 UART
  5 Video

Press switch 4 to initiate the selected test.

The selected test continues to loop until the operator presses a new key. Errors are handled in the same manner as with the main self-test routine (failed test number in LED A and blinking F in LED B). No indication is made for a passing test.

I/O TEST 2-10

The I/O Test exercises the RS232 and keyboard ports.

NOTE

In order for the I/O test to pass, SW4-4, SW4-5, and SW6-4 must be in the ON (closed) position before the test is initiated. Set these switches to OFF (open) for normal operation or for use as a terminal.

Press switch 2 to initiate the test (upper LED displays “U”). The I/O Test checks both send and receive through U12 and U13.

TERMINAL MODE 2-11

In terminal mode, the Demo/Trainer emulates an ANSI-compatible subset of the VT100 commands. The arrow keys are mapped to be VT100-compatible. Commands implemented in terminal mode are described in Table 1. The keyboard must be attached to the keyboard connector before the operator initiates terminal mode. Use the following procedure when using Terminal Mode:

1. Press Function Test Switch 3 to initiate terminal mode.

   The setup screen appears. Field selections (with listed characteristics) include the following:

   Transmit/Receive Speed (300, 1200, 4800, or 9600)

   Operation (Line or Local)

   Parity (none, odd, or even)

   Data Bits (7 or 8)

   (50 or 60 Hz)

Table 1. Terminal Mode Commands

The Terminal Mode Commands described below use the following three notation conventions:

<xxx>	Means "press the xxx key". Example: <ESC> indicates the ESC key.
XXX	Means to type the name of the input as shown. Example: 2K means to type 2K as shown.
{xxx}	Indicates a required user-defined input. Example: {Pn} means to type the number of lines (or spaces).

Note that angle brackets, < > and brackes, { } are not part of the command sequence, but are used to illustrate keyboard use and differentiate parts of the sequence.

CURSOR MOVEMENT COMMANDS

<ESC>[{Pn}A	Move cursor up
<ESC>[{Pn}B	Move cursor down
<ESC>[{Pn}C	Move cursor right
<ESC>[{Pn}D	Move cursor left
<ESC>[{Pl};{Pc}H	Direct cursor addressing
<ESC>[{Pl};{Pc}f	Direct cursor addressing
<ESC>[M	Reverse index

Where: {Pn} = number of lines up or down or spaces left or right
{Pl} = line position
{Pc} = column position

Example: To move the cursor to the right 32 spaces, type the ESC key, followed by a left bracket, the number 32, and capital D. Do not insert any space characters in the command.

CHARACTER ATTRIBUTE COMMANDS

<ESC>[{Ps};{Ps};{Ps};...;{Ps}m

{Ps} = a number from the following:

0 (or none)	All attributes off.
1	Bold on.
4	Underscore on.
5	Blink on.
7	Reverse video on.

Example: Set bold and blink attributes by pressing the ESC key, followed by 1;5m.

ERASING COMMANDS

<ESC>[K	Erase from cursor to end-of-line.
<ESC>[0K	Erase from cursor to end-of-line.
<ESC>[1K	Erase from beginning of line to cursor.
<ESC>[2K	Erase entire line containing cursor.
<ESC>[J	Erase from cursor to end-of-screen.
<ESC>[0J	Erase from cursor to end-of-screen.
<ESC>[1J	Erase from beginning of screen to cursor.
<ESC>[2J	Erase entire screen.

2. Press the space bar (or the FIELD SELECT key) to choose the desired characteristic.

3. Use the arrow keys (← or →) to select the next field.

4. Press "F1" to engage the selected characteristics and begin terminal emulation.

5. Press any other Functional Test Switch to exit the mode.

DISPLAY TEST 2-12

This test displays all characters and attributes in rapid succession. Simultaneously press switches 2 and 3 to initiate the test.

CLEAR/FILL SCREEN 2-13

This function test alternates display of a screen filled with a character set test pattern with a clear screen.

Press switch 4 once to initiate the test (character set screen), press again to display a clear screen.

Breakpoints 2-14.

To aid in demonstrating runuut and breakpoints, the following software table is setup to allow easy self-test entry and exit points. Routines other than those noted will save results of the test in RAM at address 1000H. Any non-zero value indicates a passing condition.

ENTRY ADDRESS	FUNCTION CALLED
F8000	Exit, executes a halt instruction
F8100	RAM test
F8200	ROM test
F8300	PIA initialization. No results.
F8400	PIA test
F8500	Terminal mode. No results.
F8600	UART initialization. No results.
F8700	UART test
F8800	Video initialization. No results.
F8900	Video test
F8A00	Fill video RAM with test pattern. No results.
F8B00	Clear video RAM. No results.

The following example shows how to use the table:

RUN UUT STARTING ADDR F8100 BREAK ADDR F8000

This example first jumps to the RAM test (F8100), storing the results of the test at 1000H, and then jumps to F8000 and stops. This method allows for clean entries to and exits from all self test routines. Set-up of only one breakpoint address is required. Upon returning from the indicated test all routines jump to the exit or breakpoint address F8000.

Termcap 2-15.

The Demo/Trainer can be operated with a UNIX™ computer system. However, the controlling computer termcap file must be altered so that some of the characters sent by that computer are translated into control codes understood by the Demo/Trainer. The required termcap is as follows:

```
dm|demo|trainer|demotrainer:\
        :cr=^M:do=^J:nl=^J:bl=^G:co#80:li#24:cl=50\E[;H\E[2J:\
        :le=^H:bs:cm=5\E[%i%d;%dH:\
        :ce=3\E[K:cd=50\E[J:\
        :ku=\E[A:kd=\E[B:kr=\E[C:kl=\E[D:kb=^H:\
        :ho=\E[H:ta=^I:pt:sf=2*^J:vt#3:am:\
        :sr=2*\EM:\
        :so=\E[7m:se=\E[m:us=\E[4m:ue=\E[m:\
        :md=\E[1m:mr=\E[7m:mb=\E[5m:me=\E[m:\
        :nd=2\E[C:up=2\K[A:
```

FAULT SWITCH DESCRIPTIONS 2-16.

Each fault switch allows the operator to introduce a simulated problem in some area of the Demo/Trainer. There are six switch banks, each consisting of eight segments.

The 48 possible fault switch settings are described in Table 2. The associated reference pertains to “x-y” locators found on sheet 1, 2, or 3 of the schematic diagram.

THEORY OF OPERATION 3-1.

This discussion deals with the Demo/Trainer on a functional block diagram level. Refer to the block diagram in Figure 2 and the component locator in Figure 3. In addition, a portion of the schematic diagrams is portrayed for each functional area. The full schematic diagrams, along with descriptions for mnemonics used on the diagrams and in this discussion, are presented at the end of this manual.

Microprocessor 3-2.

The Demo/Trainer uses an Intel® 80286 microprocessor, employing a 16-bit data bus and a 24-bit address bus. Refer to Figure 4. Microprocessor input and output lines used in the Demo/Trainer are described in Table 3.

NOTE

The pod connection, J5, provides all signal connections otherwise used by the on-board microprocessor U14.

Clock 3-3.

The Clock circuit is shown in Figure 5. U25B divides the 32-MHz oscillator (U18) output by two. The resulting 16 MHz (U25B-9) is used as the DOT clock in the video circuit. This signal is also divided by two again (U25A-5), deriving the 8-MHz clock signal used by the microprocessor. The 8-MHz clock is also used by the RAM Timing, Ready, and Bus Controller (U15) circuits. Ready and reset signals are synchronized to the 8-MHz clock with U1.

Some Demo/Trainer circuits operate more slowly and require wait states to operate with the 8-MHz 80286 microprocessor. The PIA (U31), the DUART (U11), and the Video Controller (U72) fall into this category. These circuits use three wait states, established by U17, to delay the READY- signal to the microprocessor.

Table 2. Fault Switches

FAULT SWITCH 1 (SW1)		
These switch segments are normally closed. Any segment set to OPEN introduces the described fault.		
SW1-1	Action: Result: Reference:	Open A15 at the Processor (U14-16) ROM and RAM test failure schematic sheet 1, 5C
-2	Action: Result: Reference:	Open ROM (U27-22) OE- line ROM Test on U29, U30 failure schematic sheet 1, 5B
-3	Action: Result: Reference:	Open IA19 to address decoder (U8) Causes ready problems at addresses where A19 is low schematic sheet 1, 4C
-4	Action: Result: Reference:	Open RAS- to DRAM RAM write/read errors schematic sheet 2, 5D
-5	Action: Result: Reference:	Open data out ID08 from DRAM U41-14 RAM write/read errors schematic sheet 2, 1C
-6	Action: Result: Reference:	Disconnect +5V from Processor (U14-62) UUT power fail schematic sheet 1, 6B
-7	- spare -	
-8	- spare -	
FAULT SWITCH 2 (SW2)		
These switch segments are normally set to OPEN. Any closed segment introduces the described fault.		
SW2-1	Action: Result: Reference:	Disable clock (U25-15) Pod Timeout schematic sheet 1, 7D
-2	Action: Result: Reference:	Short LED Drive data input (U32-17) to ground. Top LED decimal point stays on. schematic sheet 1, 2C
-3	Action: Result: Reference:	Short A09 to +5V BUS Test finds address drivability fault. schematic sheet 1, B8
-4	Action: Result: Reference:	Short A08 to A05. Also short to D08 if SW2-6 is closed, and short to D09 if SW2-8 is closed. Bus test finds all these errors. schematic sheet 1, B8

Table 2. Fault Switches (cont)

FAULT SWITCH 2 (SW2) (cont)		
-5	Action: Result: Reference:	Short A04 to ground. Bus test reports address bit tied. schematic sheet 1, B8
-6	Action: Result: Reference:	Short A05 to D08 with other possibilities as in SW2-4. Bus test reports the error. schematic sheet 1, B8
-7	Action: Result: Reference:	Short D12 to +5V Bus test reports the error. schematic sheet 1, B8
-8	Action: Result: Reference:	Short D09 to D08 with other combinations as in SW2-4. Bus test reports the error. schematic sheet 1, B8
FAULT SWITCH 3 (SW3)		
These switch segments are normally set to OPEN. Any closed segment introduces the described fault.		
SW3-1	Action: Result: Reference:	Short D05 to ground Bus test reports the error. schematic sheet 1, B7
-2	Action: Result: Reference:	Short ISPARE (spare interrupt input on U20-4) to ground. Pod reports Active Interrupt if trap turned on (default is trap off) schematic sheet 1, B7
-3	Action: Reference:	Short the microprocessor substrate filter capacitor (U14-52) to ground. schematic sheet 1, B7
-4	Action: Result: Reference:	Short INTR (U14-57) to ground. Prevents interrupts from occurring schematic sheet 1, B7
-5	Action: Result: Reference:	Short SRDY- (U1-2) to ground. I/O reads and writes will not work properly because they require wait states. RAM Test fails with unstable data during looping read. schematic sheet 1, 87
-6	Action: Result: Reference:	Short IM/IO to +5V (U22-6). I/O cannot be selected. schematic sheet 1, B7
-7	Action: Result: Reference:	Short ROM0- to +5V (U9-9). A read at any ROM0 address will not activate the ROM. schematic sheet 1, B7
-8	Action: Result: Reference:	Short ID08 to ID09 (U23-11, U23-12). Bus test will not detect the error, but a RAM test will. schematic sheet 1, B7

Table 2. Fault Switches (cont)

FAULT SWITCH 4 (SW4)		
These switch segments are normally set to OPEN. Any closed segment introduces the described fault.		
SW4-1	Action: Result: Reference:	Short IA08 to IA05 (U16-6 to U2-19). RAM test will expose this error. schematic sheet 1, B7
-2	Action: Result: Reference:	Short ID05 to gnd (U3-16). RAM test will find this error. schematic sheet 1, B7
-3	Action: Result: Reference:	Short ROM1- (U27-20) to gnd ROM Test on U29, U30 fails schematic sheet 1, A1
-4	Action: Reference:	Loopback Tx to Rx on J2 (the RS-232 connector). schematic sheet 1, B5
-5	Action: Reference:	Loopback CTS to RTS on J2 schematic sheet 1, A1
-6	Action: Reference:	Short CTS to ground (U12-8) schematic sheet 1, A1
-7	Action: Result: Reference:	Short RAM- (U58-6) to CAS- (U60-14) RAM test fails. schematic sheet 2, D6
-8	Action: Result: Reference:	Short R46 RAM side to +5V. This is the RA4 multiplexed address line on the DRAM. RAM address decoding errors. schematic sheet 2, 5C
FAULT SWITCH 5 (SW5)		
These switch segments are normally set to OPEN. Any closed segment introduces the described fault.		
SW5-1	Action: Result: Reference:	Disable DRAM refresh (U56-12) RAM Test with increased delay will detect this error schematic sheet 2, 7C
-2	Action: Result: Reference:	Short R49 RAM side to ground. This is the RA7 multiplexed address line on the DRAM. RAM address decoding errors. schematic sheet 2, 5C
-3	Action: Result: Reference:	Short U64-3 to U44-5 Refresh fault. RAM does not return ready. schematic sheet 2, 6C
-4	Action: Result: Reference:	Short CASU- (R50 RAM side) to +5V RAM R/W error. schematic sheet 2, 5C

Table 2. Fault Switches (cont)

FAULT SWITCH 5 (SW5) (cont)		
-5	Action: Result: Reference:	Short CASL- (R51 RAM side) to ground RAM R/W error. schematic sheet 2, B4
-6	Action: Reference:	Short AB05 (U83-9) video RAM address line to ground. schematic sheet 3, 6D
-7	Action: Reference:	Short character ROM A0 (U75-2) to ground. schematic sheet 3, 4D
-8	Action: Reference:	Short DADD05 (U72-29) to ground. schematic sheet 3, 7C
FAULT SWITCH 6 (SW6)		
These switch segments are normally set to OPEN. Any closed segment introduces the described fault.		
SW6-1	Action: Reference:	Short the blink attribute (U86-16) to + 5V. schematic sheet 3, 4C
-2	Action: Reference:	Short CCLK to ground (U72-16). schematic sheet 3, 3B
-3	Action: Reference:	Short U71-3 to ground. schematic sheet 3, 5B
-4	Action: Reference:	Loop back for keyboard test. schematic sheet 1, 3B
-5	- spare -	
-6	- spare -	
-7	- spare -	
-8	- spare -	

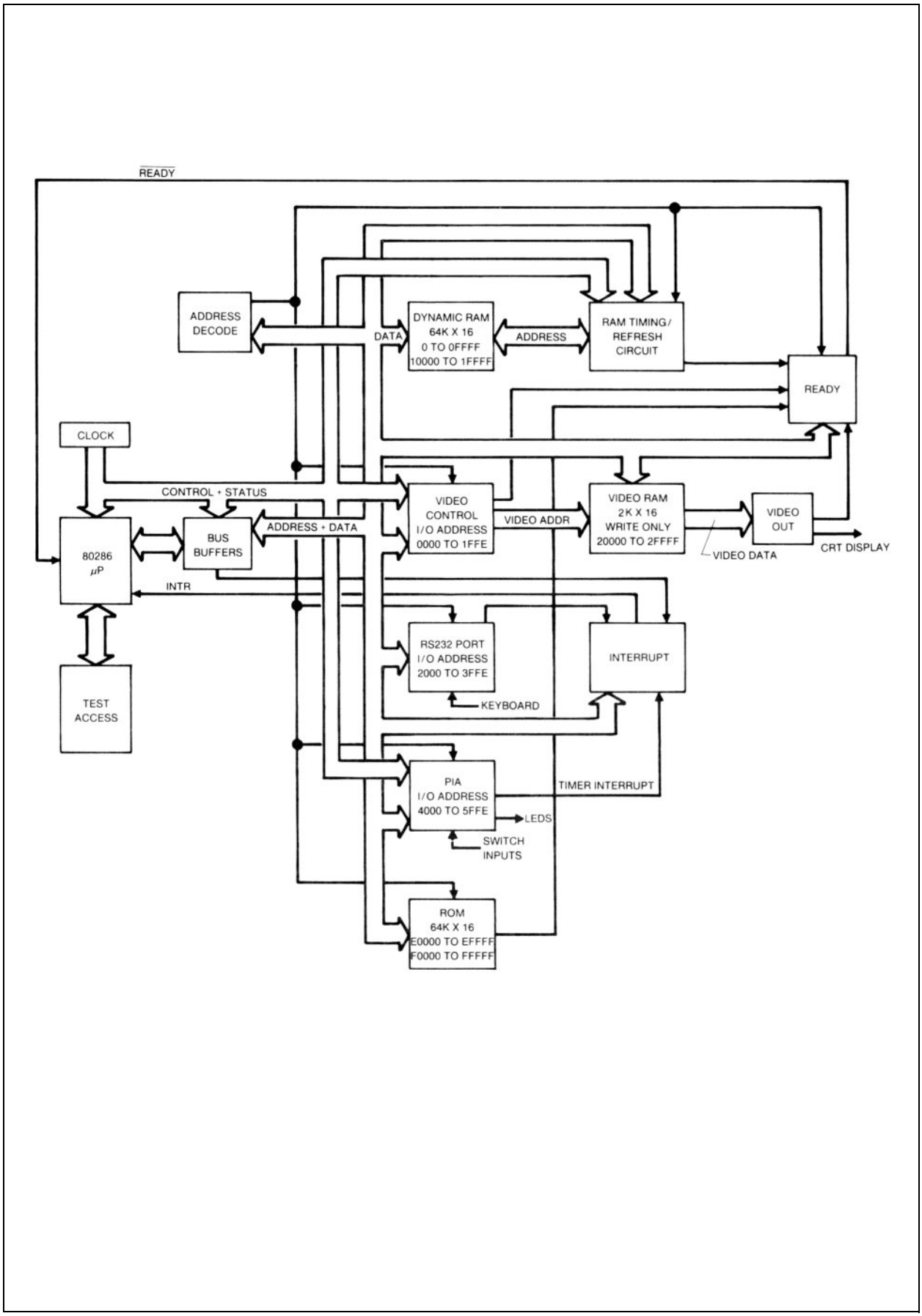


Figure 2. Functional Block Diagram

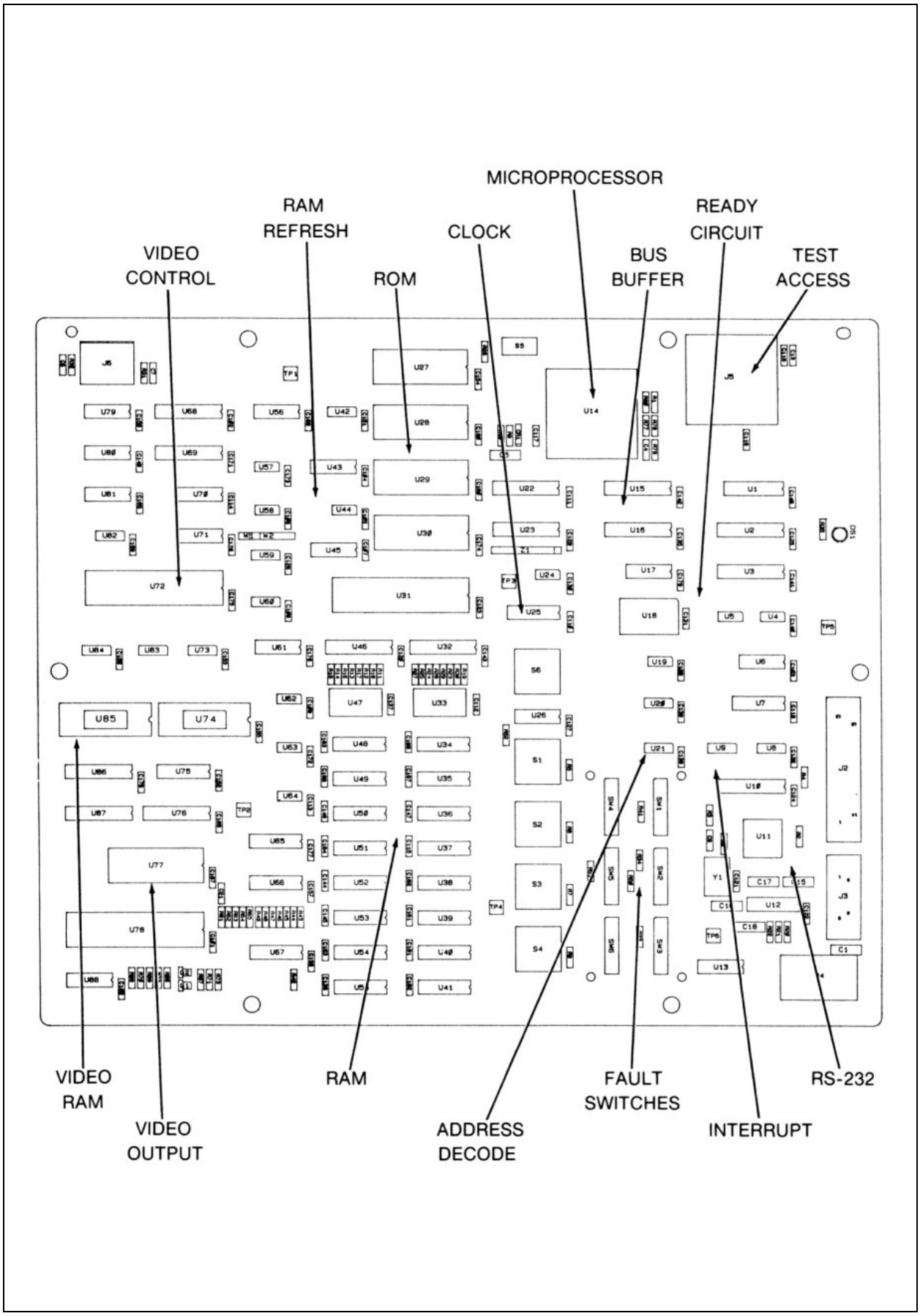


Figure 3. Functional Block Locator

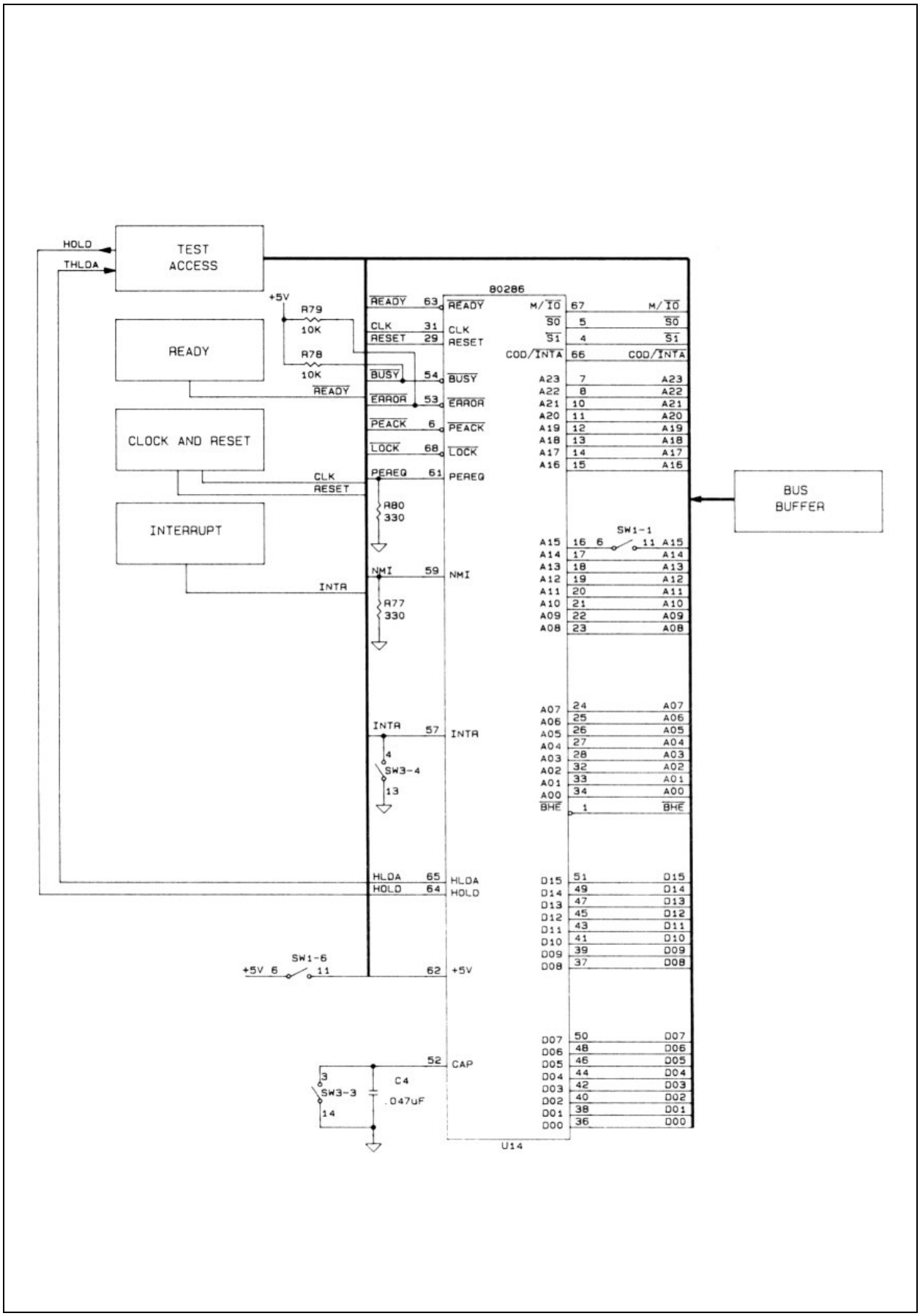


Figure 4. Microprocessor

Table 3. Microprocessor Input/Output Lines

A00-A23:	Address bus outputs for memory and I/O port addresses. A16-23 are low for I/O transfers. Both A0 and BHE- low indicates full word transfer (D00-15). A0 low and BHE- high indicates byte transfer on the lower half bus (D00-7). A0 high and BHE- lowindicates byte transfer on the upper half bus (D8-15).
BHE-:	Bus high enable output. When BHE- is low and A0 is high, BHE- specifies data transfer on the upper byte (D8-15) of the data bus.
CLK:	8-MHz system clock input
COD/INTA-:	Code/Interrupt Acknowledge. See M/IO-.
D00-D15:	Data bus output for memory and I/O write cycles, input for memory, I/O, and interrupt acknowledge read cycles.
HLDA:	Hold acknowledge output. The bus hold acknowledge condition is activated after the HOLD input is set. The 80286 sets HLDA high and tri-states the bus drivers.
HOLD:	Bus hold request input. Hold state can be set high with S5 in the TEST position, allowing for control by an external pod. In hold state, the bus drivers are tri-stated and HLDA is set true.
INTR:	Interrupt request input suspends current program execution if interrupts are enabled in software. The 80286 then responds by reading an 8-bit interrupt vector identifying the source of the external interrupt.
M/IO-:	Memory/I/O Select. With COD/INTA-, indicates the type of bus cycle.

M/IO-	COD/INTA-	
low	low	Interrupt Acknowledge Cycle
low	high	I/O Access Cycle
high	low	Memory Access Cycle
high	high	Instruction Fetch Cycle

READY-:	Bus ready input. When low, READY- terminates a bus cycle. All returned conditions are synchronous to the system clock. Some ready conditions require three wait states before READY- is returned low. The microprocessor will not complete a read or write until READY- has been returned low by the addressed device.
RESET:	High input lasting more than 16 system clock cycles clears the 80286 internal logic, setting output pins S0-, S1-, PEACK-, A0-A23, BHE-, and LOCK- high and M/IO-, COD/INTA-, and HLDA low. D0-D15 are tri-stated.
S0-, S1-:	Bus cycle status lines (outputs) that identify the beginning of a bus cycle and help identify the type of cycle.
+5V:	Vcc

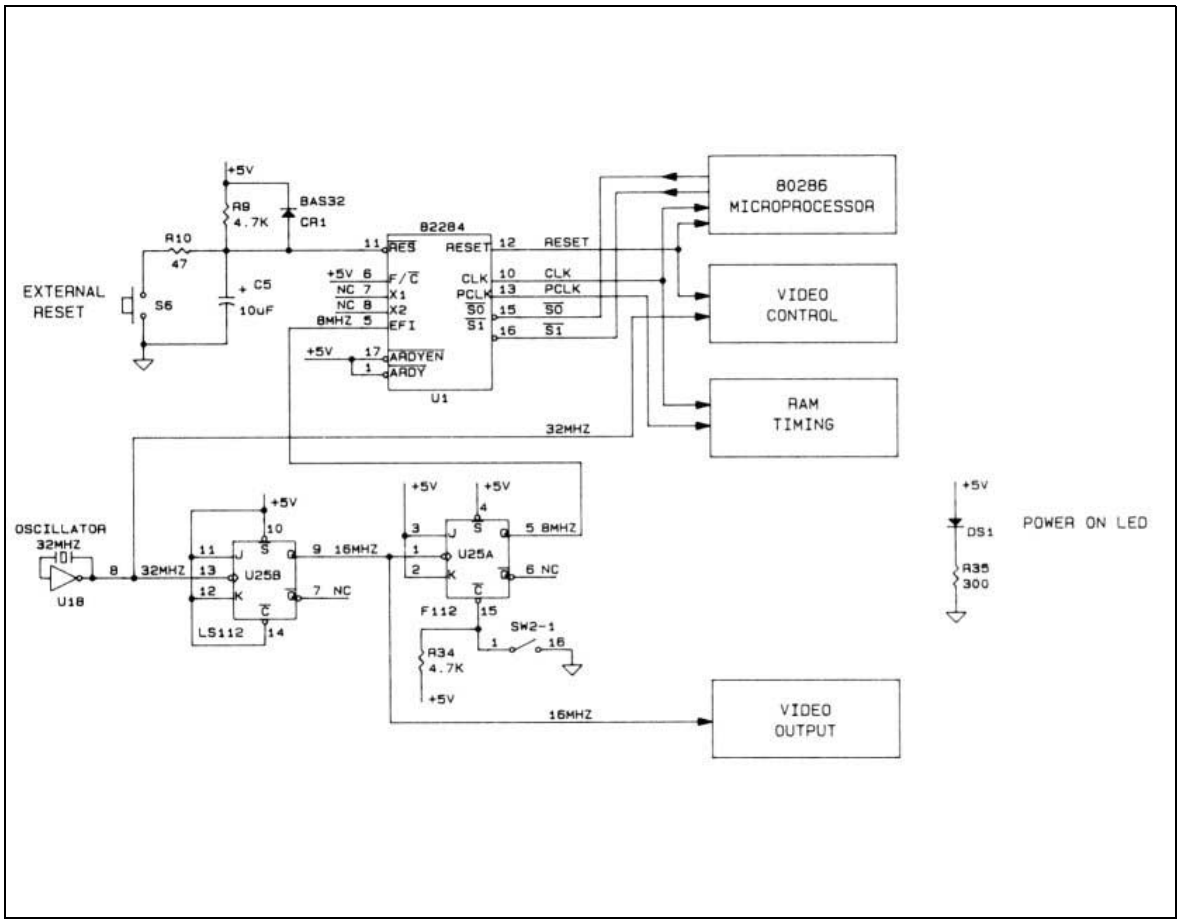


Figure 5. Clock

Test Access 3-4.

The Test Access functional block provides connections to all microprocessor lines as shown in Figure 6. Control passes to an external 80286 Pod connected at J5 when Test Switch S5 is set to TEST.

Bus Buffer 3-5.

The Bus Buffer, shown in Figure 7, uses an 82288 bus controller (U15) to decode status lines S0- and S1- from the microprocessor and generate command signals for bus cycle control. Three bus states are possible: addressing, data read/ write, or tri-state. An “I” is appended to some mnemonics, signifying signals internal to the Demo/Trainer. For example, data bus lines D00-D15 become internal lines ID00-15.

The address bus (A00-23) is buffered with latches U2, U16, and U22. The rising edge of each ALE transition latches a new address.

For the data bus (D00-15), the 82288 outputs control signals DEN (data enable) and DT/R- (data transmit/receive). These two signals control the state of data bus transceivers U23 and U3. For a write cycle, both DEN and DT/ R- are high. Read cycles are enabled when DEN is high and DT/R- is low.

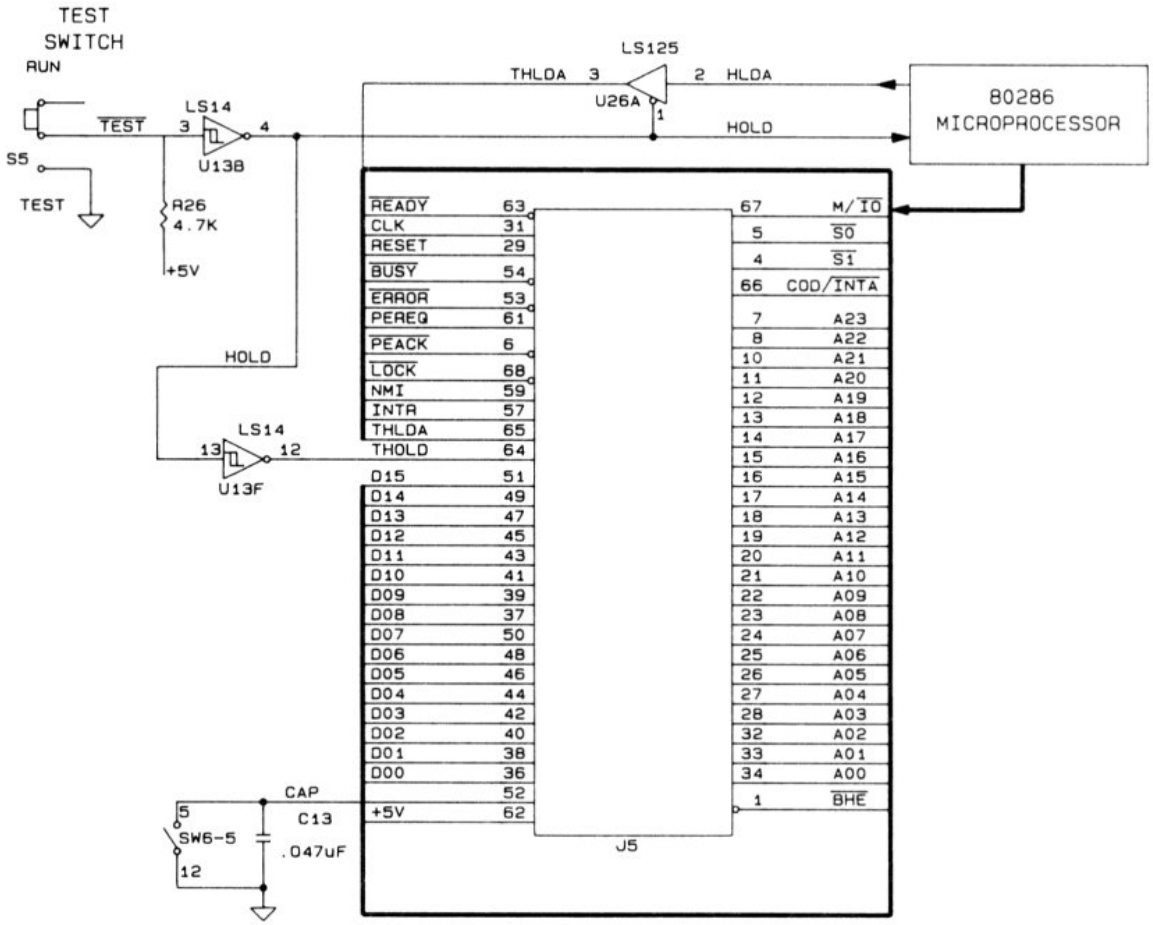


Figure 6. Test Access

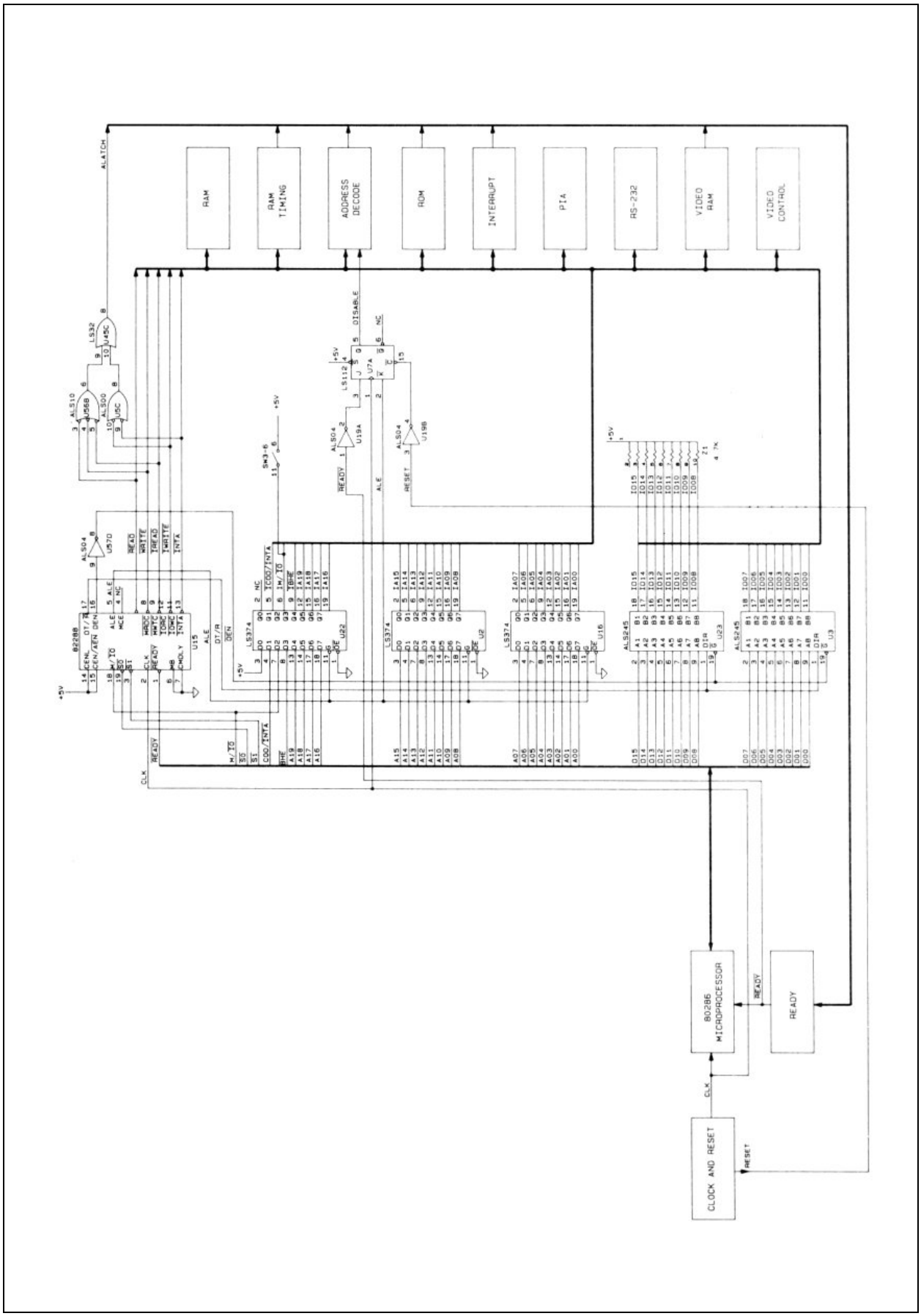


Figure 7. Bus Buffer

Address Decode 3-6.

The Address Decode circuit (U8, U9, and U21) selects the memory or I/O device being addressed. Refer to Figure 8. Some of the buffered address lines and bus controller lines are monitored to enable reads from either ROM (ROM0- or ROM1- set low), the interrupt vector (IPOLL- set low) or RAM (RAM0-, RAM1-, or VRAM- set low). Address Decode may also enable the following select lines:

- VIDSLT-
  Read or write from/to the video controller.

- PPISLT-
  Write outputs to PIA LEDs or read inputs from the Functional Test Switches.

- I/OSLT-
  Read the ASCII keyboard or read/write from/to the RS-232 port.

The Address Decode outputs are as follows:

ADDRESS DECODE OUTPUT	RANGE ENABLED	CIRCUIT ADDRESSED
RAM0-	00000-0FFFF	64K byte dynamic RAM
RAM1-	10000-1FFFF	64K byte dynamic RAM
VRAM-	20000-2FFFF	Video RAM
IPOLL-	30000-3FFFF	Interrupt polling
SPARE1-	40000-4FFFF	(ready is returned)
SPARE2-	50000-5FFFF	(ready is returned)
ROM0-	E0000-EFFFF	64K byte ROM
ROM1-	F0000-FFFFF	64K byte ROM
I/O ADDRESSES		
VIDSLT-	00000-01FFE	Video Control
I/OSLT-	02000-03FFE	RS-232 port UART
PPISLT-	04000-05FFE	PIA

ROM 3-7.

Demo/Trainer operating system code is stored in two 32K X 8 Eproms, U27 and U28. Refer to Figure 9. Since a 16-bit system is used, ROM is organized as 32K X 16 (F0000 to FFFFE). Although this comprises a 64K address range, ROM can only be accessed in 16 bit mode, and A0 is consequently not connected to the ROM address lines. A0 is always low in word accesses. At reset, 80286 code execution begins at the reset address (FFFFF0). Address lines A20-A23 are not used, and ROM accesses do not require wait states.

RAM and RAM Timing 3-8.

The RAM circuit is portrayed in Figure 10. RAM Timing (circuit and timing diagram) is shown in Figure 11. The Demo/Trainer uses 128K bytes of dynamic RAM. Composed of sixteen 4164 chips, RAM is primarily used for storing arrays, variables, stack, interrupt service address, and results from built-in self-test routines.

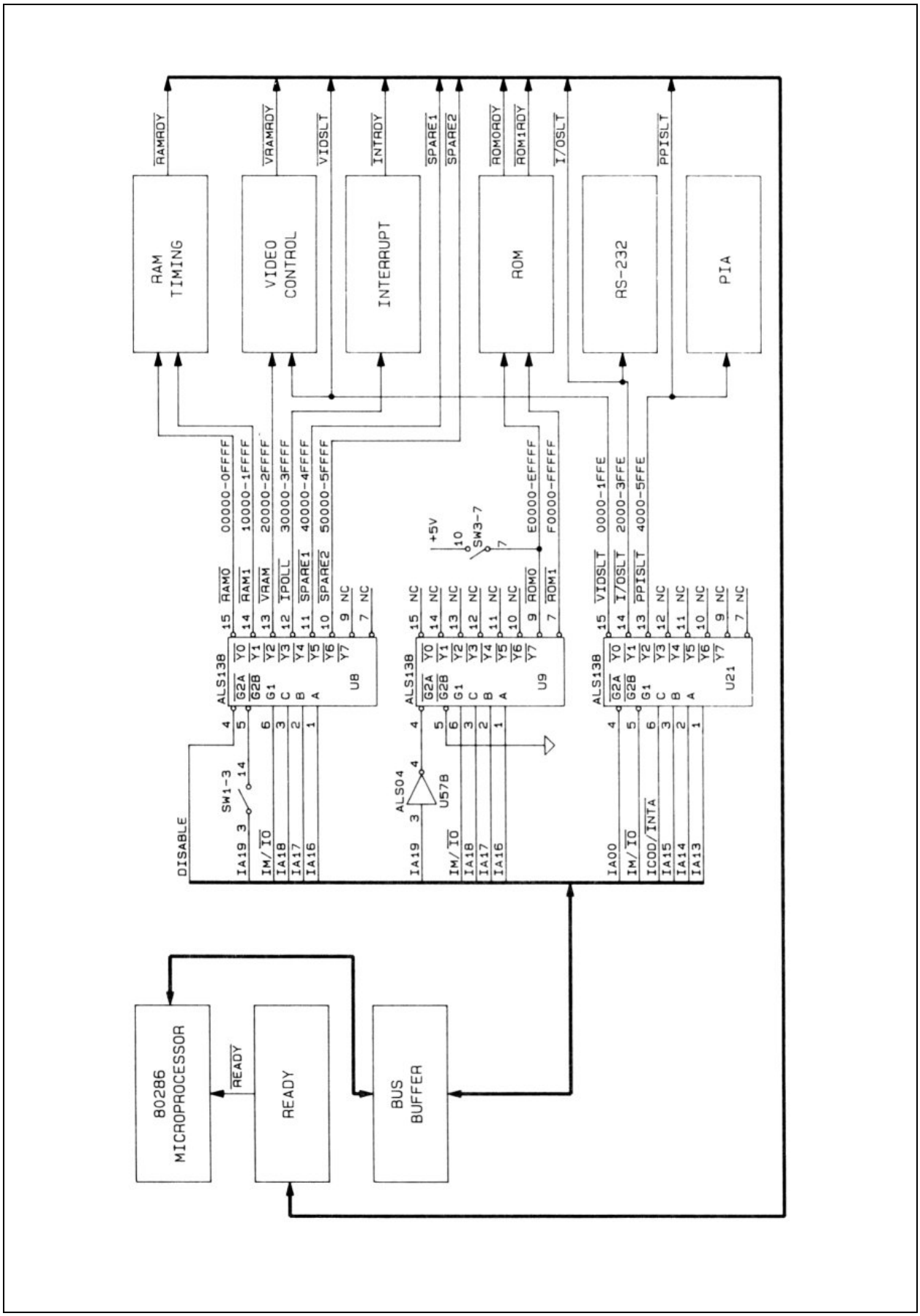


Figure 8. Address Decode

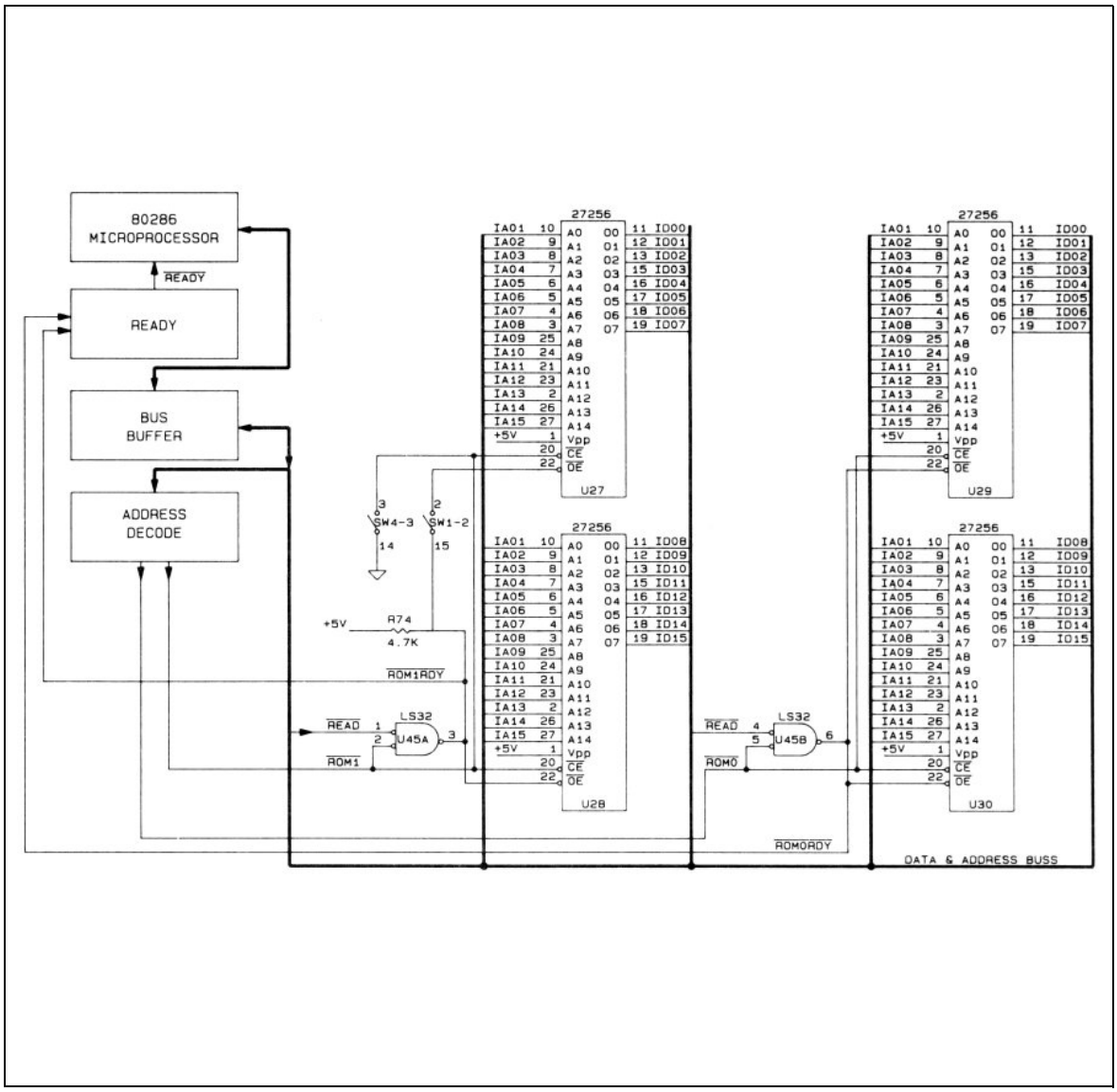


Figure 9. ROM

To select RAM, U65 and U66 multiplex 16 address lines into 8 address signals. The multiplexed address is then latched into the RAM chips by two externally applied clock pulses. The first, the negative going edge of the row-address-strobe pulse (RAS-), latches the 8 row address bits. The second, the negative going edge of the column-address-strobe pulse (CAS-), latches the 8 column address bits. Timing for RAS and CAS is determined by delay line U60. CAS is a delayed RAS signal; it goes low 55 nsec after RAS goes low.

The 80286 can access upper and lower bytes separately or together as a word. RAM is organized as 128K bytes addressed from 00000 to 1FFFE. Access is accomplished by gating CASL- and CASU- (U58D). IA00 (internal buffered address bit zero) selects D0-D7 and IBHE- (internal buffered bus high enable) selects D8-D15. The low byte is accessed when IA00 is low. The high byte is accessed when IBHE- is low. The entire word is accessed when both IA00 and IBHE- are low. The processor determines the type of access based on the instruction being executed.

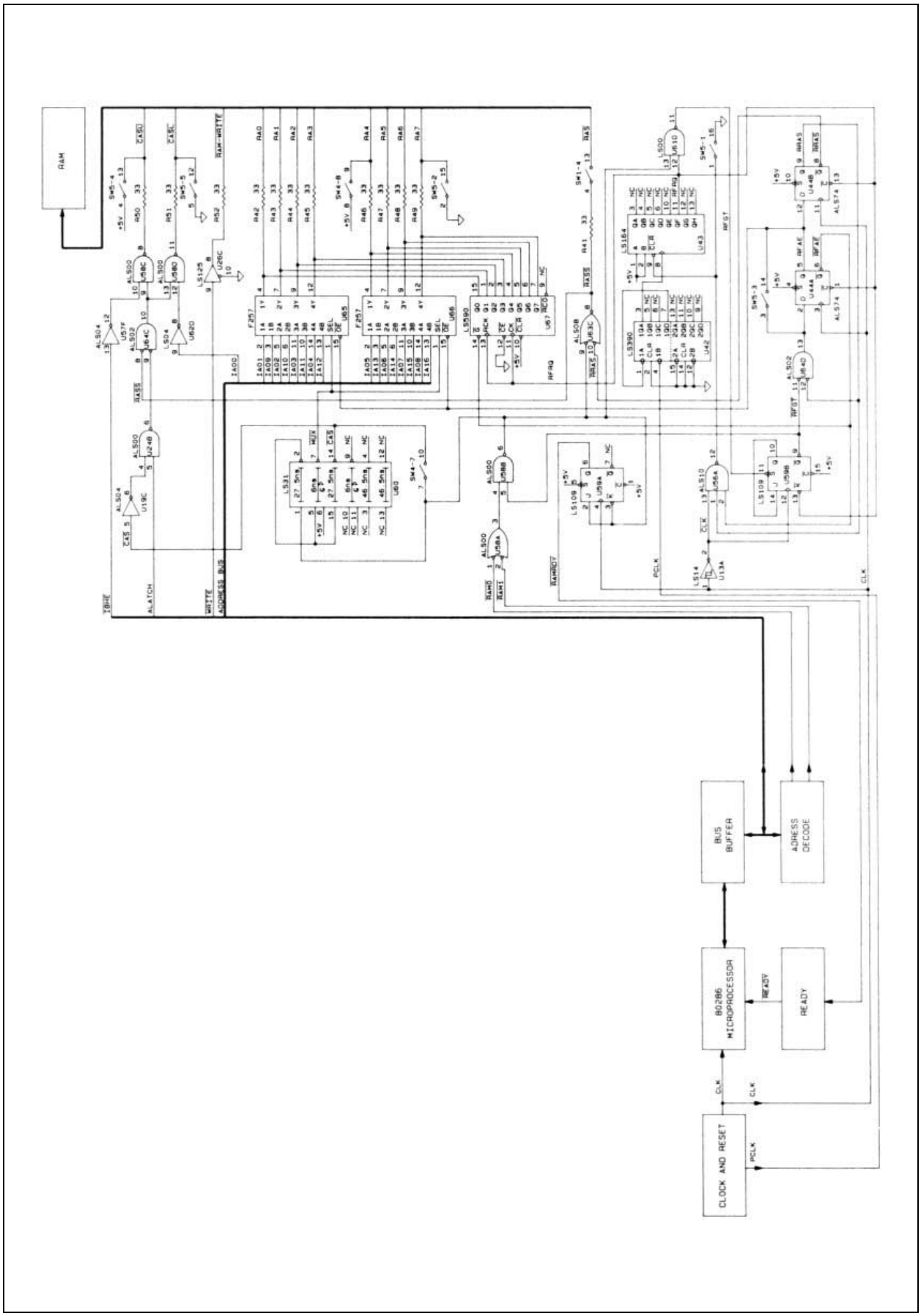


Figure 10. RAM

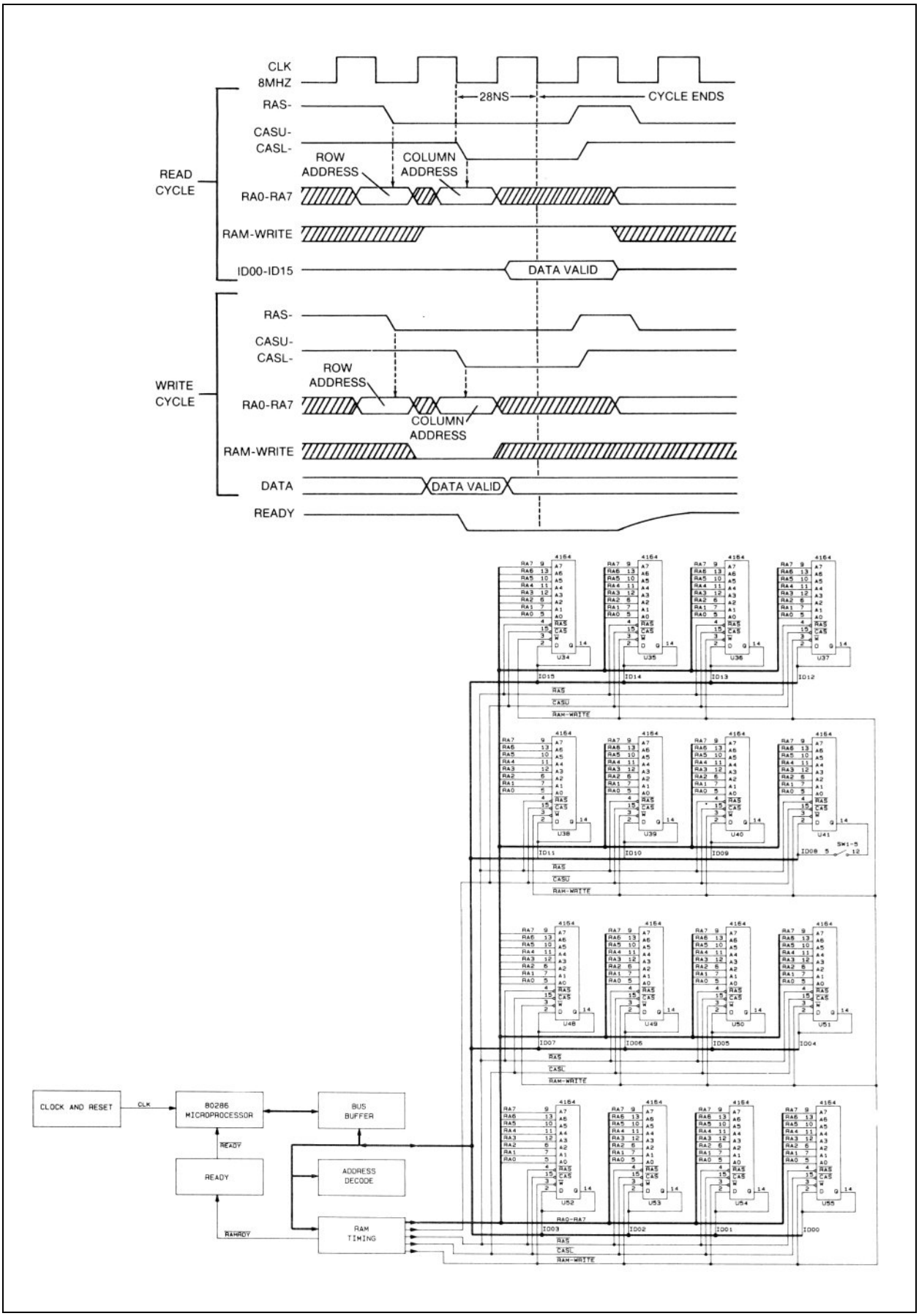


Figure 11. RAM Timing

RAM Refresh 3-9.

To maintain data, each of the 128 RAS addresses of the ram must be refreshed (or read) every 2 msec. The Demo/Trainer uses the RAS-only refresh method for this purpose. A RAS-only refresh cycle asserts only the RAS line to strobe in the refresh address.

A single Demo/Trainer row refresh occurs every 15 usec. A complete refresh entails 128 row refreshes, requiring about 1.9 msec.

The RFRQ (refresh request) signal both marks the need for a refresh cycle and increments the refresh address counter U67. U42 and U43 are used to divide PCLK (4 MHz) by 16 to produce RFRQ.

RAM refresh and RAM access are mutually exclusive. U61D insures that a refresh cannot occur if a ram access is in progress, Conversely, if a refresh is in progress and the processor asks for a RAM access, U58B prevents ready from being returned, resulting in the addition of a wait state. The processor is thus put on hold until the refresh has been completed.

RAM refresh is carried out in the following fashion:

1. If RAM- is high (no ram access in progress) and refresh is being requested, U61D outputs RFGT (refresh grant).

2. RFGT high enables the U44A(U44B state machine. This circuit times the output of refresh address enable (RFAE) to U67. After the proper refresh address setup time, is also enables Refresh RAS (RRAS) to strobe in the refresh address.

3. After the refresh address is strobed in, RFGT goes low, allowing processor access of ram.

Ram Refresh timing is illustrated in Figure 12.

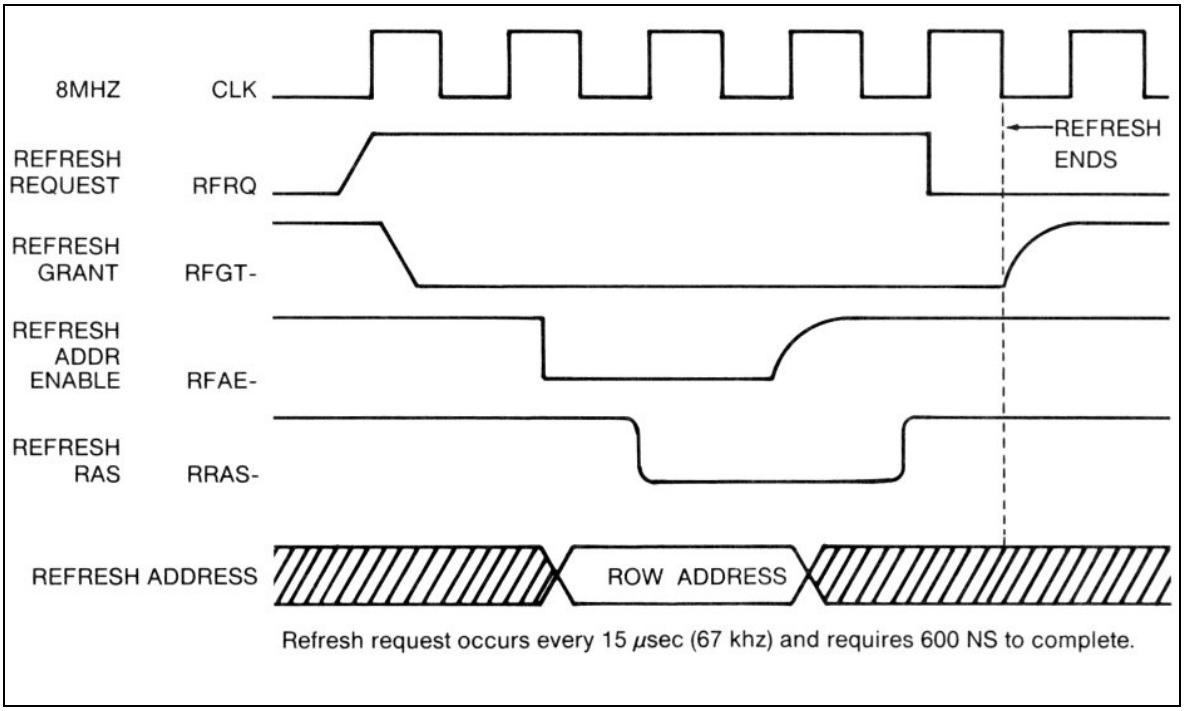


Figure 12. RAM Refresh Timing

Ready Circuit 3-10.

The microprocessor does not proceed to the next instruction cycle until it receives a READY- signal (low) from the Ready Circuit. Any circuit addressed by the microprocessor must return a ready signal to complete the current bus cycle. RAM, ROM, Video RAM, and interrupts do not require wait states. Some of the circuits (PIA, I/O, and Video Controller) cannot match the speed of the microprocessor and must use three wait cycles for synchronization. The Ready Circuit is shown in Figure 13.

Interrupt Circuit 3-11.

Refer to Figure 14. Demo/Trainer interrupt software cycles the lower LED one segment at a time. Since a new interrupt is generated every 100 ms, this LED indicates that the microprocessor is running. Each cycle starts when the continuously-running TIMER- output from U11 goes low. An interrupt can also be generated by closing fault switch SW3-2. In either case, U20 supplies 8:3 encoding of the interrupt source for storage as the interrupt vector by U10. At each interrupt, U20-14 returns an interrupt request (INTR high) to the microprocessor.

The following three things must then happen before the interrupt vector is read by the microprocessor: the microprocessor must set interrupt acknowledge (INTA-) low, the bus controller (U15) must set a read cycle (READ- low), and the address decoder (U8) must select the interrupt address bank by setting IPOLL- low. The microprocessor now moves the current operating program to the stack and enters the service routine. The rotating (lower) LED is advanced one segment, the Functional Test Switches are checked, and the interrupt timer (part of U11) is reset. The microprocessor then retrieves the stack and exits the service routine.

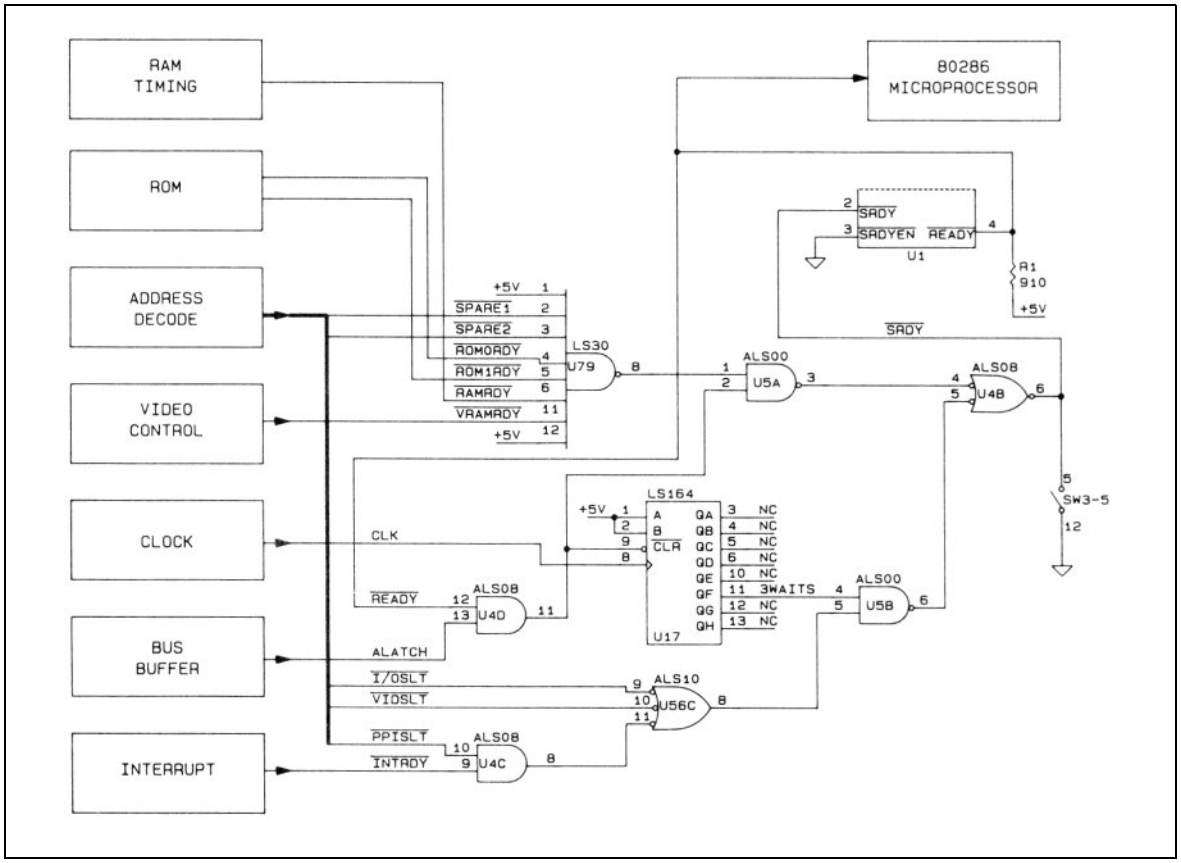


Figure 13. Ready Circuit

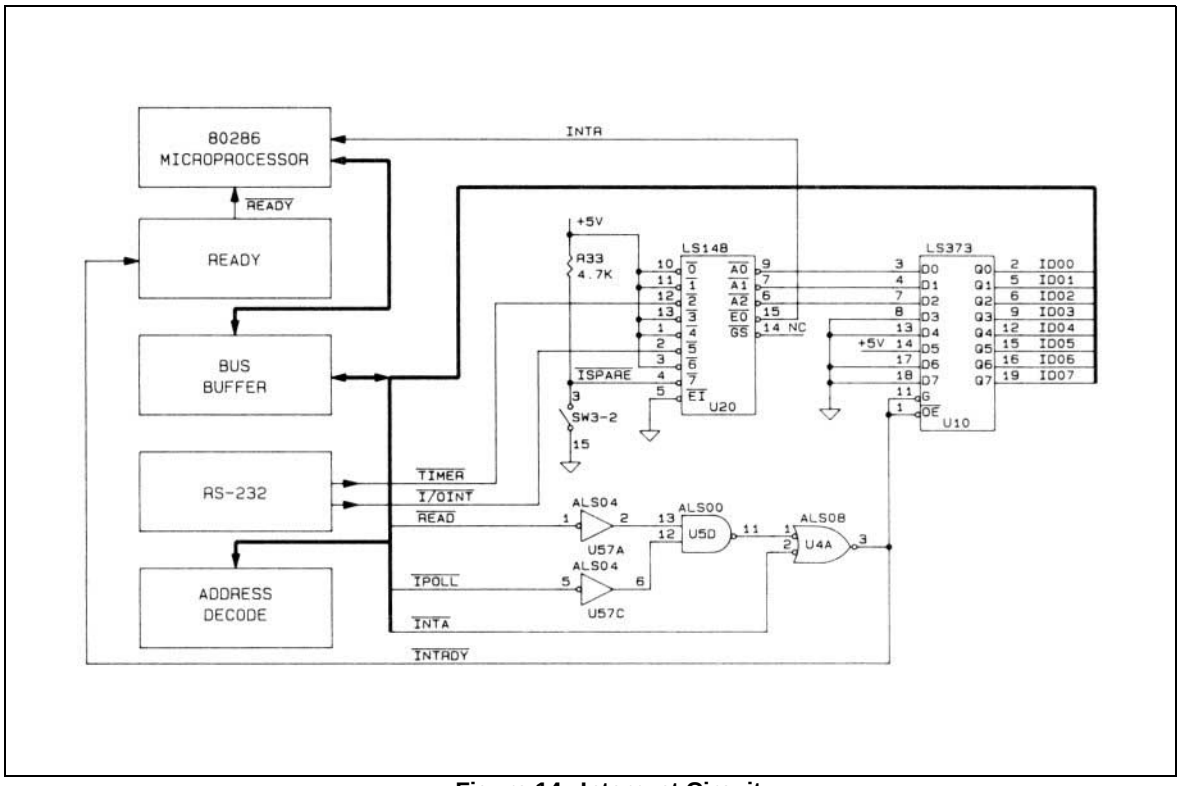


Figure 14. Interrupt Circuit

Video Control 3-12.

The Demo/Trainer uses the Signetics (R) 2674 Advanced Video Display Controller (AVDC), U72, along with the 2675 Color/Monochrome Attributes Controller (CMAC), U78. The 2674 and 2675 are programmable devices designed for use in CRT terminals and display systems that employ raster scan techniques. The CMAC is discussed under Video Output below. The 2674 (AVDC) generates the vertical and horizontal timing signals necessary for the display of data on a CRT monitor. It is programmed with monitor setup information, providing cursor, blanking, and clock signals to the CMAC (U78). In time with horizontal (HSYNC) and vertical (VSYNC) sync signals, the AVDC addresses Video RAM (U74 and U85) and the Character PROM (U77) on lines DADD00-11. This sequencing yields display characters using the ASCII codes supplied by the microprocessor (and stored in Video RAM) and the correct display characters stored in the Character PROM.

The video control circuit is illustrated in Figure 15. Figure 16 shows video timing.

Video RAM 3-13.

U74 and U85 provide two kilobytes of static video RAM. The associated circuit is shown in Figure 17. When addressed over the main address bus (IA01-11),Video RAM is used to store ASCII character codes supplied by the microprocessor over the main data bus (DB00-15). The video system on the Demo/Trainer is character-mapped, meaning that a specific video ram address maps into a physical location on the monitor screen. Video RAM is write-only.

Video Control sequentially samples these addresses over lines DADDOO-11 and generates display characters using the ASCII codes found at these addresses and the corresponding display character information found in the Character PROM (U77). The most significant bit of Video RAM is used for video attributes. The least significant bit comprises the ASCII code for the character to be displayed.

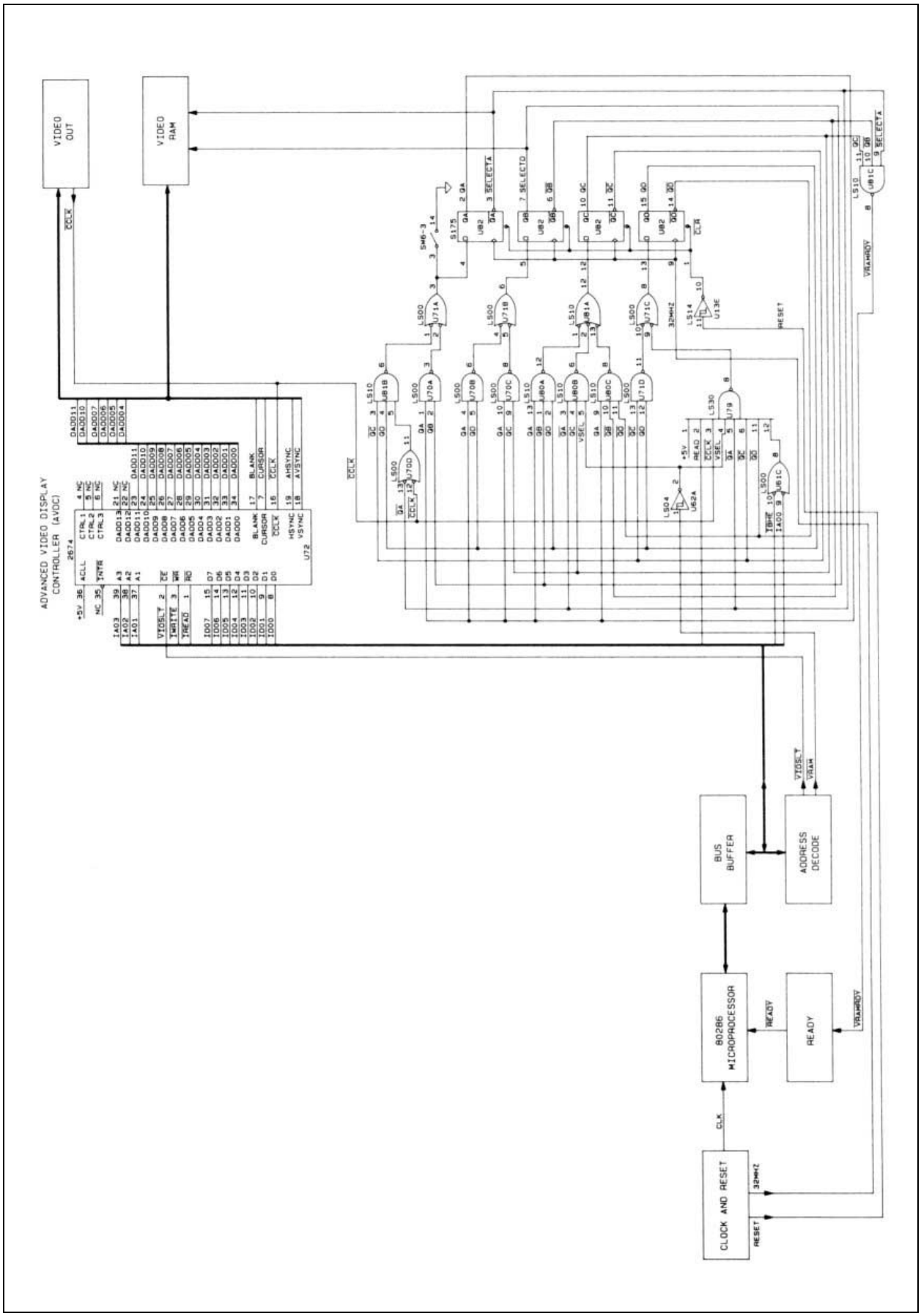


Figure 15. Video Control Circuit

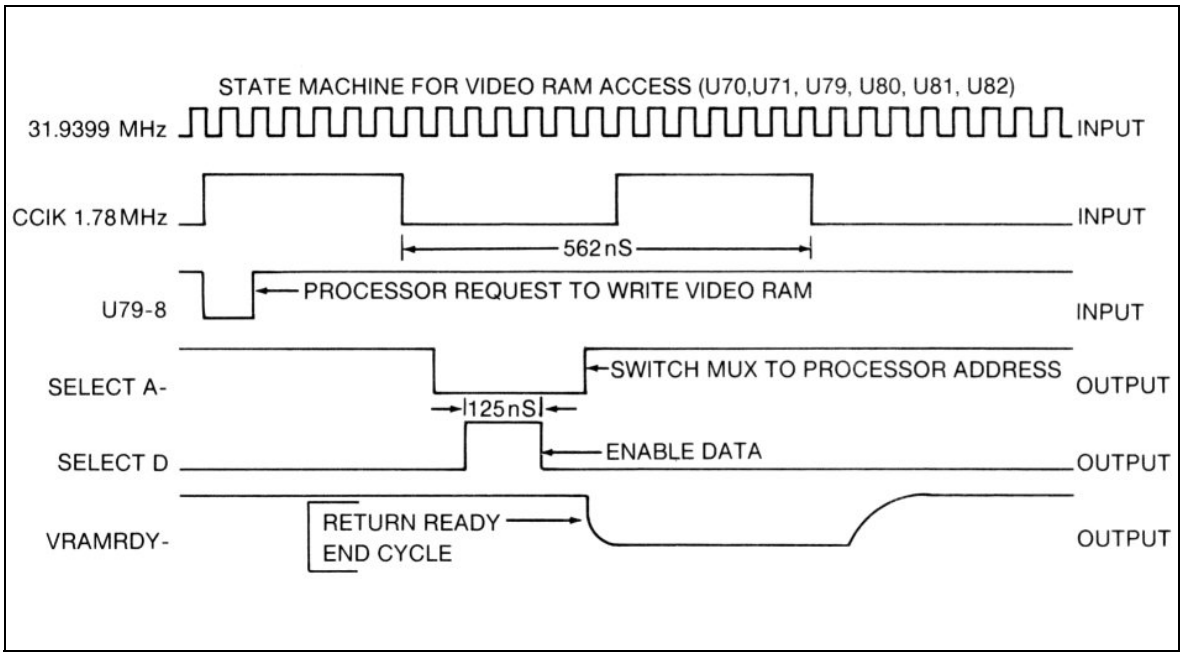


Figure 16. Video Timing

Video Output 3-14.

The Video Output, shown in Figure 18, comprises the 2675 Color/Monochrome Attributes Controller (CMAC) and associated circuitry. The 2675 contains a programmable dot clock divider to generate a character clock, a high speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the display.

Associated circuitry includes latches U87 and U76, which clock in display information provided by the character PROM, and Q1 and Q2, which boost the video signal before it is synchronized with the HSYNC and VSYNC at the crt.

RS-232 3-15.

The dual asynchronous receiver-transmitter (DUART) U11 receives serial data input from the keyboard (RXDA/TXDA) and handles bi-directional signal flow with the RS-232 port (RXDB/TXDB). Associated circuitry is illustrated in Figure 19. Keyboard input must be at 1200 baud. U12 acts as a level shifter, coupling TTL signal levels on the Demo/Trainer to RS-232 levels at the serial interface. U12 uses a “charge pump” to shift levels from a +5V source to ±10V RS-232 signals.

Programmable Interface Adapter (PIA) 3-16.

The Programmable Interface Adapter is shown in Figure 20. The PIA (U31) can be programmed for operation with three ports, each with 8 data lines. Each port is addressed for read or write by address lines IA01 and IA02. In the Demo/Trainer, ports A (lines PA0-7) and B (lines PB0-7) are used for outputs to the two on-board seven-segment LEDs. “A” corresponds to the upper LED, which shows the number of the self-test in progress. “B” corresponds to the lower LED, which shows a cycling indication when code is running, a flashing “F” when a fault has been detected, or blank during self-test selection. Port C (lines PC0-7) is used for inputs from the four Function Test Switches.

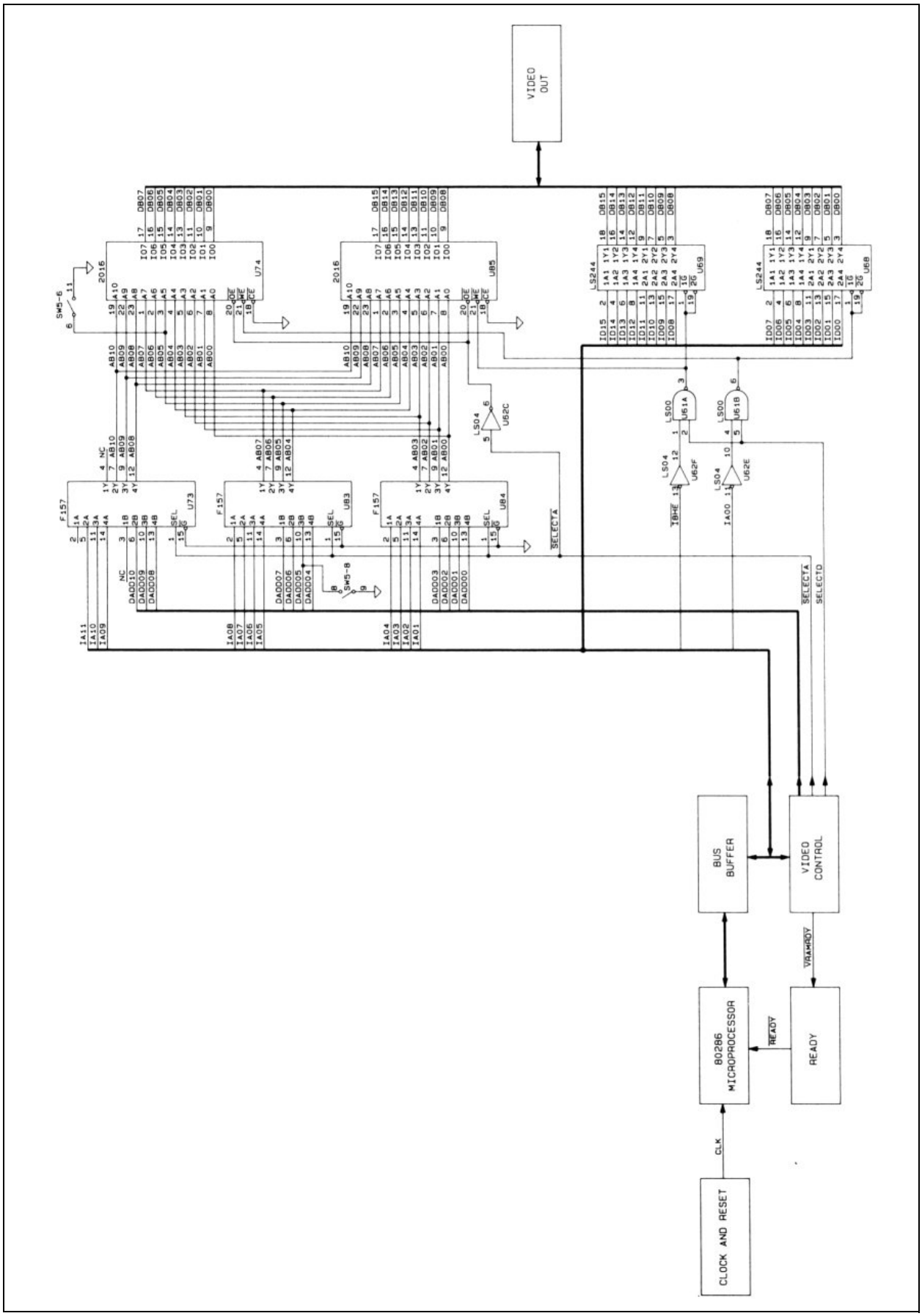


Figure 17. Video RAM

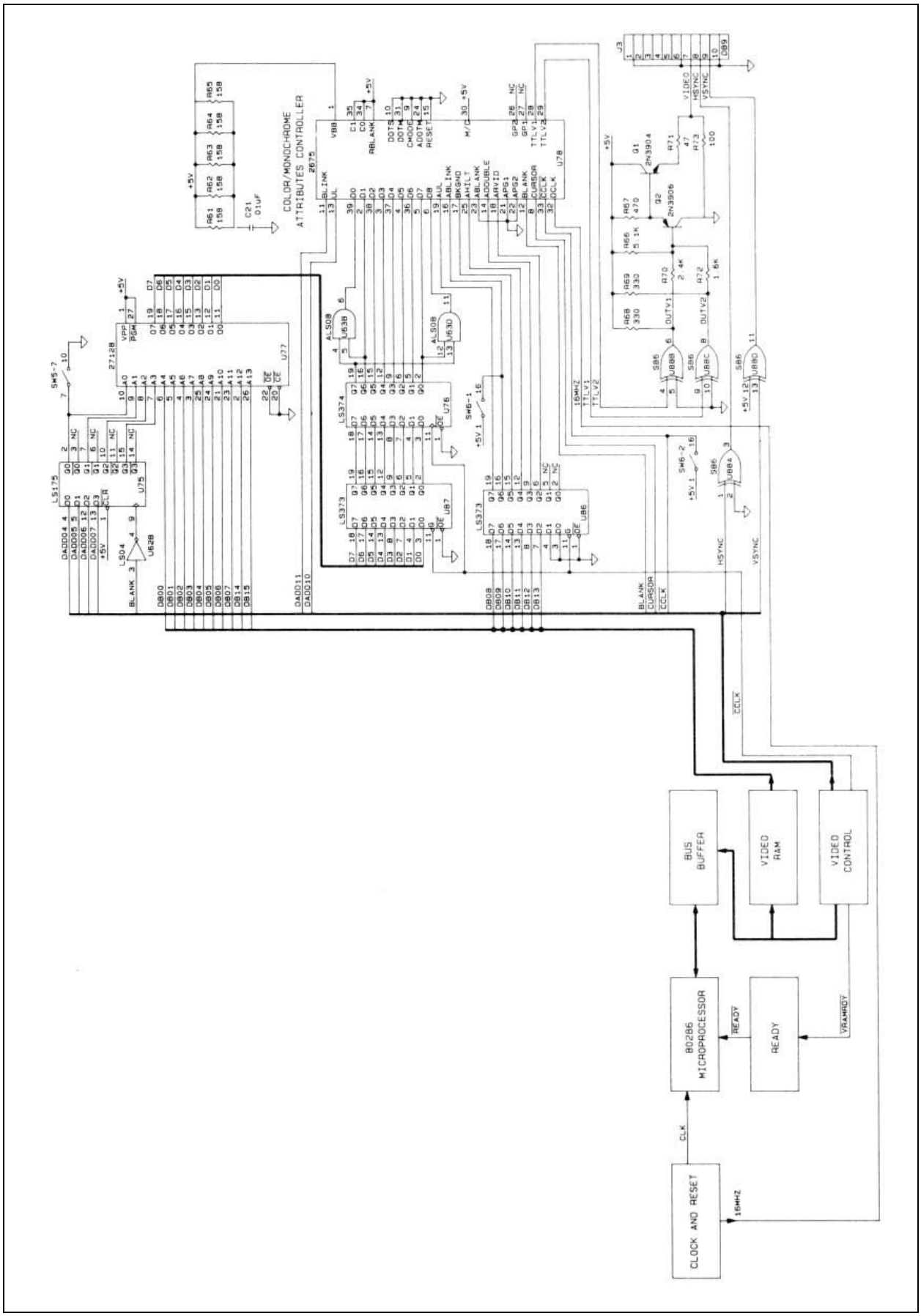


Figure 18. Video Output

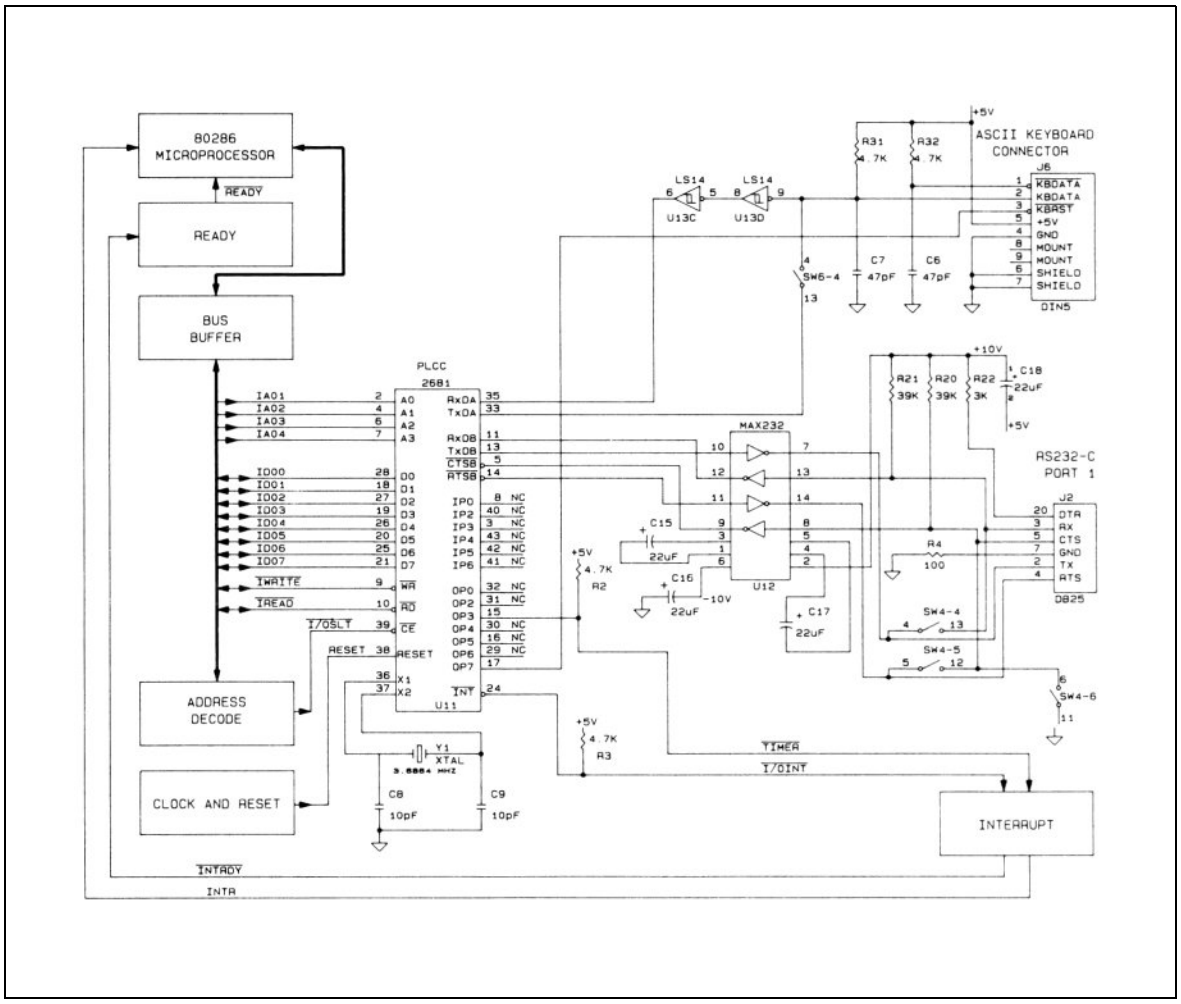


Figure 19. RS-232

Fault Switches 3-17.

Fault Switches are electrically connected throughout the Demo/Trainer circuitry. Refer to the Table 2, Fault Switches, earlier in this manual for detailed descriptions of switch functions and electrical locations. The schematic diagrams referenced in Table 2 are found at the end of this manual.

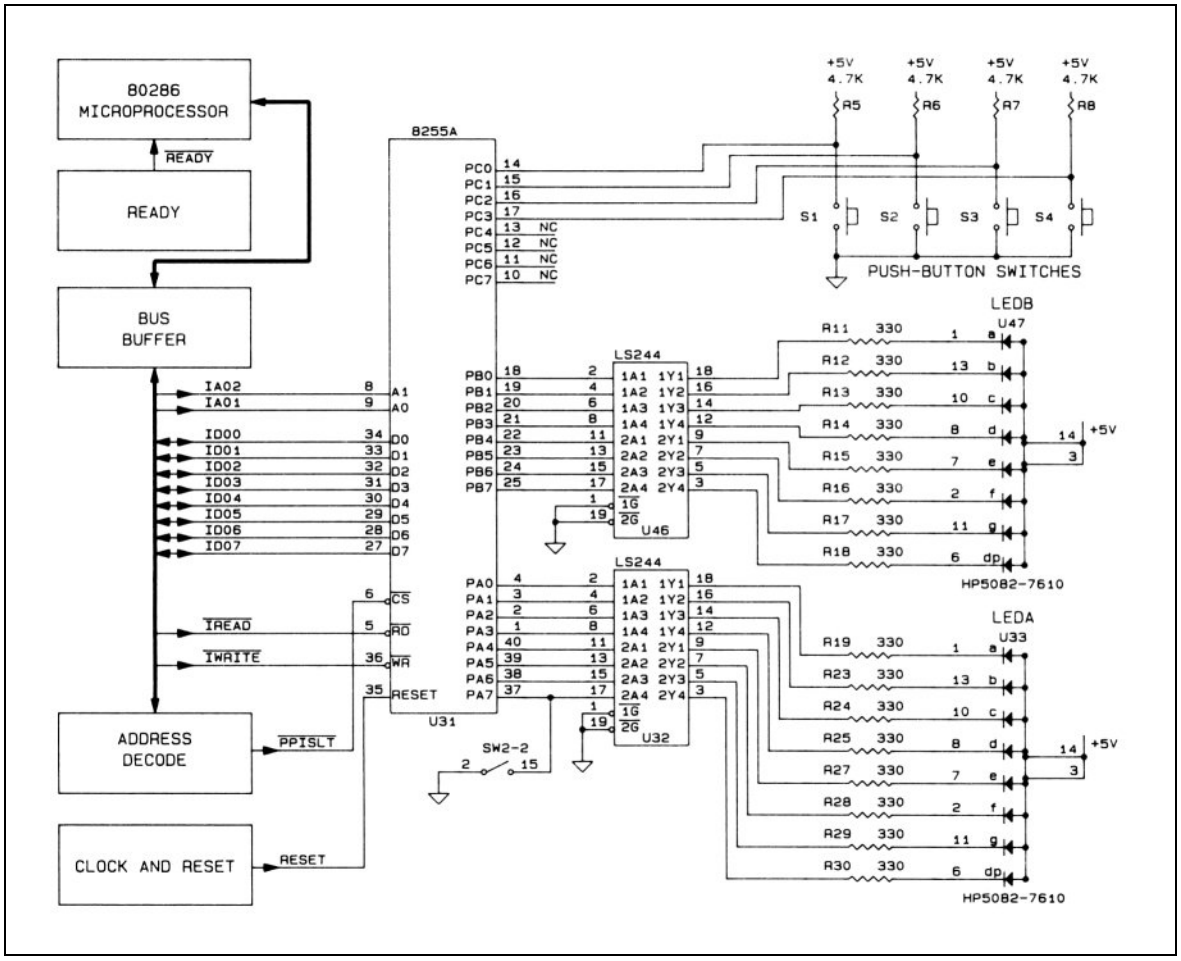


Figure 20. Programmable Interface Adapter (PIA)

LIST OF REPLACEABLE PARTS 4-1.

Introduction 4-2.

An illustrated parts list for the Demo/Trainer follows. Parts are listed alpha-numerically by assembly and reference designator.

The parts lists provides the following information for each part:

1. Reference Designator.
2. Description.
3. Fluke Stock Number.
4. Federal Supply Code for Manufacturers.
5. Manufacturer's Part Number.
6. Total Quantity of Components Per Assembly.
7. Recommended Quantity.

How to Obtain Parts 4-3.

All components may be ordered from the John Fluke Mfg. Co., Inc. or an authorized representative using the FLUKE STOCK NUMBER.

Some components may be ordered directly from the manufacturer using the manufacturer's part number. In the event that the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt and efficient handling of your order, include the following information.

1. Instrument Model and Serial Number.
2. Fluke Stock Number.
3. Reference Designator.
4. Printed circuit assembly (pca) part number and revision letters. The revision level of the printed wiring board and the revision level of the assembly should both be provided.
5. Description.
6. Quantity.

Price information for parts is available from the John Fluke Mfg. Co., Inc. and its authorized representatives. Prices are also available in a Fluke Replacement Parts Catalog, which is available on request.

CAUTION

An asterisk indicates a device which may be damaged by static discharge.

SCHEMATIC DIAGRAM 5-1.

The schematic diagram for the Demo/Trainer is presented at the end of this manual.

Table 4. Demo/Trainer Final Assembly
(See Figure 21.)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N 0 T -E-
	*	DEMO/TRAINER PWB ASSEMBLY	767962	89536	767962	1		
BT 1		POW SUP,30W,5 @ 6A,OPEN FRAME	627844	89536	627844	1		
F 1		FUSE,1/4 X 1-1/4,SLOW,1.0A,250V	109272	71400	MDL1A	1		
FL 1		FILTER,LINE,240V/6A	446328	05245	6J4	1		
H 1		SCREW,MACH,PHP,S.STL,6-32X3/8	334458	89536	334458	1	5	
H 2		SCREW,MACH,PHP SEMS,STL,8-32X3/8	436030	89536	436030	4		
H 3		SCREW,MACH,FHP,STL,10-32X1/2	114520	89536	114520	6		
H 4		NUT,STL,CAP EXT LW,6-32X7/64	152819	89536	152819	9		
MP 1		CASE, DEMO/TRAINER	802116	89536	802116	1	1	
MP 2		FRONT PANEL, DEMO/TRAINER	788505	89536	788505	1		
MP 3		SCREEN, DEMO/TRAINER	788604	89536	788604	1		
MP 4		BRKT, POWER SUPPLY, DEMO/TRAINER	788463	89536	788463	1		
MP 5		A C BARRIER	805762	89536	805762	1		
MP 6		PROGRAMMED FLOPPY,DEMO/TRAINER USER	816256	89536	816256	1		
MP 7		SHIPPING CONTAINER/FOAM, DEMO/TRAINER	803130	89536	803130	1		
S 1		SWITCH,ROCKER,DPST	800649	89536	800649	1		
TM 1		DEMO/TRAINER OPERATIONS MANUAL	803148	89536	803148	1		
U 27, 30	*	PROGRAMMED 27256 V1.0 U 27, 30	818757	89536	818757	2	1	
U 28, 29	*	PROGRAMMED 27256 V1.0 U 28, 29	818765	89536	818765	2	1	
U 77	*	PROGRAMMED 27128A-150 V1.0 U 77	818740	89536	818740	1		
W 1		CORD, LINE, R/A 5-15/IEC, 3-18AWG, SVT	363481	89536	363481	1		
W 2		HARNESS, POWER SUPPLY, DEMO UUT	788612	89536	788612	1	1	

An * in 'S' column indicates a static-sensitive part.

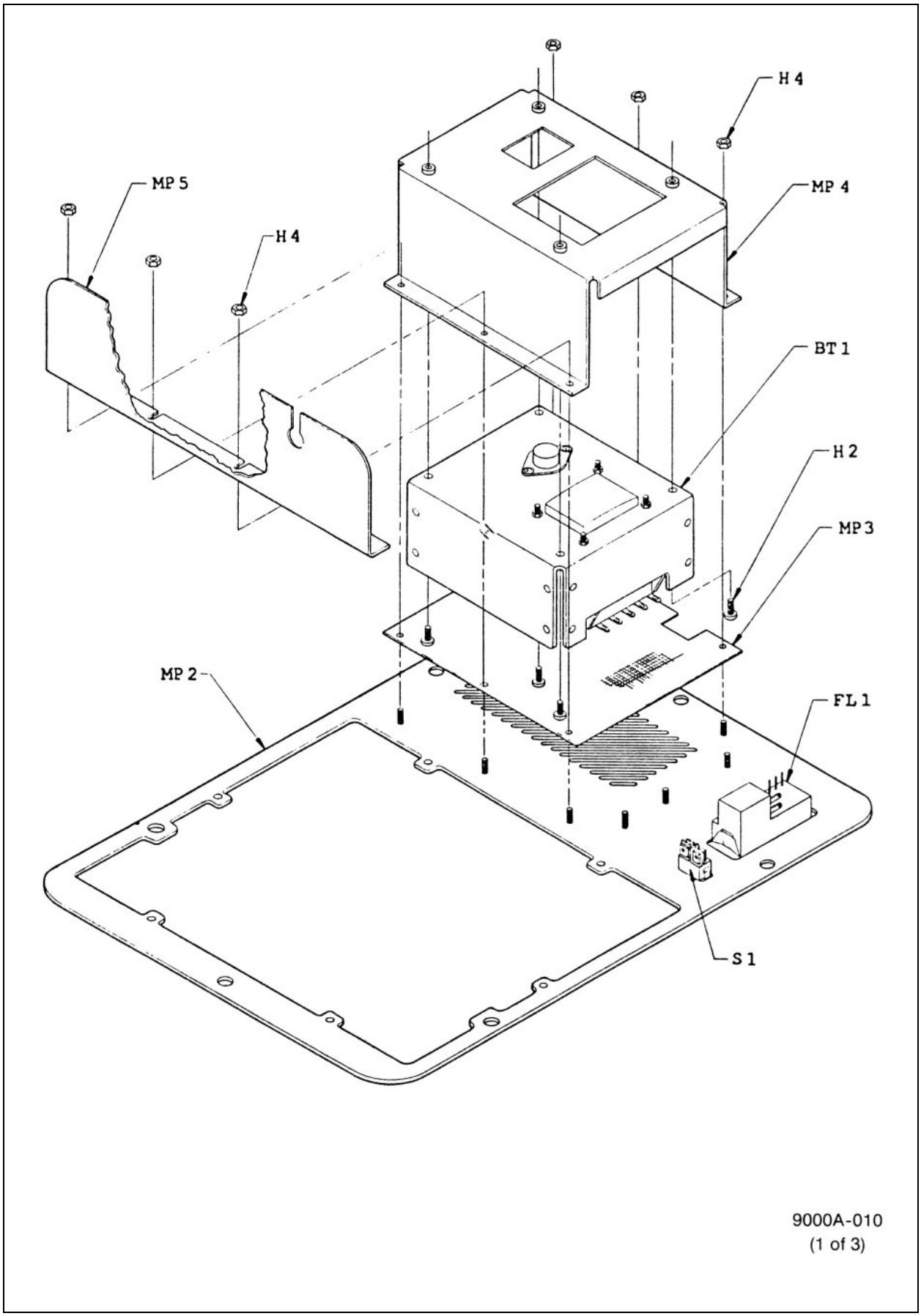


Figure 21. Demo/Trainer Final Assembly

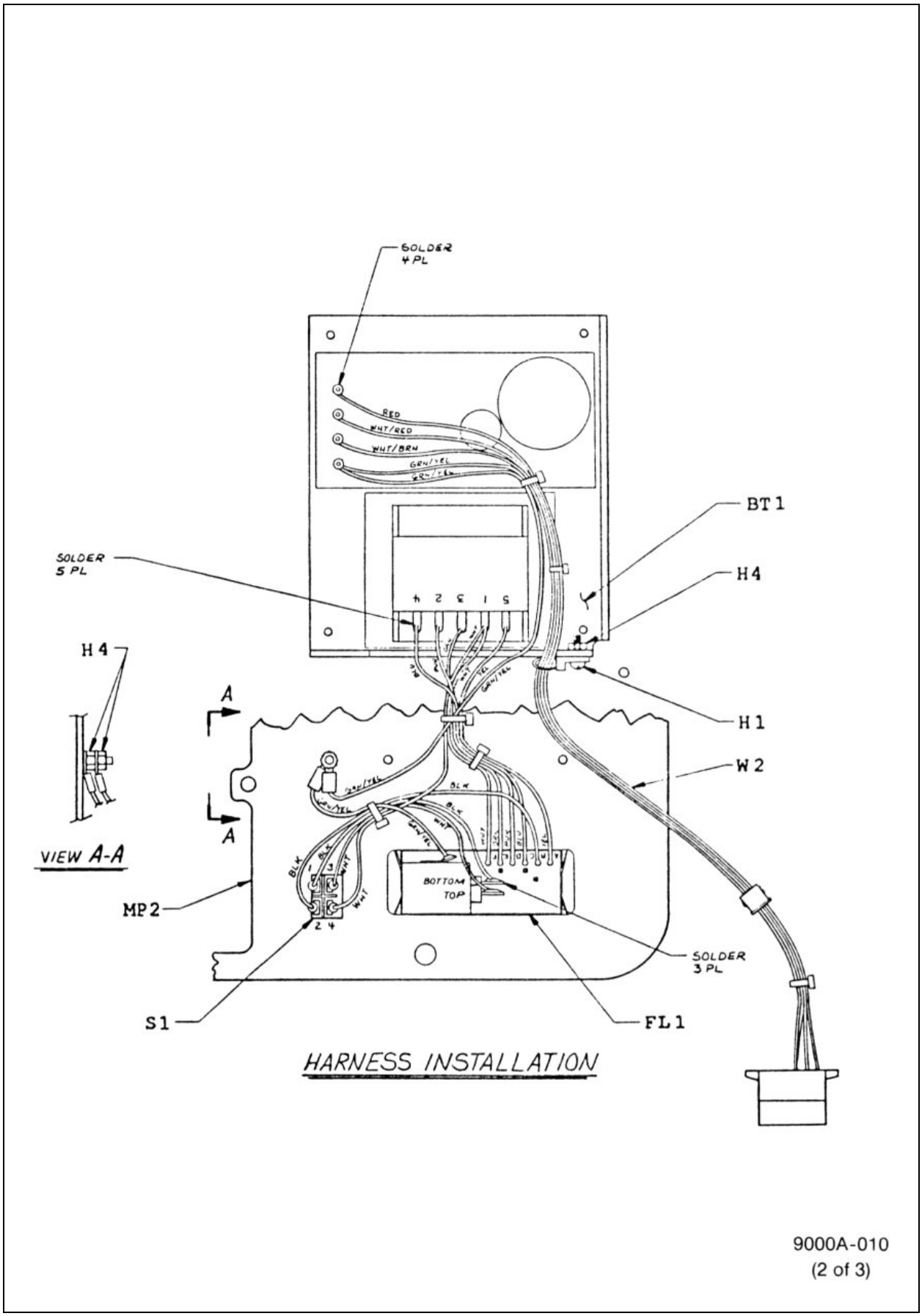


Figure 21. Demo/Trainer Final Assembly (cont)

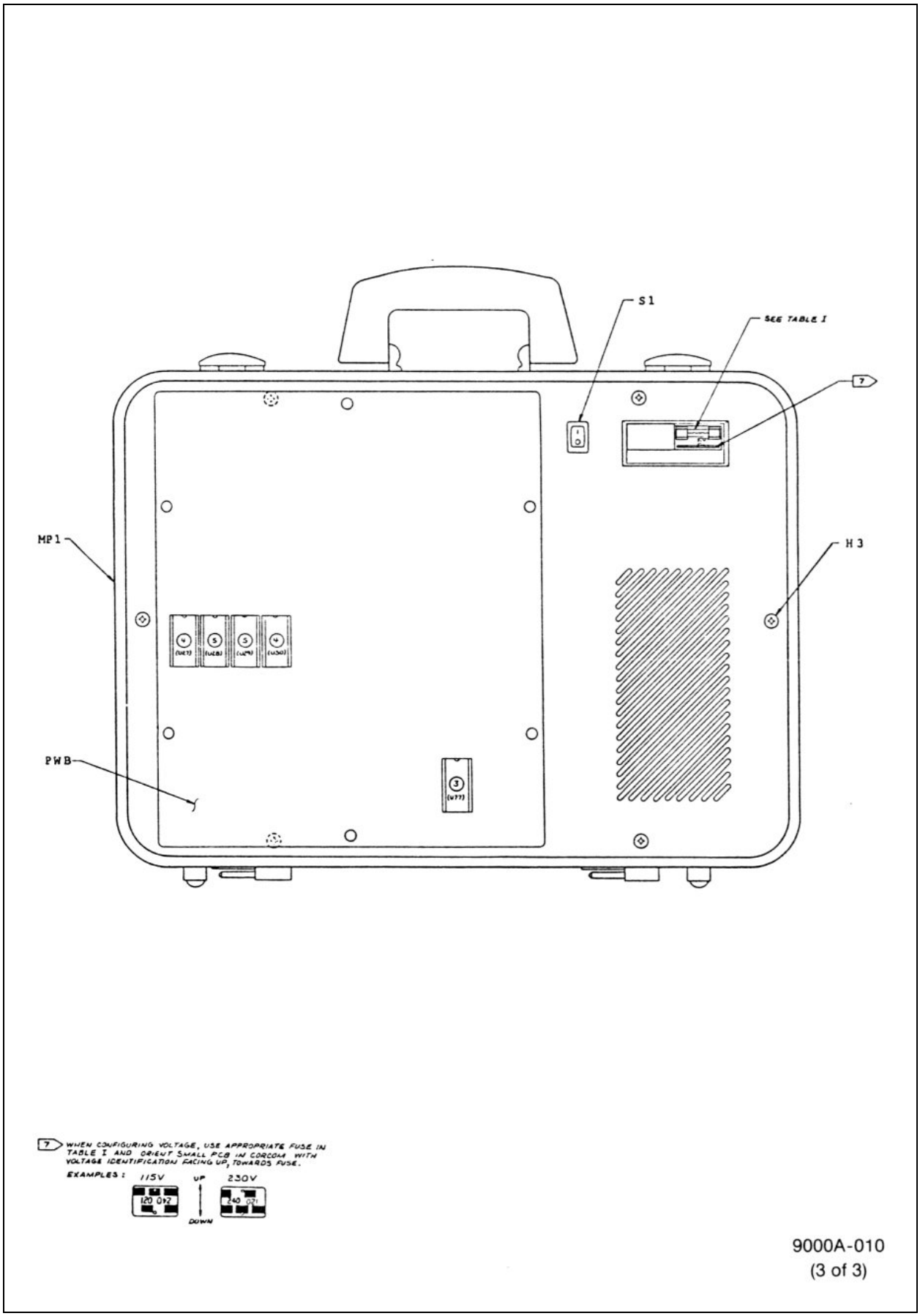


Figure 21. Demo/Trainer Final Assembly (cont)

Table 5. Demo/Trainer PWB Assembly
(See Figure 22.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N 0 T -E-
C 1		CAP,TA,3.3UF,+-20%,25V	780486	89536	780486	1		
C 4, 13		CAP,CER,0.047UF,+-20%,50V,X7R,1206	782615	89536	782615	2		
C 5		CAP,TA,10UF,+-20%,25V	772491	89536	772491	1		
C 6, 7		CAP,CER,47PF,+-10%,50V,COG,1206	747352	89536	747352	2		
C 8, 9		CAP,CER,10PF,+-10%,50V,COG,1206	747311	89536	747311	2		
C 15- 18		CAP,TA,22UF,+-20%,15V	746982	89536	746982	4		
C 21,101-132,		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	85		
C 135-183,185-			747261					
C 187			747261					
CR 1		DIODE,SI,BV=75.0V,I0=100MA,MLF	742064	89536	742064	1	1	
DS 1	*	LED,RED,LUM INT= 1 MCD,W/STANDOFFS	429555	12040	NLS5053	1	1	
H 1		SCREW,CAPTIVE,SS,6-32,21/32,WSTANDOFF	380634	89536	380634	6		
J 2		CONN,D-SUB,PWB,25 PIN	811422	89536	811422	1		
J 3		CONN,D-SUB,PWB,9 SCKT	811430	89536	811430	1		
J 4		CONN PART,MATE-N-LOK,HOUSG,REC,15 POS	339911	89536	339911	1		
J 5		SOCKET RECEPTICAL ASSY.	775981	89536	775981	1		
MP 1		KEY-TOP-"1"	639989	89536	639989	1		
MP 2		KEY-TOP-"2"	639997	89536	639997	1		
MP 3		KEY-TOP-"3"	640003	89536	640003	1		
MP 4		KEY-TOP-"4"	640011	89536	640011	1		
MP 5		KEY-TOP-RESET	639963	89536	639963	1		
MP 6		BLOCK, SPACER 68 POS	773242	89536	773242	1		
MP 7		HEAT DIS,CHIP CARRIER LID,ALUM	745851	89536	745851	1		
MP 8		CONN PART,MATE-N-LOK,JKT,0.093D,PWB	335000	89536	335000	15		
Q 1		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742676	89536	742676	1	1	
Q 2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742684	89536	742684	1	1	
R 1		RES,CHIP,CERM,910,+-5%,0.125W,1206	769257	89536	769257	1		
R 2, 3, 5-		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	89536	740522	12		
R 9, 26, 31-			740522					
R 34			740522					
R 4, 73		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	89536	746297	2		
R 10, 71		RES,CHIP,CERM,47,+-5%,0.125W,1206	746263	89536	746263	2		
R 11- 19, 23-		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	89536	746370	20		
R 25, 27- 30,			746370					
R 68, 69, 77,			746370					
R 80			746370					
R 20, 21		RES,CHIP,CERM,39K,+-5%,0.125W,1206	746677	89536	746677	2		
R 22		RES,CHIP,CERM,3K,+-5%,0.125W,1206	746511	89536	746511	1		
R 35		RES,CHIP,CERM,300,+-5%,0.125W,1206	746362	89536	746362	1		
R 41- 52		RES,CHIP,CERM,33,+-5%,0.125W,1206	746248	89536	746248	12		
R 61- 65		RES,CHIP,CERM,158,+-1%,0.125W,1206	769828	89536	769828	5	1	
R 66		RES,CHIP,CERM,5.1K,+-5%,0.125W,1206	746560	89536	746560	1		
R 67		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	89536	740506	1		
R 70		RES,CHIP,CERM,2.4K,+-5%,0.125W,1206	746495	89536	746495	1		
R 72		RES,CHIP,CERM,1.6K,+-5%,0.125W,1206	746446	89536	746446	1		
R 78, 79		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	89536	746610	2		
S 1- 4, 6		SWITCH,PUSHBUTTON,SPST KEYBOARD	513473	89536	513473	5		
S 5		SWITCH,SLIDE,SPDT	417287	95146	MSS-1040-1	1	1	
SW 1- 6		SMITCH,MODULE,SPST,DIP,8 POS	414490	00779	435166-5	6	1	
U 1	*	IC,NMOS,80286 CLOCK GENERATOR,6MHZ	783423	89536	783423	1	1	
U 2, 16, 22,	*	IC,LSTTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	4	1	
U 76			473223					
U 3, 23	*	IC,ALSTTL,OCTAL BUS XCVR W/3-STATE	647214	01295	SN74ALS245N	2	1	
U 4, 63	*	IC,ALSTTL,QUAD 2 INPUT AND GATE,SOIC	741827	89536	741827	2	1	
U 5, 24, 58	*	IC,ALSTTL,QUAD 2 INPUT NAND GATE,SOIC	782268	89536	782268	3		
U 6, 79	*	IC,LSTTL, 8 INPUT NAND GATE	404889	01295	SN74LS30N	2	1	
U 7, 25	*	IC,FTTL,DUAL JK F/F,-EDG TRIG	781211	89536	781211	2	1	
U 8, 9, 21	*	IC,ALSTTL,3-8 LINE DCDR W/ENABLE,SOIC	741686	89536	741686	3	1	
U 10, 86, 87	*	IC,LSTTL,OCTAL D TRANSPARENT LATCHES	504514	01295	SN74LS373N	3	1	
U 11	*	IC,NMOS,DUAL ASYN RECVR/TRANS,PLCC	742999	89536	742999	1	1	
U 12	*	IC,CMOS,DUAL RS-232 TRANS/RECEIVER,5V	799445	89536	799445	1	1	
U 13	*	IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	01295	SN74LS14N	1	1	
U 14	*	IC,NMOS,16-BIT MPU, 6MHZ,LCC	782813	89536	782813	1		
U 15	*	IC,NMOS,80286 BUS CONTROLLER,6MHZ	783431	89536	783431	1	1	
U 17, 43	*	IC,LSTTL,8BIT S-IN, P-OUT R-SHIFT RGS	408732	01295	SN74LS164N	2	1	
U 18		OSCILLATOR,31.9399 MHZ,TTL CLOCK	800029	89536	800029	1		
U 19, 57	*	IC,ALSTTL,HEX INVERTERS,SOIC	782300	89536	782300	2	1	
U 20	*	IC,LSTTL,8 TO 3 LINE ENCODER,SOIC	782326	89536	782326	1	1	
U 26	*	IC,LSTTL,QUAD BUS BFR W/3-STATE OUT	472746	01295	SN74LS125N	1	1	
U 31	*	IC,NMOS,PROGRMBL PERIPHERAL INTERFACE	723536	89536	723536	1	1	

An * in 'S' column indicates a static-sensitive part.

Table 5. Demo/Trainer PWB Assembly (cont)

REFERENCE DESIGNATOR -A->-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N 0 T -E-
U 69	*		429035					
U 33, 47	*	DIODE,LED,RED,7 SEGMENT,NUMERIC	495440	28480	QDSP3515	2		
U 34- 41, 48-	*	IC,64K X 1 DYN RAM, l28/2MS REFRESH	721944	89536	721944	16	1	
U 55	*		721944					
U 42	*	IC,LSTTL,DUAL DIV BY 2, 5 CNTR,SOIC	741967	89536	741967	1	1	
U 44	*	IC,ALSTTL,DUAL D F/F,+EDG TRG,SOIC	742452	89536	742452	1		
U 45	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	1	
U 56	*	IC,ALSTTL,TRIPLE 3 INPUT NAND GATE	740886	89536	740886	1	1	
U 59	*	IC,LSTTL,DUAL J-F F/F,+EDG TRIG,SOIC	742502	89536	742502	1	1	
U 60	*	IC,LSTTL,DELAY ELEMENTS,SOIC	773077	89536	773077	1	1	
U 61, 70, 71	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	3	5	
U 62	*	IC,LSTTL,HEX INVERTER,SOIC	741017	89536	741017	1	1	
U 64	*	IC,ALSTTL,QUAD 2 INPUT NOR GATE,SOIC	782284	89536	782284	1	1	
U 65, 66	*	IC,FTTL,QUAD,2-INPUT MULTIPLEXER	647156	01295	74F257PC	2	1	
U 67	*	IC,LSTTL,8-BIT BINARY CNTR W/REG-OUT	741173	89536	741173	1	1	
U 72	*	IC,NMOS,ADVANCED VIDEO DISPLAY CNTRLR	742775	89536	742775	1		
U 73, 83, 84	*	IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	89536	773028	3	1	
U 74, 85	*	IC, 2K X 8 STAT RAM	584144	33297	uPD4016C-2	2		
U 75	*	IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR	393215	01295	SN74LS175N	1	1	
U 78	*	IC,BIPOIAR,COLOR/MONO.ATTRI.CONTROLR	742767	89536	742767	1	1	
U 80, 81	*	IC,LSTTL,TRIPLE 3 INPUT NAND GATE	393074	01295	SN74LS10N	2	1	
U 82	*	IC,STTL,QUAD D F/F,+EDG TRG,SOIC	742700	89536	742700	1	1	
U 88	*	IC,STTL,QUAD 2 INPUT XOR GATE	379297	01295	SN74S86N	1	1	
XU 14		SOCKET,IC,CHIP CARRIER,68 PIN,0.100	720888	89536	720888	1		
XU 18		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
XU 27- 30, 77		SOCKET,IC,28 PIN	448217	91506	328-AG39D	5		
XU 31, 72, 78		SOCKET,IC,40 PIN	429282	09922	DILB40P-108	3		
XU 34- 41, 48-		SOCKET,IC,16 PIN	276535	91506	316-AG39D	17		
XU 55, 3			276535					
XU 74, 85		SOCKET,IC,24 PIN	376236	91506	324-AG39D	2		
Y 1		CRYSTAL,3.6864MHZ,+/-50PPM,SURF.MNT.	800193	89536	800193	1		
Z 1		RES,NET,SIP,10 PIN,9 RES,4.7K,+-2%	484063	80031	95081002CL	1	1	

An * in 'S' column indicates a static-sensitive part.

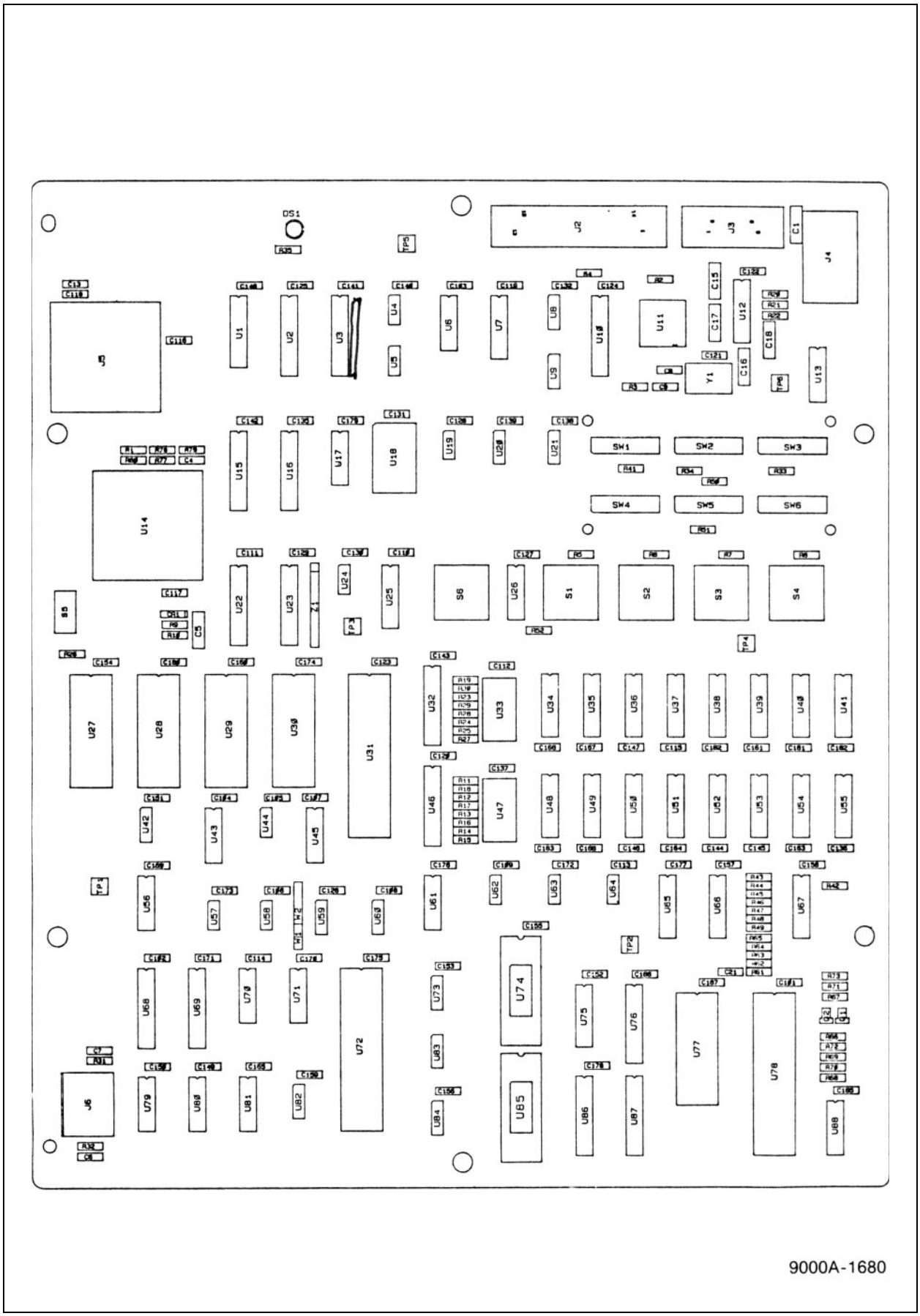


Figure 22. Demo/Trainer PWB Assembly

Table 6. Demo/Trainer Mnemonics

AB00-10	Address lines for Video RAM. Can be sourced by microprocessor (IA01-11) or video controller (DADD00-10) via U73, U83, and U84 multiplexers.
ADDRBUS	Main address bus (IA00-15) used by microprocessor.
ALATCH	Address valid signal used for valid address timing.
CAS-	Column address select, used to enable column addressing of dynamic RAM.
CLK (8 MHZ)	The clock source. In the Demo/Trainer, a 31.9399 MHz clock source divided by four is used by the microprocessor.
DADD00-15	The bus used by the Video Controller in addressing Video RAM.
DATABUS	The main data bus (ID00-15) used throughout the Demo/Trainer.
DB00-15	The data bus used by the data output circuit of Video RAM.
HLDA	Hold acknowledge. The microprocessor has acknowledged the hold state set by the RUN-TEST switch (S5). HLDA is supplied to the pod test connector.
HSYNC	Horizontal sync for video output.
I/OINT-	I/O interrupt, generated by DUART servicing RS-232 and keyboard ports.
I/OSLT-	I/O select, enables DUART servicing I/O ports.
IA00	Used to determine even or odd byte on the 16-bit address bus.
IA00-15	Main address bus (addrbus)
IBHE-	Bus high enable (buffered).
IC0D/INTA-	Distinguishes instruction fetch cycles from memory read cycles. Also distinguishes interrupt acknowledge cycles from I/O.
ID00-15	Main data bus (databus)
IM/IO	Memory/I/O to address decode (distinguishes memory accesses from I/O accesses.
INTA	Interrupt acknowledge from the 82288.
INTR	Interrupt input.
INTRDY-	Interrupt ready.
IPOLL-	Interrupt poll.
IREAD-	Internal read.

Table 6. Demo/Trainer Mnemonics (cont)

IWRITE-	Internal write.
PCLK	Processor clock: 50% duty cycle, with 1/2 frequency of main clock.
PPISLT-	Programmable peripheral interface select.
RAM0-	Main RAM select.
RAM1-	Main RAM select.
RAMRDY-	RAM ready for read or write by microprocessor.
RASS-	Row address select, used to enable row addressing of dynamic RAM.
READ-	Memory read command.
READY-	Ready signal to microprocessor.
RESET	External reset (S6) to microprocessor, PIA, pod test connector, DUART, and video timing circuits.
ROM0-	ROM 0 (U29, U30) select.
ROM0RDY-	ROM 0 ready for read.
ROM1-	ROM 1 (U27, U28) select.
ROM1RDY-	ROM 1 ready for read.
SELECTA-	Video RAM address decode and RAM enable.
TIMER-	DUART (U11) output used for start of each interrupt (100 ms period).
VIDEO	Video output.
VIDSLT-	Video select.
VRAM-	Video RAM select. Used to time microprocessor access to video RAM.
VRAMRDY-	Video RAM ready. Microprocessor can now access video RAM.
VSYNC	Vertical sync for video output.
WRITE-	Memory write command.

Table 7. I/O Initialization Procedure

PIA INITIALIZATION

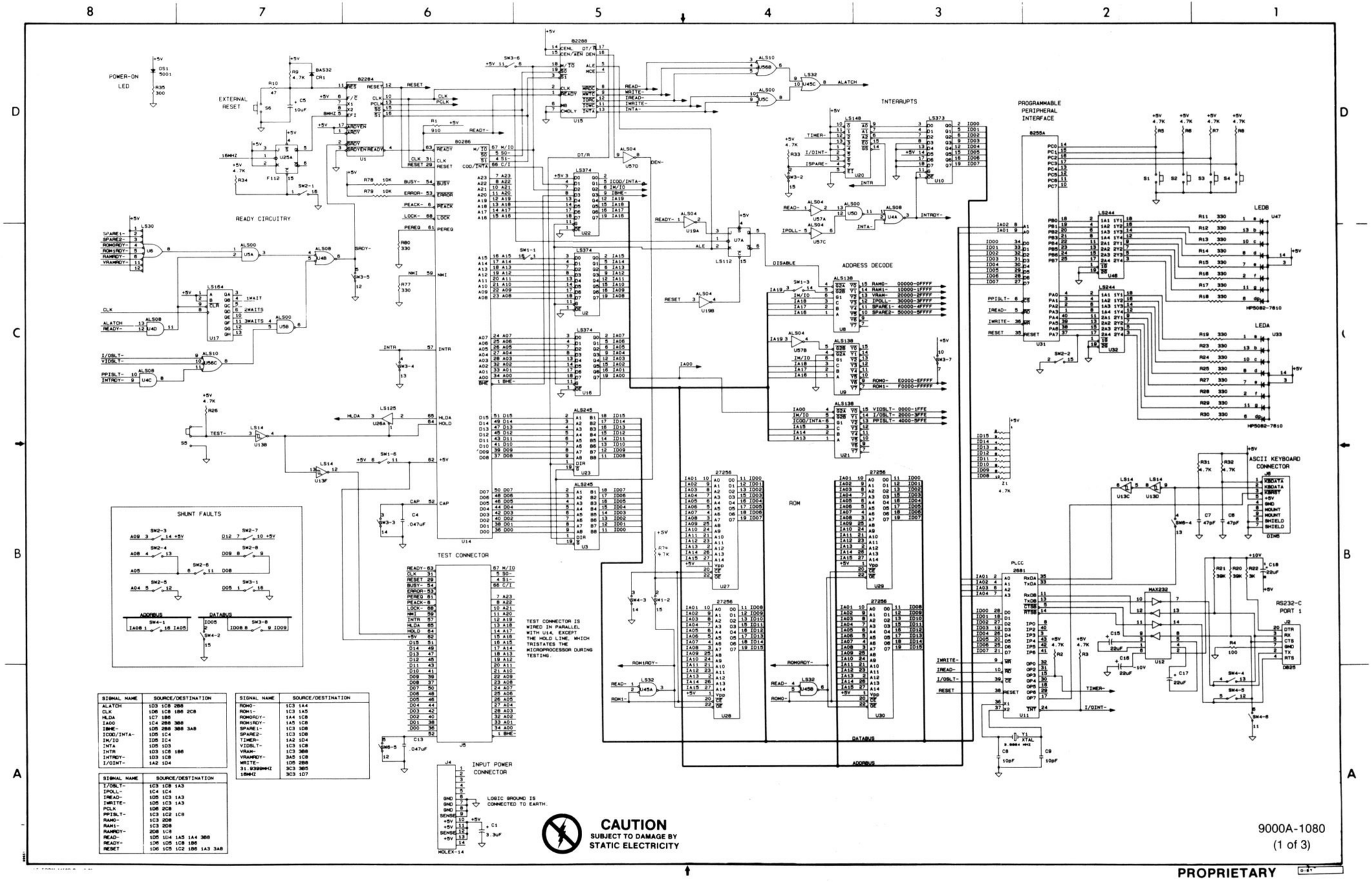
I/O Address	PIA Access Using I/O Byte Addresses (8255A)
WRITE 4006 = 89	Set PIA Ports A and B to output, Port C to input
WRITE 4000 = FF	Output to Port A
WRITE 4002 = FF	Output to Port B

UART INITIALIZATION

I/O Address	UART Access Using I/O Byte Addresses (SCN2681)
WRITE 2004 = 2A	CRA
WRITE 2004 = 3A	CTUR
WRITE 2004 = 49	
WRITE 2014 = 2A	
WRITE 2014 = 3A	
WRITE 2014 = 45	
WRITE 2000 = 13	MR1A
WRITE 2000 = 07	MR1B
WRITE 2010 = 13	CSRA
WRITE 2010 = 07	OPCR
WRITE 2002 = 66	
WRITE 2012 = BB	
WRITE 201A = 00	
WRITE 201E = FF	
WRITE 201C = 80	Set output port
WRITE 201E = FF	Reset output port, reset keyboard
	Setup for the counter/timer follows
WRITE 200C = 00	CTUR Setup Port RxDB to cause interrupt
WRITE 200E = 78	CTLR when character received
WRITE 201A = 04	Set OPCR
WRITE 2008 = 10	CACR
READ 201C	Start count

VIDEO INITIALIZATION

I/O Address	Video Access Using I/O Byte Addresses (SCN2674)
WRITE 0002 = 00	
WRITE 0002 = 00	
WRITE 0000 = 48	
WRITE 0000 = 20	
WRITE 0000 = 22	
WRITE 0000 = 86	
WRITE 0000 = l7	
WRITE 0000 = 4F	
WRITE 0000 = 09	
WRITE 0000 = 28	
WRITE 0000 = 00	
WRITE 0000 = 10	
WRITE 0000 = 00	
WRITE 0000 = 00	
WRITE 0000 = 00	
WRITE 0000 = 00	
WRlTE 0000 = 00	
WRITE 0004 = 01	
WRITE 0006 = 00	
WRITE 0008 = 00	
WRITE 000A = 00	
WRITE 000C = 00	
WRITE 000E = 00	
WRITE 0002 = 29	
WRITE 0002 = 31	

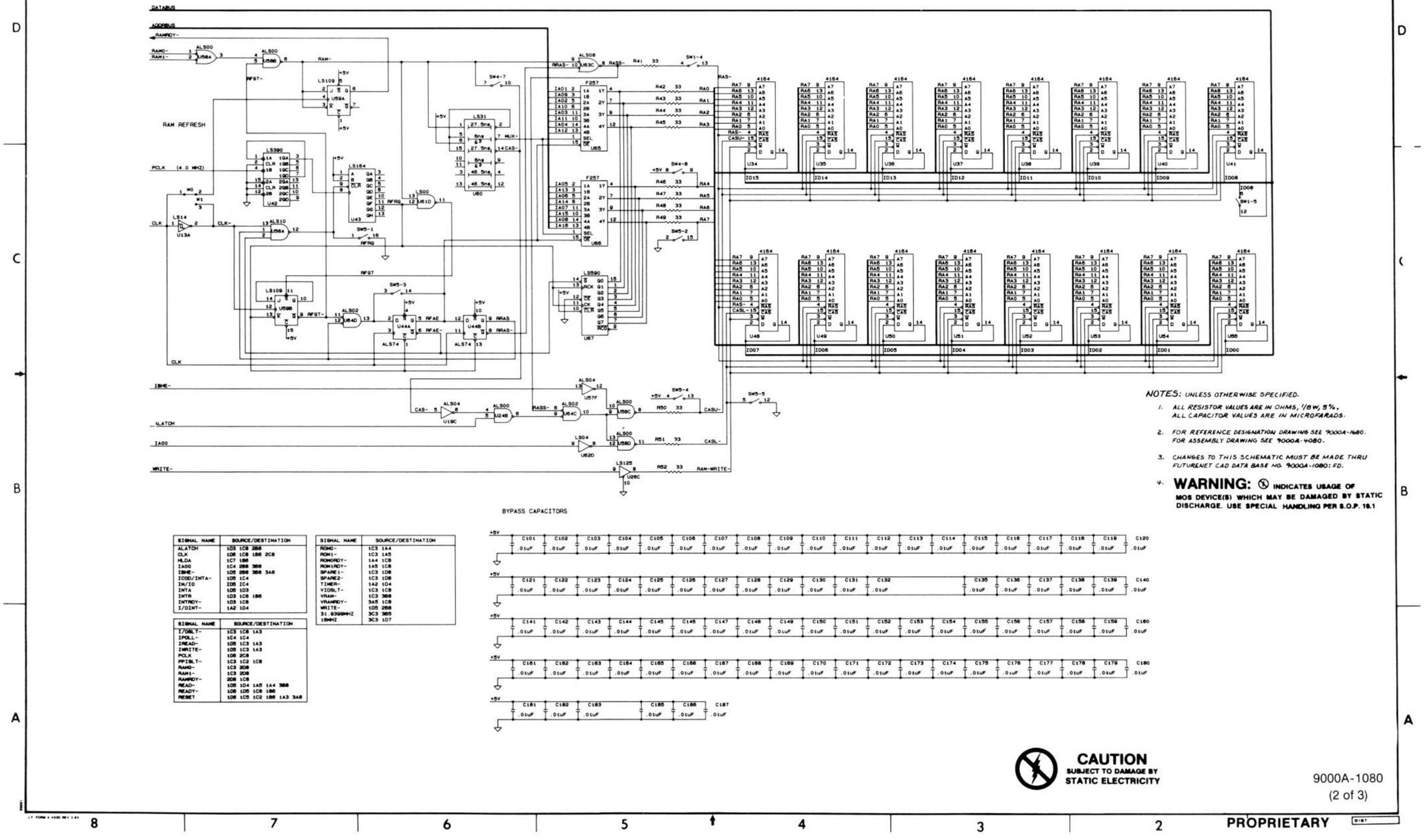


SIGNAL NAME	SOURCE/DESTINATION
ALATCH	1D3 1C8 2B8
CLK	1D6 1C8 1B6 2C8
HLDA	1C7 1B6
IA00	1C4 2B8 3B8
IBHE-	1D5 2B8 3B8 3A8
ICOD/INTA-	1D5 1C4
IM/IO	1D5 1C4
INTA	1D5 1D3
INTR	1D3 1C8 1B6
INTRDY-	1D3 1C8
I/OINT-	1A2 1D4

SIGNAL NAME	SOURCE/DESTINATION
I/OSLT-	1C3 1C8 1A3
IPOLL-	1C4 1C4
IREAD-	1D5 1C3 1A3
IWRITE-	1D5 1C3 1A3
PCLK	1D6 2C8
PPISLT-	1C3 1C2 1C8
RAM0-	1C3 2D8
RAM1-	1C3 2D8
RAMRDY-	2D8 1C8
READ-	1D5 1D4 1A5 1A4 3B8
READY-	1D6 1D5 1C8 1B6
RESET	1D6 1C5 1C2 1B6 1A3 3A8

SIGNAL NAME	SOURCE/DESTINATION
ROM0-	1C3 1A4
ROM1-	1C3 1A5
ROMORDY-	1A4 1C8
ROM1RDY-	1A5 1C8
SPARE1-	1C3 1D8
SPARE2-	1C3 1D8
TIMER-	1A2 1D4
VIDSLT-	1C3 1C8
VRAM-	1C3 3B8
VRAMRDY-	3A5 1C8
WRITE-	1D5 2B8
31.9392MHZ	3C3 3B5
18MHZ	3C3 1D7

Figure 23. Demo/Trainer PWB Assembly



SIGNAL NAME	SOURCE/DESTINATION
ALATCH	1D3 1C8 2B8
CLK	1D6 1C8 1B6 2C8
HLDA	1C7 1B6
IA00	1C4 2B8 3B8
IBHE-	1D5 2B8 3B8 3A8
IO00/INTA-	1D5 1C4
IM/IO	1D5 1C4
INTA	1D5 1D3
INTR	1D3 1C8 1B6
INTRDY-	1D3 1C8
I/OINT-	1A2 1D4

SIGNAL NAME	SOURCE/DESTINATION
I/OBLT-	1C3 1C8 1A3
IPOLL-	1C4 1C4
IREAD-	1D5 1C3 1A3
IWRITE-	1D5 1C3 1A3
PCLK	1D6 2C8
PPIBLT-	1C3 1C2 1C8
RAM0-	1C3 2D8
RAM1-	1C3 2D8
RAMRDY-	2D8 1C8
READ-	1D5 1D4 1A5 1A4 3B8
READY-	1D8 1D5 1C8 1B6
RESET	1D8 1C5 1C2 1B6 1A3 3A8

SIGNAL NAME	SOURCE/DESTINATION
ROM0-	1C3 1A4
ROM1-	1C3 1A5
ROMRDY-	1A4 1C8
ROM1RDY-	1A5 1C8
SPARE1-	1C3 1D8
SPARE2-	1C3 1D8
TIMER-	1A2 1D4
VIOSLT-	1C3 1C8
VRAM-	1C3 3B8
VRAMRDY-	3A5 1C8
WRITE-	1D5 2B8
31.939MHZ	3C3 3B5
15MHZ	3C3 1D7

Figure 23. Demo/Trainer PWB Assembly (cont)

ADVANCED VIDEO DISPLAY CONTROLLER

COLOR/MONOCHROME ATTRIBUTES CONTROLLER

OSCILLATOR 32MHZ

Note: oscillator is really 31.9399MHz

REF DES	DEVICE	+5V	GND	PACKAGE	QTY
U1	82284	18	9	DIP	1
U2, 15, 22, 76	74LS374	20	10	DIP	4
U3, 23	74ALS245	20	10	DIP	2
U4, 83	74ALS08	14	7	SO	2
U5, 24, 58	74ALS00	14	7	SO	3
U6, 79	74LS30	14	7	DIP	2
U7	74LS112	16	8	DIP	2
U8, 9, 21	74ALS138	16	8	SO	3
10, 86, 87	74LS373	20	10	DIP	
U11	2681	44	22	PLCC	1
U12	MAX232	16	15	DIP	1
U13	74LS14	14	7	DIP	1
U14	82286	30	60	LCC	1
U15	82288	20	10	DIP	1
U17, 43	74LS184	14	7	DIP	2
U18	OSCILLATOR	14	7	DIP	1
U19, 57	74ALS04	14	7	SO	2
U20	74LS148	16	8	SO	1
U25	74F112	16	8	DIP	2
U26	74LS125	14	7	DIP	3
U27-30	27256	28	14	DIP	4
U31	8255	26	7	DIP	1
U32, 46, 66, 69	74LS244	20	10	DIP	4
U33, 47	7-SEG LED	NN	NN	DIP	2

REF DES	DEVICE	+5V	GND	PACKAGE	QTY
U34-41, U48-55	4164-15	8	16	DIP	16
U42	74LS390	16	8	SO	1
U44	74ALS74	14	7	SO	1
U45	74LS32	14	7	DIP	1
U56	74ALS10	14	7	DIP	1
U59	74LS109	16	8	SO	1
U60	74LS31	16	8	SO	1
U61, 70, 71	74LS00	14	7	DIP	3
U62	74LS04	14	7	SO	1
U64	74ALS02	14	7	SO	1
U65, U66	74F257	16	8	DIP	2
U67	74LS590	16	8	DIP	1
U72	2674	40	20	DIP	1
U73, 83, 84	74F157	16	8	SO	3
U74, 85	2018	24	12	DIP	2
U75	74LS175	16	8	DIP	1
U77	27128A-150 CR	28	14	DIP	1
U78	2675	40	20	DIP	1
U80, 81	74LS10	14	7	DIP	2
U82	74S175	16	8	SO	1
U88	74S86	14	7	DIP	1
DS1	LDR 5001	NN	NN	XXXX	1
Z1	4.7K	1	NN	SIP	1

SPARES

SIGNAL NAME	SOURCE/DESTINATION
ALATCH	1D3 1C8 2B8
CLK	1D6 1C8 1B6 2C8
HLDA	1C7 1B6
IA00	1C4 2B8 3B8
IBHE-	1D5 2B8 3B8 3A8
ICOD/INTA-	1D5 1C4
IM/IO	1D5 1C4
INTA	1D5 1D3
INTR	1D3 1C8 1B6
INTRDY-	1D3 1C8
I/OINT-	1A2 1D4

SIGNAL NAME	SOURCE/DESTINATION
I/OBLT-	1C3 1C8 1A3
IPOLL-	1C4 1C4
IREAD-	1D5 1C3 1A3
IWRITE-	1D5 1C3 1A3
PCLK	1D6 2C8
PPIBLT-	1C3 1C2 1C8
RAM0-	1C3 2D8
RAM1-	1C3 2D8
RAMRDY-	2D8 1C8
READ-	1D5 1D4 1A5 1A4 3B8
READY-	1D6 1D5 1C8 1B6
RESET	1D6 1C5 1C2 1B6 1A3 3A8

SIGNAL NAME	SOURCE/DESTINATION
ROM0-	1C3 1A4
ROM1-	1C3 1A5
ROMRDY-	1A4 1C8
ROM1RDY-	1A5 1C8
SPARE1-	1C3 1D8
SPARE2-	1C3 1D8
TIMER-	1A2 1D4
VIDBLT-	1C3 1C8
VRAM-	1C3 3B8
VRAMRDY-	3A5 1C8
WRITE-	1D5 2B8
31.9399MHZ	3C3 3B5
16MHZ	3C3 1D7

CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

9000A-1080
(3 of 3)

PROPRIETARY

Figure 23. Demo/Trainer PWB Assembly (cont)