Continuously Variable Slope Delta Modulator/Demodulator

Providing a simplified approach to digital speech encoding/decoding, the MC3418 CVSD is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I²L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable (VCC/2 Reference Provided On–Chip)
- MC3418 has a 4–Bit Algorithm (Commercial Telephone)

Representative Block Diagram

This device contains 144 active transistors.
# MAXIMUM RATINGS

(All voltages referenced to \( V_{EE} \), \( T_A = 25^\circ C \), unless otherwise noted.)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>( V_{CC} )</td>
<td>(-0.4 ) to (+18 )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Differential Analog Input Voltage</td>
<td>( V_I )</td>
<td>( \pm 5.0 )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Digital Threshold Voltage</td>
<td>( V_{TH} )</td>
<td>(-0.4 ) to ( V_{CC} )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Logic Input Voltage</td>
<td>( V_{Logic} )</td>
<td>(-0.4 ) to (+18 )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Coincidence Output Voltage</td>
<td>( V_{O(Con)} )</td>
<td>(-0.4 ) to (+18 )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Syllabic Filter Input Voltage</td>
<td>( V_I(Syl) )</td>
<td>(-0.4 ) to ( V_{CC} )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Gain Control Input Voltage</td>
<td>( V_I(GC) )</td>
<td>(-0.4 ) to ( V_{CC} )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Reference Input Voltage</td>
<td>( V_{I(ref)} )</td>
<td>( V_{CC}/2 ) – ( 1.0 ) to ( V_{CC} )</td>
<td>Vdc</td>
</tr>
<tr>
<td>( V_{CC}/2 ) Output Current</td>
<td>( I_{ref} )</td>
<td>(-25 )</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTE:** ESD data available upon request.

## ELECTRICAL CHARACTERISTICS

(\( V_{CC} = 12 \) V, \( V_{EE} = Gnd \), \( T_A = 0 \) to \( 70^\circ C \), unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage Range (Figure 1)</td>
<td>( V_{CCR} )</td>
<td>4.75</td>
<td>12</td>
<td>16.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>Power Supply Current (Figure 1) @ Idle Channel</td>
<td>( I_{CC} )</td>
<td>–</td>
<td>3.7</td>
<td>5.5</td>
<td>mA</td>
</tr>
<tr>
<td>Gain Control Current Range (Figure 2)</td>
<td>( I_{GCR} )</td>
<td>0.002</td>
<td>–</td>
<td>3.0</td>
<td>mA</td>
</tr>
<tr>
<td>Analog Comparator Input Range (Pins 1 and 2)</td>
<td>( V_I )</td>
<td>1.3</td>
<td>–</td>
<td>( V_{CC} – 1.3 )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Analog Output Range (Pin 7)</td>
<td>( V_O )</td>
<td>1.3</td>
<td>–</td>
<td>( V_{CC} – 1.3 )</td>
<td>Vdc</td>
</tr>
<tr>
<td>Input Bias Currents (Figure 3)</td>
<td>( I_{IB} )</td>
<td>–</td>
<td>0.25</td>
<td>1.0</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Comparator in Active Region</td>
<td>( I_{IO} )</td>
<td>–</td>
<td>0.05</td>
<td>0.4</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Analog Input (I1)</td>
<td>–</td>
<td>0.25</td>
<td>1.0</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Analog Feedback (I2)</td>
<td>–</td>
<td>0.06</td>
<td>0.3</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Syllabic Filter Input (I3)</td>
<td>–</td>
<td>–0.06</td>
<td>–0.3</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Reference Input (I5)</td>
<td>–</td>
<td>–0.06</td>
<td>–0.3</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Analog Input/Analog Feedback</td>
<td>( I_{11} ) – ( I_{12} ) (Figure 3)</td>
<td>–</td>
<td>0.05</td>
<td>0.4</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Analog Input/Analog Feedback</td>
<td>( I_{15} ) – ( I_{16} ) (Figure 4)</td>
<td>–</td>
<td>0.01</td>
<td>0.1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( V_{IO} )</td>
<td>–</td>
<td>2.0</td>
<td>6.0</td>
<td>mV</td>
</tr>
<tr>
<td>V/I Converter (Pins 3 and 4) (Figure 5)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>mA/mV</td>
</tr>
<tr>
<td>Transconductance</td>
<td>( g_m )</td>
<td>0.1</td>
<td>0.3</td>
<td>–</td>
<td>mA/mV</td>
</tr>
<tr>
<td>V/I Converter, 0 to 3.0 mA</td>
<td>–</td>
<td>1.0</td>
<td>10</td>
<td>–</td>
<td>mA/mV</td>
</tr>
<tr>
<td>Integrator Amplifier, 0 to ( \pm 5.0 ) mA Load</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>mA/mV</td>
</tr>
<tr>
<td>Propagation Delay Times (Note 1)</td>
<td>( t_{PLH} )</td>
<td>–</td>
<td>1.0</td>
<td>2.5</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Clock Trigger to Digital Output</td>
<td>( C_L = 25 ) pF to Gnd</td>
<td>–</td>
<td>0.8</td>
<td>2.5</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Clock Trigger to Coincidence Output</td>
<td>( C_L = 25 ) pF to Gnd, ( R_L = 4.0 ) kΩ to ( V_{CC} )</td>
<td>–</td>
<td>1.0</td>
<td>3.0</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Coincidence Output Voltage – Low Logic Stage</td>
<td>( V_{O(Con)} )</td>
<td>–</td>
<td>0.12</td>
<td>0.25</td>
<td>Vdc</td>
</tr>
</tbody>
</table>

**NOTES:**
1. All propagation delay times measured 50% to 50% from the negative going (from \( V_{CC} \) to \(+0.4 \) V) edge of the clock.
2. Dynamic total loop offset (\( V_{O(Con)} \)) equals \( V_{IO} \) (comparator) (Figure 3) minus \( V_{IOX} \) (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the \( 10 \) kΩ integrator resistor. The clock frequency is \( 32 \) kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one–half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to ensure good idle channel performance.
### ELECTRICAL CHARACTERISTICS (continued)  
(V<sub>CC</sub> = 12 V, V<sub>EE</sub> = Gnd, T<sub>A</sub> = 0 to 70°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coincidence Output Leakage Current – High Logic State</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt;(Con)</td>
<td>–</td>
<td>0.01</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt; = 15 V, 0°C ≤ T&lt;sub&gt;A&lt;/sub&gt; ≤ 70°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Applied Digital Threshold Voltage Range (Pin 12)</td>
<td>V&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>1.2</td>
<td>–</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; – 2.0</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Digital Threshold Input Current</td>
<td>I&lt;sub&gt;(th)&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>5.0</td>
<td>µA</td>
</tr>
<tr>
<td>1.2 V ≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt; – 2.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt; Applied to Pins 13, 14 and 15</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>–50</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt; Applied to Pins 13, 14 and 15</td>
<td>–</td>
<td></td>
<td>–10</td>
<td>–50</td>
<td></td>
</tr>
<tr>
<td>Maximum Integrator Amplifier Output Current</td>
<td>I&lt;sub&gt;O&lt;/sub&gt;</td>
<td>±5.0</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; /2 Generator Maximum Output Current (Source Only)</td>
<td>I&lt;sub&gt;ref&lt;/sub&gt;</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; /2 Generator Output Impedance (4.75 V ≤ V&lt;sub&gt;CC&lt;/sub&gt; ≤ 16.5 V)</td>
<td>z&lt;sub&gt;ref&lt;/sub&gt;</td>
<td>–</td>
<td>3.0</td>
<td>6.0</td>
<td>Ω</td>
</tr>
<tr>
<td>Logic Input Voltage (Pins 13, 14 and 15)</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>V&lt;sub&gt;th&lt;/sub&gt; – 0.4</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Low Logic State</td>
<td>V&lt;sub&gt;H&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>V&lt;sub&gt;th&lt;/sub&gt; + 0.4</td>
<td>–10</td>
</tr>
<tr>
<td>High Logic State</td>
<td>–</td>
<td>–</td>
<td>1.3</td>
<td>±4.3</td>
<td></td>
</tr>
<tr>
<td>Dynamic Total Loop Offset Voltage (Note 2) (Figures 3, 4 and 5)</td>
<td>ΣV&lt;sub&gt;offset&lt;/sub&gt;</td>
<td>–</td>
<td>±0.5</td>
<td>±3.0</td>
<td>mV</td>
</tr>
<tr>
<td>I&lt;sub&gt;GCl&lt;/sub&gt; = 12 µA, V&lt;sub&gt;CC&lt;/sub&gt; = 12 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0°C ≤ T&lt;sub&gt;A&lt;/sub&gt; ≤ +70°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;GCl&lt;/sub&gt; = 12 µA, V&lt;sub&gt;CC&lt;/sub&gt; = 5.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0°C ≤ T&lt;sub&gt;A&lt;/sub&gt; ≤ +70°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital Output Voltage</td>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>–</td>
<td>0.1</td>
<td>0.4</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = –0.35 mA</td>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; – 0.2</td>
<td>–</td>
</tr>
<tr>
<td>Syllabic Filter Applied Voltage (Pin 3) (Figure 2)</td>
<td>V&lt;sub&gt;(Syl)&lt;/sub&gt;</td>
<td>3.2</td>
<td>–</td>
<td>–</td>
<td>V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>Integrating Current (Figure 2)</td>
<td>I&lt;sub&gt;IInt&lt;/sub&gt;</td>
<td>8.0</td>
<td>10</td>
<td>12</td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;GCl&lt;/sub&gt; = 12 µA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;GCl&lt;/sub&gt; = 1.5 mA</td>
<td>1.42</td>
<td>1.5</td>
<td>1.58</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;GCl&lt;/sub&gt; = 3.0 mA</td>
<td>2.75</td>
<td>3.0</td>
<td>3.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Dynamic Integrating Current Match (Figure 6)</td>
<td>V&lt;sub&gt;O(Ave)&lt;/sub&gt;</td>
<td>–</td>
<td>±100</td>
<td>±280</td>
<td>mV</td>
</tr>
<tr>
<td>I&lt;sub&gt;IH&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current – High Logic State (V&lt;sub&gt;IH&lt;/sub&gt; = 18 V)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Digital Data Input</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Encode/Decode Input</td>
<td>–</td>
<td>–</td>
<td>5.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Input Current – Low Logic State (V&lt;sub&gt;IL&lt;/sub&gt; = 0 V)</td>
<td>I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>µA</td>
</tr>
<tr>
<td>Digital Data Input</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Clock Input</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Encode/Decode Input</td>
<td>–</td>
<td>–</td>
<td>36</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Clock Input, V&lt;sub&gt;IL&lt;/sub&gt; = 0.4 V</td>
<td></td>
<td>–</td>
<td>–72</td>
<td>–</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. All propagation delay times measured 50% to 50% from the negative going (from V<sub>CC</sub> to +0.4 V) edge of the clock.
2. Dynamic total loop offset (ΣV<sub>offset</sub>) equals V<sub>IO</sub> (comparator) (Figure 3) minus V<sub>IOX</sub> (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 kΩ integrator resistor. The clock frequency is 32 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to ensure good idle channel performance.

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**DEFINITION AND FUNCTION OF PINS**

**Pin 1 — Analog Input**

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

**Pin 2 — Analog Feedback**

This is the noninverting input to the analog signal comparator. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to V<sub>CC</sub>/2 at Pin 10 or ground.

The analog input comparator has bias currents of 1.0 µA max, thus the driving impedances at Pins 1 and 2 should be...
equal to avoid disturbing the idle channel characteristics of the encoder.

**Pin 3 — Syllabic Filter**

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6.0 to 50 ms are used in voice codecs.

**Pin 4 — Gain Control Input**

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V - I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/µs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop of fset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

**Pin 5 — Reference Input**

This pin is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

**Pin 6 — Filter Input**

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should always be between 8.0 kΩ and 13 kΩ to maintain good idle channel characteristics.

**Pin 7 — Analog Output**

This is the integrator op amp output. It is capable of driving a 600 Ω load referenced to V_{CC}/2 to +6.0 dBm and can otherwise be treated as an op amp output. Pins 5, 6 and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/µs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

**Pin 8 — VEE**

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

**Pin 9 — Digital Output**

The digital output provides the results of the delta modulator’s conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and noninverting with respect to Pin 2. It is locked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

**Pin 10 — V_{CC}/2 Output**

An internal low impedance mid-supply reference is provided for use in single supply applications. The internal regulator is a current source and must be loaded with a resistor to ensure its sinking capability. If a +6.0 dBm signal is expected across a 600 Ω input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is possible only if Pin 10 sources 3.66 mA into a resistor normally and will source the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 µF bypass capacitor from Pin 10 to V_{EE} is also recommended. The V_{CC}/2 reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

**Pin 11 — Coincidence Output**

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. The MC3418 contains a 4-bit register. Pin 11 is an open collector NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_S C_S while the decay constant is (R_S + R_P) C_S. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3.0 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4.0 kΩ to 12 V and C_L = 25 pF to ground.

**Pin 12 — Digital Threshold**

This input sets the switching threshold for Pins 13, 14 and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the V_{CC}/2 reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

**Pin 13 — Digital Data Input**

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 µs before and after the clock trigger for proper clocking.

**Pin 14 — Clock Input**

The clock input determines the data rate of the codec circuit. A 32 k bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum high time for the clock input is 300 ns and minimum low time is 900 ns.

**Pin 15 — Encode/Decode**

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

**Pin 16 — VCC**

The power supply range is from 4.75 to 16.5 V between Pin V_{CC} and V_{EE}.
Figure 1. Power Supply Current

Figure 2. $I_{\text{GCR}}$ – Gain Control Range and $I_{\text{Int}}$ – Integrating Current

Figure 3. Input Bias Currents, Analog Comparator Offset Voltage and Current

Figure 4. Integrator Amplifier Offset Voltage and Current

NOTE: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.
NOTES:
1. Integrator amplifier offset voltage plus slope polarity switch mismatch.
2. $V_{IOX}$ is the average voltage of the triangular waveform observed at the measurement points.

NOTES:
1. $V_{IO}$ (Note 1 and 2)
2. $V_{IOX}$ is the average voltage of the triangular waveform observed at the measurement points.

NOTES:
1. Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across $10 \, k\Omega$ resistor with $I_{GC} = 1.5 \, mA$.
2. See Note 2 in the Electrical Characteristics table.
3. See Figures 8 and 9.

TYPICAL PERFORMANCE CURVES

Figure 5. V/I Converter Offset Voltage, $V_{IO}$ and $V_{IOX}$

Figure 6. Dynamic Integrating Current Match

Figure 7. Typical $I_{Int}$ versus $I_{GC}$ (Mean ±2 σ)

Figure 8. Normalized Dynamic Integrating Current Match versus $V_{CC}$

$T_A = 25^\circ C$
$V_{CC} = 12 \, V$
(See Figure 6, Normalized to 10 kΩ)
$\bullet I_{GC} = 1.5 \, mA$
Figure 9. Normalized Dynamic Integrating Current Match versus Clock Frequency

![Graph showing normalized dynamic integrating current match](image)

Figure 10. Dynamic Total Loop Offset versus Clock Frequency

![Graph showing dynamic total loop offset](image)

Figure 11. Block Diagram of the CVSD Encoder

![Diagram of CVSD encoder](image)

Figure 12. CVSD Waveforms

![Waveforms diagram](image)
Figure 13. Block Diagram of the CVSD Decoder

Digital In → Sampler → Level Detect Algorithm → Slope Magnitude Control → Audio Out

Integrator → Slope Polarity Switch

Figure 14. 16 kHz Simplex Voice Codec (Single–Pole Companding and Single Integration)
The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

**The Delta Modulator**

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band-limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4.0 kHz and clock rates from 8.0 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

**The Companding Algorithm**

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator’s dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 4–bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single–pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all 1s, all 0s algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm operates only on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.
CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3418 is shown in Figure 14. This IC is a general purpose CVSD building block which allows the system designer to tailor the encoder’s transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application, and they are as follows:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single–pole networks. The selection of items 1 through 4 govern the codec performance.

Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13 and 14) from analog signal paths (Pins 1 to 7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications, the circuit in Figure 14 may be operated anywhere from 9.6 to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 16. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4–wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32 k bits and above. Other codecs may use bit rates up to 200 k bits/sec.

Shift Register Length (Algorithm)

The MC3418 has a 4–bit algorithm well suited for 32 kHz and higher clock rates. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal history. At 16 kHz and below, the 4–bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3418 is intended for high performance, high bit rate systems.
Figure 15. CVSD Circuit Schematic
Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor \( R_X \). \( R_X \) must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1.0 kHz of 0 dBm level. In practice, the useful dynamic range extends about 6.0 dB above the design level.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single–pole of 160 Hz is used.

\[
\frac{V_O}{I_i} = \frac{1}{C \left( \frac{R_S}{R} + \frac{1}{RC} \right)} = \frac{K}{S + \omega_0}
\]

where \( \omega_0 = 2 \pi f \)

\[10^3 = \omega_0 = 2 \pi f \]

\[f = 159.2 \text{ Hz} \]

Note that the integration filter produces a single–pole response from 300 to 3.0 kHz. The current required to move the integrator output a specific voltage from zero is simply:

\[
I_i = \frac{V_O}{R_1} + \left( C_1 \times \frac{dV_O}{dt} \right)
\]

Now a 0 dBm sine wave has a peak value of 1.0954 V. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1.0 kHz sine wave is:

\[
I_i = \frac{1.1 \text{ V}}{2 (10 \text{ k}\Omega)} + \frac{0.1 \mu\text{F} (1.1)}{0.125 \text{ ms}} = 0.935 \text{ mA}
\]

The voltage on \( C_S \) which produces a 33 \( \mu \text{A} \) current is determined by the value of \( R_X \):

\[
I_i = \frac{V_O}{R_1} + \left( C_1 \times \frac{dV_O}{dt} \right)
\]

The voltage on \( C_S \) which produces a 33 \( \mu \text{A} \) current is determined by the value of \( R_X \):

\[
I_i = \frac{0.1 \mu\text{F} 20 \text{ mV}}{62.5 \mu\text{s}} = 33 \mu\text{A}
\]

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one–zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3418 is tested to ensure that a 20 mVpp minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one–zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1 – 0 pattern.

To set the idle channel step size, the value of \( R_{min} \) must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (\( C_S \)) would decay to zero. However, the voltage divider of \( R_S \) and \( R_{min} \) (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

\[
I_i = \frac{V_O}{R_1} + \left( C_1 \times \frac{dV_O}{dt} \right)
\]

For values of \( V_O \) near \( V_{CC}/2 \) the \( V_O/R \) term is negligible; thus:

\[
I_i = \frac{\Delta V_O}{\Delta T}
\]

where \( \Delta T \) is the clock period and \( \Delta V_O \) is the desired peak–to–peak value of the idle output. For a 16 k bit system using the circuit in Figure 14:

\[
I_i = \frac{0.1 \mu\text{F} 20 \text{ mV}}{62.5 \mu\text{s}} = 33 \mu\text{A}
\]

The voltage on \( C_S \) which produces a 33 \( \mu\text{A} \) current is determined by the value of \( R_X \):

\[
I_i = \frac{0.1 \mu\text{F} 20 \text{ mV}}{62.5 \mu\text{s}} = 33 \mu\text{A}
\]

In Figure 14 \( R_S \) is 18 k\( \Omega \). That selection is discussed with the syllabic filter considerations. The voltage divider of \( R_S \) and \( R_{min} \) must produce an output of 41.6 mV.

\[
\frac{V_{CC} R_S}{R_S + R_{min}} = V_{Smin} R_{min} = 2.4 \text{ k}\Omega
\]

Having established these four parameters – clock rate, number of shift register bits, loop gain, and minimum step size – the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.
Integration Filter Design

The circuit in Figure 14 uses a single–pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1.0 or 2.0 dB by using a two–pole integration network. The improved circuit is shown in Figure 17.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1.0 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1.0 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low–pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2.0 kHz, and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz, and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low–pass filter which breaks at about 2.5 kHz.) The two–pole network in Figure 17 has a transfer function of:

\[ V_O = \frac{R0R1}{R2C2(R0 + R1)} \left( S + \frac{1}{R0 + R1C1} \right) S + \left( \frac{1}{R2C2} \right) \]

Figure 17. Improved Filter Configuration

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 17 represent one implementation of the telephony filter requirement.

The selection of the two–pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

\[ I_i = \frac{V_O}{R_0} + \left( \frac{R2C2}{R0} + \frac{R1C1}{R0} + C1 \right) \frac{\Delta V_O}{\Delta T} + \left( \frac{R2C2C1 + R1C1R2C2}{R0} \right) \frac{\Delta V_O^2}{\Delta T^2} \]

The calculation of desired gain resistor \( R_X \) then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single–pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across \( CS/VCC \).

The S/N performance may be improved by modifying the voltage to current transformation produced by \( R_X \). If different portions of the total \( R_X \) are shunted by diodes, the integrator current can be other than \( (VCC - VS)/R_X \). These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of \( R_X \) in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor–diode networks are shown in Figure 18.

Figure 18. Resistor–Diode Networks

If the performance of more complex diode networks is desired, the circuit in Figure 19 should be used. It simulates the companding characteristics of nonlinear \( R_X \) elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 21 provides excellent performance for 12 to 40 kHz systems.
Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5.0 mV minimum step size and a typical 1.0% current match from 15 µA to 3.0 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the 4-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 19, a telephone quality codec can be mass produced.

The circuit in Figure 19 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1.0 kHz test tone at a 37.7 k bit rate. At 37.7 k bits, 40 voice channels may be multiplexed on a standard 1.544 MB T1 facility. This codec has also been tested for 10-7 error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators, and small PABX installations.

The Active Companding Network

The unique feature of the codec in Figure 19 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C\textsubscript{s} divided by the voltage swing of the coincidence output. In Figure 19, the voltage swing of Pin 11 is 6.0 V. The operating companding ratio is analoged by the voltage between Pins 10 and 4 by means of the virtual short across Pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 V below V\textsubscript{CC}/2, then the positive input of A1 is (V\textsubscript{CC}/2 – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6.0 V).

The present step size of the operating codec is directly related to the voltage across R\textsubscript{x}, which established the integrator current. In Figure 19, the voltage across R\textsubscript{x} is amplified by the differential amplifier A2 whose output is single ended with respect to Pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 V. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at Pin 4 is amplified by A1. The output of A1 changes the voltage across R\textsubscript{x} in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at Pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R\textsubscript{x}, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on Pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R\textsubscript{x} and the gain of A2 and A1. The gain of A2 is also experimentally determined, but once determined, the circuit is easily repeated.

With no input signal, the companding ratio at Pin 4 goes to zero and the voltage across R\textsubscript{x} goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R\textsubscript{x}. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V\textsubscript{CC} and Pin 4 and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 20. A smooth 2.0 dB drop is realized from 12 dBm to –24 under the control of A1. At –24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R\textsubscript{x}. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 19 is designed specifically for 37.7 k bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 19 represents a significant step forward in the art and cost of CVSD codec designs.

* A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 19, 0.050 µF would work well.
Figure 19. Telephone Quality Deltamod Coder*

* Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.
Figure 20. Signal–to–Noise Performance and Frequency Response*

(a) Signal–to–Noise Performance of Telephony Quality Deltamodulator

(b) Frequency Response versus Input Level
(Slope Overload Characteristic)

*Showing the improvement realized with the circuit in Figure 19.

Figure 21. High Performance Elliptic Filter for CVSD Output

Designed for 0.28 dB ripple in the pass band
ω₀₁ = 3.0 kHz
ω₀₂ = 6.0 kHz
AdB at ω₀₂ and above 29.5 dB
Figure 22. Full Duplex/32 k Bit CVSD Voice Codec

**Codec Components**
- $R_{X1}, R_{X2} = 3.3$ kΩ
- $R_{P1}, R_{P2} = 3.3$ kΩ
- $R_{S1}, R_{S2} = 100$ kΩ
- $R_{I1}, R_{I2} = 20$ kΩ
- $R_{12} = 1.0$ kΩ
- $R_{M1}, R_{M2} = 15$ MΩ
- Minimum step size = 6.0 mV
- $C_{S1}, C_{S2} = 0.05$ µF
- $C_{I1}, C_{I2} = 0.05$ µF
1. 2 MC3418
2. 1 MC3403 (or MC3406)

**Input Filter Specifications**
- 12 dB/Octave Rolloff above 3.3 kHz
- 6.0 dB/Octave Rolloff below 50 Hz

**Output Filter Specifications**
- Break Frequency – 3.3 kHz
- Stop Band – 9.0 kHz
- Stop Band Atten. – 50 dB
- Rolloff – > 40 dB/Octave

**Filter Components**
- $R_{1} = 965$ Ω
- $R_{2} = 72$ kΩ
- $R_{3} = 72$ kΩ
- $R_{4} = 63.46$ kΩ
- $R_{5} = 127$ kΩ
- $R_{6} = 365.5$ kΩ
- $R_{7} = 1.645$ MΩ
- $R_{8} = 72$ kΩ
- $R_{9} = 72$ kΩ
- $R_{10} = 29.5$ Ω
- $R_{11} = 72$ kΩ
- $C_{1} = 3.3$ µF
- $C_{2} = 837$ pF
- $C_{3} = 536$ pF
- $C_{4} = 100$ µF
- $C_{5} = 222$ pF
- $C_{6} = 77$ pF
- $C_{7} = 38$ pF
- $C_{8} = 837$ pF
- $C_{9} = 536$ pF

**NOTE:**
1. All Res. 0.1% to 1%
2. All Cap. 0.1%
The salient feature of CVSD codecs is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required, and the cost objectives. To illustrate the choices available, the data in Figure 23 compares the signal-to-noise ratios and dynamic range of various codec design options at 32 k bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non–voice applications of the MC3418 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.
### OUTLINE DIMENSIONS

**P SUFFIX**

**PLASTIC PACKAGE**

**CASE 648–08**

**ISSUE R**

**NOTES:**
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION S DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

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<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
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<td>0.39</td>
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<td>0.040</td>
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**DW SUFFIX**

**PLASTIC PACKAGE**

**CASE 751G–02**

**(SO–16L)**

**ISSUE A**

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
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<th>MAX</th>
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